

Influence of AlN Growth Temperature on the Electrical Properties of Buffer Layers for GaN HEMTs on Silicon

Yvon Cordier, Rémi Comyn, Eric Frayssinet, Mario Khoury, Marie Lesecq,

Nicolas Defrance, Jean-Claude de Jaeger

▶ To cite this version:

Yvon Cordier, Rémi Comyn, Eric Frayssinet, Mario Khoury, Marie Lesecq, et al.. Influence of AlN Growth Temperature on the Electrical Properties of Buffer Layers for GaN HEMTs on Silicon. physica status solidi (a), 2018, 215 (9), pp.1700637. 10.1002/pssa.201700637. hal-03576045

HAL Id: hal-03576045 https://hal.science/hal-03576045

Submitted on 15 Feb 2022

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers. L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

Influence of AIN growth temperature on the electrical properties of buffer layers for GaN HEMTs on Silicon

Yvon Cordier¹, Rémi Comyn¹, Eric Frayssinet¹, Mario Khoury^{1,2}, Marie Lesecq², Nicolas Defrance², Jean-Claude DeJaeger²

¹ Université Côte d'Azur, CNRS, CRHEA, rue B. Grégory, 06560 Valbonne, France

² Université de Lille, UMR 8520 - IEMN, 59000 Lille, France

Despite a lower growth temperature is generally consid-ered as a drawback for achieving high crystal quality, the necessity to reduce the nucleation temperature of AlN on Silicon has permitted Molecular Beam Epitaxy (MBE) to demonstrate high performance for GaN transistors operating at high frequency. Compared to Metal-Organic Vapor Phase Epitaxy (MOVPE), the control of the interface between the AlN nucleation layer and the substrate is easier and the reduced growth temperature allows to obtain a more electrically resistive interface while keeping good crystal quality. More, we show that further reducing the growth temperature within the nucleation and stress mitigating layers has a noticeable impact on the lateral and vertical buffer leakage currents. At the same time the buffer of MBE grown HEMT structures exhibits low RF propagation losses (below 0.5 dB/mm up to 70 GHz). Also, results obtained with structures regrown by MOVPE on MBE AlN-on-Si templates confirm that the thermal budget is critical for the resistivity of AlN/Si. On the other hand, the insertion of a 1.5 μ m thick Al_{0.05}Ga_{0.95}N layer within a 2 μ m HEMT structure significantly improves the vertical breakdown voltage up to 740 V permitting to compare favourably with MOVPE epilayers with similar total thickness.

1 Introduction GaN on Silicon is a promising way to produce low cost electron devices. The most commonly used growth techniques for III-Nitride heterostructures are the Metalorganic Vapor Phase Epitaxy (MOVPE) and the molecular beam epitaxy (MBE), each of these techniques having its own advantages and drawbacks. While MOVPE is widely used due to larger throughput and larger wafer size handling capability, MBE operates at a lower temperatures under high vacuum with much less source products consumption and it is equipped with useful in-situ inspection tools such as reflection high energy electron diffraction (RHEED). MBE production tools for III-Nitrides are rare, but a lot of research reactors are used worldwide and are at the origin of demonstrations of optoelectronic and electronic devices. The most established way to grow III-Nitrides on Silicon starts with the growth of a nucleation layer made of AlN. This layer protects the substrate surface from exposure to Gallium, which can dope Silicon with acceptors and can react with Silicon at high temperature to result in a melt-back etching. For high performance lateral field effect transistors, high resistivity material is necessary to isolate the transistor channel from the Silicon substrate. In the following parts, the main features of ammonia source MBE growth are reminded and our experimental set-up is described. Then, the critical formation of the interface between the AlN nucleation layer and the Silicon substrate is discussed, and the influence of temperature on its electrical properties is studied. The critical role of the AlN growth temperature is further analized within thin simple GaN/AlN buffer structures and within thicker ones grown with stress mitigating stacks for High Electron Mobility Transistor (HEMT) applications. The results obtained for buffer resistivity and RF propagation losses confirm the main advantages of lowering the AlN growth temperature for these applications. More, MOVPE regrowth experiments performed on AlN-on-Silicon templates grown by MBE confirm that the thermal budget plays a critical role on the electrical properties of the interface with the substrate. Finally, we show that thanks to the control of the interface and the insertion of a 1.5 μ m Al_{0.05}Ga_{0.95}N layer in the buffer of a HEMT of total thickness below 2 μ m, a high vertical breakdown voltage of 740 V can be achieved leading to a breakdown field of 3.8 MV/cm.

2 Molecular Beam Epitaxy

2.1 Ammonia MBE growth The main features of ammonia-MBE (NH₃-MBE) are the followings. Ammonia thermally decomposes at the surface of the films at temperatures beyond 450°C [1]. The typical growth temperature for GaN is 800°C, while thick AlN films necessitate higher temperatures. Usually, AlGaN films can be grown in the 800-875°C temperature range, the optimum temperature depending on the Al content and the thickness of the film to be grown. Growth rates in the range of 0.5-1.5 µm/h are quite easy to achieve for GaN. The study described here has been made in a Riber Compact 21T MBE reactor equipped with an NH₃ gas injector [2,3], double filament Ga cells and cold lip Al cells to avoid creeping. The reactor configuration was optimized for uniform films on 2 in. diameter substrates [2]. Nevertheless, even with this configuration, the GaN thickness uniformity deviation is below 3% on 3 in. diameter. The optimum growth conditions are N-rich, i.e require a large ammonia flow rate (maximum of 200 sccm in our MBE reactor). Last points

concerns the growth of AlGaN alloys. The desorption of Ga and Al species is negligible when AlGaN is grown at 800°C with a large ammonia flow rate, so that composition and growth rate calibrations are more easy. More, at such temperature, AlGaN does not relax the strain via composition modulations [4], which is a noticeable advantage compared to MOVPE [5].

2.2 The AIN/Si interface The formation of the AlN/Si interface achieved using NH3-MBE has been studied by Lelouarn et al [6]. The growth process developed from this study starts with the exposure of the Si(111) surface to ammonia and the nucleation of AlN at a reduced temperature below 650°C, followed by a quick temperature ramping beyond 800°C while pursuing the growth of the following AlN layers. Contrary to MOVPE grown material [7], it follows from such a process a flat well defined interface with no sign of amorphous or highly perturbed crystal layers as confirmed by transmission electron microscopy [8]. The absence of a Silicon Nitride film at the interface is an advantage for achieving better crystal quality films. More, a consequence of this low temperature process is a reduced risk of exposing the Silicon surface to Aluminum and residual Gallium, and consequently a limited p-type doping of the substrate as verified by measuring the sheet resistance of grown samples (R>20kOhms/sq, the limit of our contactless resistance measurement setup).



Figure 1 Tapping mode AFM view of the surface of 20 nm (left) and 160 nm thick (right) AlN layers grown by NH₃-MBE on Silicon.

As shown in Fig.1 (left picture), the growth rapidly results in smooth and pit-free AlN films, which seems different from MOVPE [9]. Atomic Force Microscopy (AFM) shows surfaces with typical root mean square roughness (rms) well below 1 nm (typically < 0.3 nm) at the micrometre scale.

Fig.2a shows the capacitance-voltage (C-V) profile measured with a Mercury probe (central dot diameter 792 μ m) obtained on a thin 20 nm AlN film grown by MBE at 920°C on a high purity (float zone) Silicon substrate with a nominal resistivity ρ >5kOhms.cm. At negative bias, a low n-type doping level (few 10¹³/cm³) is deduced from the profile while a low accumulation of electrons is noticed at positive bias for the low frequency range (1-20 kHz) used for this quite resistive sample.



Figure 2 C-V profile of 20nm AlN layers grown by NH₃-MBE (a) and annealed for 90 min at 1050° C under NH₃ (b) and 160nm AlN layer grown by NH₃-MBE at 920°C (c).

The same measurement performed after annealing the sample under NH3 at 1050°C for 90 min to simulate GaN growth conditions in a MOVPE reactor shows a drastic change with a slow decrease of capacitance towards positive bias that may indicate the presence of holes at the AlN/Si interface and probably the beginning of electron accumulation at positive bias (Fig.2b). At the same time the sheet resistance drops below 10kOhms/sq, which may be due to the diffusion of Aluminum or residual Gallium into the substrate [10]. However the diffusion of Gallium through AlN is less likely due to the absence of pinholes. Only small dislocation pits can be observed with AFM. Furthermore, AlN nucleation layer is almost totally relaxed by misfit dislocations with an edge component in the plane of the interface and typical spacing of 5 AlN / 4 Si atomic rows. The stability of the interface may be reduced by the presence of such numerous defects with dangling bonds at the interface. On the other hand, the C-V profile recorded on a 160 nm thick AlN nucleation layer grown at 920°C confirms a p-doped like behaviour with acceptors located at the AlN/Si interface (Fig.2c). It is also important to notice that in-spite of the presence of such charges, the sheet

resistance of the sample remains superior to 20kOhms/sq and it is difficult to evidence dislocation pits with AFM on such a surface (Fig.1, right picture).

3 Reduction of the AIN growth temperature The HEMT structures developed on Silicon have been optimized with AlN layers grown in the 900-920°C temperature range [11]. The reason behind is a trade-off between the enhanced crystal quality of AlN and the detrimental effects of temperature rising in the MBE reactor such as parasitic outgassing for instance. More, 900°C is already too high for the monolithic integration of III-Nitride devices with Silicon devices in a CMOS first approach due to dopant diffusion [12,13]. In this context, reducing the growth temperature of AlN is mandatory and the attempts we performed led to conclude that AlN can be grown by NH3-MBE with limited degradation of the crystal quality in the 830-850°C temperature range [13,14]. In order to assess the influence of AlN growth temperature on the electrical properties, AlGaN/GaN HEMTs with thin and thick GaN buffer layers were grown. The electrical properties of the 2DEG and transistors achieved on these structures are reported in [13,14]. Thin buffers consist of 0.5 µm GaN grown on 0.2 µm AlN nucleation layer, while thick buffers consist of 1.5 μm GaN grown on 0.4-0.5 μm thick AlN/GaN/AlN stress mitigating stacks. The electrical properties of the buffer layers are reported hereafter.

3.1 Leakage current Fig.3 shows the thin buffer lateral leakage current assessed on 1 mm total width isolation patterns consisting of inter-digitated ohmic contacts pads with 5 μ m, 10 μ m and 20 μ m gaps. The substrate is not grounded. As reported in [15] the leakage current in thin structures HEMT is very sensitive to the vicinity of the Silicon substrate.



Figure 3 Lateral buffer leakage current assessed with $2x10x100 \mu$ m contacts with 5, 10 and 20 μ m spacings for thin HEMT structures with AlN grown by NH₃-MBE at 830°C and 920°C.



Figure 4 Vertical leakage current through the buffer layers of thin HEMT structures with AlN grown by NH₃-MBE at 830°C and 920°C.

The effect of lowering the AlN growth temperature is also noticeable for the vertical leakage current measured between the biased surface ohmic contacts and the substrate which is grounded (Fig.4). Secondary Ion Mass Spectrometry (SIMS) profiles of these structures show that the only noticeable difference is the Silicon concentration which seems to drop down more rapidly from AlN/Si interface to the upper part of the AlN layer when grown at lower temperature (Fig.5). In spite of a larger activation energy compared with GaN, Silicon is a donor in AlN [16], so a steeper drop of Silicon concentration may reduce the leakage. Otherwise, another explanation to enhanced electrical resistivity could be a larger amount of electrical defects able to trap any carriers. If confirmed, this last effect could make the combination of low temperature with high temperature growth steps interesting for enhancing the crystal quality while keeping a highly resistive interface.

The I-V curves shown in the inset of Fig.4 are not symmetric, with a larger reverse current at low bias as already reported by Perez-Tomas [17] and in agreement with results obtained on thin AlN MOVPE grown on pdoped Silicon [18]. However, considering the C-V profile presented in Fig.2c, further analysis is necessary to say if the model involving the presence of an electron inversion layer can be applied here. SIMS profiles performed in order to estimate the amount of Aluminum and Gallium species at the interface are shown in Fig5.b and Fig.5d. Gallium rapidly reaches the detection limit which confirms the absence of contamination from the MBE reactor. Furthermore, the steep Aluminum concentration drop at the interface is very similar for both structures. Even when some Aluminum doping may explain the C-V results presented in Fig.2, the SIMS profiles may indicate that Aluminum diffusion alone is not likely to explain the two orders of magnitude difference in vertical resistivity shown



Figure 5 SIMS profiles recorded for Carbon, Oxygen, Silicon, Gallium and Aluminum elements within buffer layer structures with AlN grown by NH₃-MBE at 920°C (a,b) and 830°C (c,d). Only the Si profiles show noticeable differences.

The vertical leakage currents recorded in the same configuration in thick buffer HEMT structures are shown in Fig.6. As for thin structures, a noticeable reduction of the leakage is obtained with the lowering of the AlN growth temperature. Also, the asymmetric I-V curves confirm the behaviour revealed by thin buffer structures.



Figure 6 Vertical leakage current through the thick buffer of HEMTs with AlN grown by NH₃-MBE at 830°C and 920°C.

3.2 High frequency propagation losses As already mentioned, MBE offers the possibility to grow Alrich AlGaN barriers producing HEMTs with interesting high frequency performances [4]. However, the fabrication of performing Microwave Monolithic Integrated Circuits (MMICs) also requires minimal wave propagation losses, which is challenging for devices made on Silicon substrate, especially at frequencies of several tens of GHz. For these substrates with high resistivity reasons, (several kOhms.cm) are preferable. Nevertheless, as already mentioned, the presence of electrical carriers in the buffer layers or in the substrate can significantly reduce the overall resistivity. Beyond trying to increase the resistivity by using lower growth temperatures, a complementary way to reduce RF propagation losses is to increase the resistive buffer laver thickness in order to reduce the capacitive coupling of the device with the lossy buried region. In such a way, Lecourt et al measured RF losses of 0.4 dB/mm at 50 GHz on a 2.5 µm thick structure grown by NH₃-MBE on resistive $(\rho > 1 k \Omega. cm)$ Si(111) substrate [20]. Fig.7 shows propagation losses recorded for the thin buffer layers previously discussed, namely 0.5 µm GaN on 0.2 µm AlN nucleation layers grown at 830°C and 920°C respectively. It is interesting to note that the losses measured in this case are not so sensitive to growth temperature, probably because the electric field is small and the sheet resistance is already beyond a threshold that can be estimated higher than 10 kOhms/sq. Propagation losses below 0.3 dB/mm and 0.5 dB/mm are obtained up to 35 GHz and 70 GHz respectively. Such results approach the ones obtained while growing the lavers at even lower temperature (750°C) with plasma assisted MBE [12] and reaching ~0.2 dB/mm at 35 GHz as well as ones published recently in [19]. Even though the growth conditions are not detailed in this last paper, it

1

appears that the crystal quality of AlN layers grown by MOVPE in this work is very poor with broad X-ray diffraction (XRD) peaks. The full width at half maximum (FWHM) of symmetric (002) omega scans is 1.9-2.4° which is noticeably broader than the 0.3-0.5° recorded for our MBE grown layers. Furthermore, the corresponding roughness of AlN layers is 3-3.4 nm while it is well below 1 nm in the MBE grown films. From our own experience, HEMT structures with AlN layers grown by MOVPE at temperatures higher than 1100°C produce good crystal quality materials [21] with AlN (002) XRD peak width well below 1° and transistors with good DC performance, but with RF losses over passing 6 dB/mm.



Figure 7 RF propagation losses in thin GaN/AlN buffer layers grown on Silicon by NH₃-MBE.

To evaluate the influence of the AlN growth temperature in a MOVPE environment, GaN / AlN structures have been regrown at different temperatures on 40 nm AlN on Silicon templates grown by MBE. The propagation losses are reported in Fig.8. The Silicon substrate is highly resistive $(\rho > 1 \text{ kOhms.cm})$. So the losses recorded for the substrate alone are well below 1 dB/mm. The first sample consists of 700 nm GaN grown at 1000°C on 120 nm AlN regrown at 1200°C. It produces propagation losses in the range of 6 dB/mm at 40GHz. The second sample with AlN regrown while grading the temperature from 1000°C to 1200°C presents noticeably lower losses in the range of 2 dB/mm. This result is still not sufficient to use such a scheme for high performance RF circuits, but it confirms the critical role of the growth thermal budget on the electrical resistivity of the buried region in structures grown on Silicon. The FWHM of AlN(002) XRD peaks is still below 0.4° for these samples. Considering these results, we believe that there is room for further reduction of the AlN growth temperature with MOVPE thanks to the quality of the MBE grown templates. More, as a better crystal quality is helpful to grow more compressively strained AlGaN and GaN layers, it is expected from such a scheme more freedom to grow highly resistive thick films so that the reduction of capacitive coupling will combine with a larger resistivity of the AlN/Si interface and will contribute to the overall reduction of the propagation losses.



Figure 8 RF losses in GaN/AlN buffer layers regrown by MOVPE on NH₃-MBE AlN/Si templates.

4 AIGaN buffer HEMT Structures with Aluminum in the buffer layer have been proposed to increase buffer resistivity as well as to enhance the confinement of the carriers located in the 2DEG, which is important both for high frequency and for high power applications. In a previous work, AlGaN/GaN double heterojunction HEMTs with 50 nm GaN channel were grown on Silicon to confirm this interest [22]. The buffer layers consisted of 10% Al molar fraction AlGaN with thicknesses ranging from 1 µm to 1.5 µm grown on 0.5 µm stress mitigating stacks. In the present study, a 1.5 µm thick AlGaN buffer HEMT was grown with a lower Aluminum molar fraction of 5% but a thinner GaN channel (10 nm) to preserve an efficient carrier confinement. The purpose of such a reduction of the Al content is to find a tradeoff in terms of resistivity and crystal quality. Thanks to the presence of Aluminum which limits the development of mounds related to kinetic roughening [23] the rms roughness is lower than 2 nm for $2x2 \ \mu m^2$ AFM scans, to be compared with 4-5 nm for thick GaN. More, the stress mitigating stack was grown with AlN and Al_{0.15}Ga_{0.85}N layers in order to increase the resistivity.

A simple photolithography process was applied to define test patterns such as TLM (transmission line model) and transistors. It consists in Cl₂/CH₄/Ar reactive ion etching for 100 nm depth mesa fabrication followed by ebeam deposition and rapid thermal annealing (750°C for 30s) of TiAlNiAu ohmic contacts, and finally the NiAu metallization for Schottky gates followed by access pads. The contact resistance extracted from TLM measurements is R_c=0.3 Ohm.mm and the sheet resistance is 710 Ohms/sq. Fig.9 shows the DC output characteristics and the transfer characteristics of a transistor with a 3 µm gate centred in a source to drain spacing of 13 µm. A 150 mA/mm drain current is obtained at V_{gs}=0V and the threshold voltage is around -2.5V. The drain and gate leakages merge below 1 μ A/mm at device pinch-off. The substrate is not grounded

and the bias seems too low to involve the Si substrate as a leakage path. Such a residual leakage current may find its origin either from the non-passivated surface states or from the buffer layer. Indeed, the device is not passivated and it is isolated by mesa etching so the gate pad is deposited at the surface of the buffer layer. To clarify this point, vertical breakdown voltage measurements have been performed in a specific set-up able to sustain voltages up to 3kV [25]. Again, substrate is grounded and positive bias is applied to the ohmic contacts at the surface. To avoid flash, the sample is dipped into Fluorinert prior to measurements.



Figure 9 DC output characteristics (top) and transfer characteristics (bottom) of a transistor fabricated on AlGaN/GaN DH-HEMT with AlGaN buffer grown by NH₃-MBE on Silicon.

I-V measurement recorded for vertical current configuration is shown in Fig.10. For the three devices reported here, it appears that beyond 100V the leakage current evolves almost exponentially with the voltage to reach a threshold of about 10⁻² A/cm² where a destructive breakdown occurs. The maximum bias sustained by the devices is 740V. Considering the total thickness of the structure below 2 µm, this is among the best values reported for structures of similar thicknesses grown on Silicon. For comparison, a 2.3 µm thick HEMT structure grown previously with a GaN buffer exhibited a vertical breakdown voltage higher than 400V [17]. More, the present result compares favourably with the 700V breakdown voltage recorded in lateral configuration with substrate floating on a 2 µm thick MOVPE grown structure with an Al_{0.25}Ga_{0.75}N buffer [25] and with the 750V obtained in the same configuration by Herbecq [24] on a HEMT

structure with a 1.6 μ m Al_{0.04}Ga_{0.96}N buffer grown by MOVPE on a transition layer stack.



Figure 10 Leakage current recorded in the vertical configuration for a DH-HEMT structure grown by NH₃-MBE.

5 Conclusion The influence of the temperature has been investigated for the NH₃-MBE growth of GaN HEMTs on Silicon substrate. In particular, lower growth temperature of AlN nucleation layer is shown to be a key parameter to enhance the resistivity of the buffer layers which results in low RF propagation losses, reduced leakage currents and larger breakdown voltages. More, we have shown that compared with MOVPE, MBE grown AlN films are of much better crystal quality (dislocation density, roughness) which offers more flexibility in the structures design to avoid cracking and which can result in superior reliability. These results may be explained by the absence of Silicon Nitride at AlN/Si interface combined with a limited Aluminum diffusion in the substrate but sufficient to mitigate the formation of an electron inversion layer. The MOCVD regrowth of GaN/AlN on thin MBE AlN on Silicon templates has also confirmed the critical role of the thermal budget on the buffer resistivity. Studies are going on to determine how far the MOCVD growth temperature can be lowered thanks to the benefit of the good crystal quality AlN achieved with NH₃-MBE.

Acknowledgements This work has been supported by the technology facility network RENATECH and the French National Research Agency (ANR) through the projects Infra SATELLITE, ASTRID GoSiMP, DESTINEE and the "Investissements d'Avenir" program GaNeX (ANR-11-LABX-0014). Ezgi Dogmus, Malek Zegaoui, and Farid Medjdoub are deeply acknowledged for the high voltage breakdown measurements.

References

- [1] M. Mesrine, N. Grandjean, and J. Massies, Appl. Phys. Lett. 72, 350 (1998).
- [2] Y. Cordier, F. Pruvost, F. Semond, J. Massies, M. Leroux, P. Lorenzini, and C. Chaix, Phys. Status. Solidi C 3, 2325 (2006).
- [3] Y. Cordier, F. Semond, J. Massies, M. Leroux, P. Lorenzini,
- and C. Chaix, J. Crystal. Growth 301-302, 434 (2007).
 - [4] Y. Cordier, Phys. Status Solidi A 212, 5, 1049-1058 (2015).
 - [5] J. Derluyn, S. Boeykens, K. Cheng, R. Vandersmissen, J.
- Das, W. Ruythooren, S. Degroote, M. R. Leys, M. Germain, and G. Borghs, J. Appl. Phys. 98, 054501 (2005).
 - [6] A. Le Louarn, S. Vézian, F. Semond and J. Massies
- J. Cryst. Growth 311 (2009) 3278
- [7] G. Radtke, M. Couillard, G. A. Botton, D. Zhu, and C. J.
- Humphreys, Appl. Phys. Lett. 100, 011910 (2012).
- [8] F. Semond, Y. Cordier, N. Grandjean, F. Natali, B.
- Damilano, S. Vézian, and J. Massies, Phys. Status Solidi A 188, 501 (2001).
- [9] J. J. Freedsman, A. Watanabe, Y. Yamaoka, T. Kubo, and T. Egawa, Phys. Status Solidi A 213, p.424 (2016).
- [10] H. Shinichi, I. Masanori, M. Toshiharu, O. Hideyuki,M. Yoshiaki, T. Isao, T. Fumihiko, S. Shohei, and E. Takashi, Appl. Phys. Express 2, 061001 (2009).
- [11] N.Baron, Y.Cordier, S.Chenot, P.Vennéguès, O.Tottereau, M.Leroux, F.Semond, and J.Massies, J. Appl. Phys. 105, 033701 (2009).
- [12] W. E. Hoke, R. V. Chelakara, J. P. Bettencourt, T. E. Kazior,
- J. R. Laroche, T. D. Kennedy, J. J. Mosca, A. Torabi, A. J. Kerr,
- H.-S. Lee, T. Palacios, J. Vac. Sci. Technol. B 30, 02B101 (2012).[13] R. Comyn, Y. Cordier, S. Chenot, A. Jaouad, H. Maher, V. Aimez, Phys. Status Solidi A 213, p.917 (2016).
- [14] R. Comyn, Y. Cordier, V. Aimez, and H. Maher, Phys. Status Solidi A 212, 1145 (2015).
- [15] P. Leclaire, S. Chenot, L. Buchaillot, Y. Cordier, D. Theron,M. Faucher, Semicond. Sci. Technol. 29 115018 (2014).
- [16] S. Contreras, L. Konczewicz, J. Ben Messaoud, H. Peyre,
 M. Al Khalfioui, S. Matta, M. Leroux, B. Damilano, J. Brault,
 Superlattices and Microstructures, 98, 253 (2016).
- [17] A. Pérez-Tomás, A. Fontserè, J. Llobet, M. Placidi, S.
 Rennesson, N. Baron, S. Chenot, J. C. Moreno, and Y. Cordier, J.
 Appl. Phys. 113, 174501 (2013).
- 1 [18] H. Yacoub, D. Fahle, M. Finken, H. Hahn, C. Blumberg,
- W. Prost, H. Kalisch, M. Heuken, and A. Vescan, Semicond. Sci.
 Technol. 29, 115012 (2014).
- 44 [19] T.T. Luong, F. Lumbantoruan, Y.-Y. Chen, Y.-T. Ho, Y.-C.
- Weng, Y.-C. Lin, S. Chang, E.-Y. Chang, Phys. Status Solidi A, 214, 1600944 (2017).
- [20] F. Lecourt, Y. Douvry, N. Defrance, V. Hoel, Y. Cordier, and J. C. De Jaeger, in: Proc. 5th European Microwave Integrated Circuits Conference (EuMIC), Paris, September 27–28, 2010, pp. 33–36.
- [21] E. Frayssinet, P. Leclaire, J. Mohdad, S. Latrach, S. Chenot,
 M. Nemoz, B. Damilano and Y. Cordier, Phys. Status Solidi A 214,
 1600419 (2017).
- [22] Y. Cordier, F. Semond, M. Hugues, F. Natali, P. Lorenzini,
 H. Haas, S. Chenot, M. Laügt, O. Tottereau, P. Vennegues, J.
 Massies, J. Crystal. Growth Vol 278/1-4, 393 (2005).
- [23] S. Vézian, F. Natali, F. Semond, and J. Massies, Phys. Rev.
 B 69, 125329 (2004).

[24] N. Herbecq, I. Roch-Jeune, N. Rolland, D. Visalli, J. Derluyn, S. Degroote, M. Germain, and F. Medjdoub, Appl. Phys. Express 7, 034103 (2014).

[25] Kai Cheng, H. Liang, M. Van Hove, K. Geens, B. De Jaeger, P. Srivastava, X. Kang, P. Favia, H. Bender, S. Decoutere, J. Dekoster, J. Ignacio del Agua Borniquel, S. W. Jun, and H. Chung, Appl. Phys. Express 5, 011002 (2012).

1