Horizontal Hall Effect Sensor with High Maximum Absolute Sensitivity

Jean-Baptiste Kammerer, Luc Hebrard, Vincent Frick, Philippe Poure, Francis Braun

Horizontal Hall Effect Sensor with High Maximum Absolute Sensitivity

Jean-Baptiste KAMMERER*, Luc HEBRARD *Member, IEEE*,
Vincent FRICK *Member, IEEE*, Philippe POURE, Francis BRAUN

Index Terms

magnetic sensor, Hall effect, short-circuit effect, high sensitivity, CMOS microsystem

Abstract

The sensitivity of conventional Hall effect sensors is strongly limited by the well known short-circuit effects. Many researches were devoted to reduce offset and noise but few works were carried out to improve the sensitivity. Here, a new shape of integrated horizontal Hall effect device is presented. This particular shape has been developed in order to minimize the short-circuit effects in the sensor, allowing to reduce its length to width ratio and consequently to reduce its average resistance. Thus the biasing current of this sensor can be significantly increased in order to obtain a higher absolute sensitivity than for conventional devices. Such a Hall effect device needs a specific biasing circuit which is also presented, first in a simple version and second in an improved one. A resolution of $32\mu T$ has been reached on a bandwidth of $5Hz$ to $1kHz$ with a $39 \times 9.2\mu m^2$ sensor biased with a current of $2.07mA$, the corresponding absolute sensitivity being $195mV/T$. The maximal absolute sensitivity of a so shaped device can be increased as much as needed by increasing its width-to-length ratio, without loss on the current related sensitivity.

INTRODUCTION

The sensitivity of conventional Hall effect devices is strongly limited by the well known short-circuit effects [1], [2]. In order to improve the signal to noise ratio of magnetic field measurement systems, many researches were devoted to reduce the offset and the low frequency noise level [3], [4], but few works were carried out to improve the maximal absolute sensitivity of Hall effect sensors. In applications such as contactless AC current measurement [5], the offset of the Hall device is not a limiting factor. On the other hand, improving its absolute sensitivity helps in designing magnetic sensors with a good signal-to-noise ratio. Indeed, the higher the sensitivity of the sensor is, the higher the noise level of the amplifier can be and the easier its design is. To achieve a high sensitivity, some ferromagnetic flux concentrators may be used [6]. Since this solution needs post-processing for ferromagnetic deposition, the so fabricated microsystems are necessarily more expensive than conventional Hall effect devices based microsystems. Here, a new shape of integrated horizontal Hall effect device is proposed. This new shape allows to minimize the short-circuit effects due to the biasing contacts and consequently allows to increase the maximal absolute sensitivity of the device. The resulting sensing element needs a specific biasing circuit which is also presented. Two microsystems have been realized using a standard CMOS $0.6\mu m$ integrated circuit technology. The first one uses a simple biasing circuit which leads to a quite low resolution, while the second one uses a more complex biasing circuit which allows to get the best performances from the new shape of Hall effect device. In the first section of this paper, a theoretical study of the new device is done and numerical simulations results are presented as proof of the validity of the theoretical formulae. In the second section, we present two specific biasing circuits which allow to bring the new Hall effect device into operation. Finally, some experimental results that confirm our assumptions are discussed and comments about the biasing technique are given in the last sections of this paper.

I. THE NEW DEVICE

A. The Hall effect

Figure 1 presents a conventional rectangular Hall effect device. In a thin and infinitely long device with punctual sensing contacts (i.e. an ideal device), the Hall voltage V_H appearing between these sensing contacts (S1 and S2 on figure 1) is proportional to the magnetic field component perpendicular to the plate plane (B_z) and to the biasing current (I) [1]:

$$|V_H| = \left| \frac{R_H}{t} I \cdot B_z \right| \tag{1}$$

$$R_H = \frac{r_n}{q n_c} \tag{2}$$

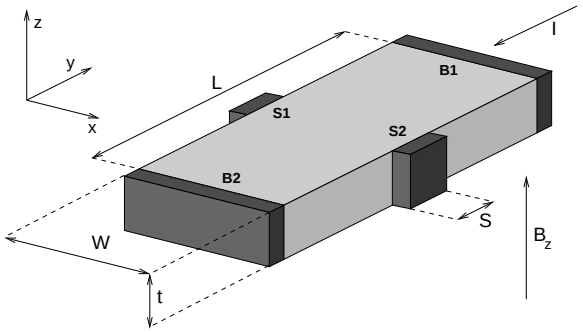

Fig. 1. Conventional rectangular Hall effect device

where R_H denotes the Hall coefficient, t the thickness of the plate, q the magnitude of the electron charge, n_c the carrier density and $r_n \approx 1.15$ the scattering factor of silicon.

B. Rectangular Hall devices

In practical rectangular Hall effect devices (figure 1), the biasing (B1 and B2) and the sensing contacts are responsible for the short-circuit effects which reduce the Hall voltage by a geometry dependent correction factor $G_{rect} < 1$. Under low induction, the geometrical correction factor G_{rect} of a long rectangular Hall plate ($\frac{L}{W} > 1.5$) with small sensing contacts ($\frac{S}{W} < 0.18$) can be approximated by the following formula [1]:

$$G_{rect} \simeq \left[1 - \exp\left(-\frac{\pi}{2}\frac{L}{W}\right)\right] \cdot \left[1 - \frac{2}{\pi}\frac{S}{W}\right] \tag{3}$$

where L and W denote the length and the width of the device, and S is the sensing contacts size (figure 1). The first term of (3) takes account for the Hall voltage reduction due to the large current supplying contacts B1 and B2 while the last term takes account for the current lines deflection near the sensing contacts S1 and S2. To keep G_{rect} close to unity, L has to be greater than W. Consequently, the resistance R_{rect} between the biasing contacts of conventional rectangular Hall devices is generally large:

$$R_{rect} = R_{\square}\frac{L}{W} \tag{4}$$

$$R_{\square} = \frac{1}{q\mu n_c t} \tag{5}$$

$R_{\square}$ is the square resistance of the device material and μ the conductivity mobility. Since the device biasing voltage is limited to V_{pow}, the maximal power supply voltage allowed by the CMOS technology,

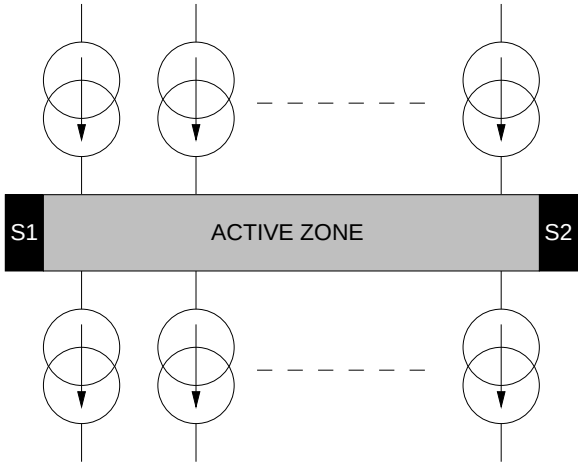

Fig. 2. The biasing principle

the biasing current I is limited to $\frac{V_{pow}}{R_{rect}}$. As a consequence the absolute sensitivity $\frac{V_H}{B_z}$ of a conventional rectangular Hall device cannot be higher than S_{max}:

$$\begin{aligned} S_{max} =& G_{rect}\frac{R_H}{t}\frac{V_{pow}}{R_{rect}} \\ =& G_{rect} r_n \mu V_{pow}\frac{W}{L} \\ \lesssim& r_n \mu V_{pow}\frac{W}{L} \end{aligned} \tag{6}$$

C. Multiple strips Hall device

To overcome this sensitivity limitation, i.e. to reduce the input resistance while keeping the geometrical correction factor close to one, a new shape of horizontal Hall effect device has been developed. This particular shape is based on a principle first proposed by Popović for MagFETs (Magnetic Field Effect Transistor) [2]. It consists in supplying the current into a short Hall effect active zone with multiple "distributed current sources" (figure 2). Since the output impedance of theses sources are very high, the device behaves as if it were infinitely long while it is kept short. To apply such a biasing principle to conventional rectangular devices, we replaced both current supplying contacts B1 and B2 by multiple narrow strips (length l, width w) while keeping the rectangular active zone (length L, width W) as short as allowed by the manufacturing process (figure 3). The resulting device is equivalent to multiple rectangular Hall effect devices (length $[2l + L]$, width w) merged together. Since the biasing contacts B1a-d and B2a-d (figure 3) of theses elementary devices are responsible for residual short-circuit effects,

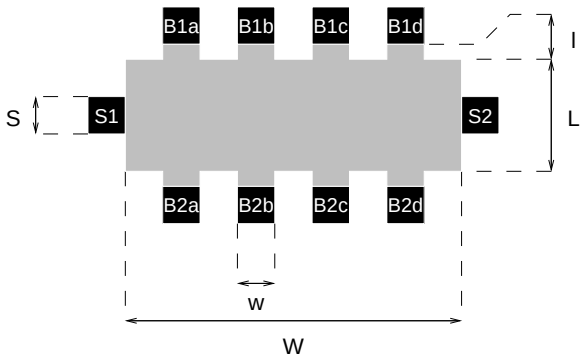

Fig. 3. The new shape (4 strips)

the expression (3) can be adapted to the new shape, leading to the geometrical correction factor G_{new} of a multiple strips device:

$$G_{new} \simeq \left[1 - \exp\left(-\frac{\pi}{2}\frac{2l+L}{w}\right)\right] \cdot \left[1 - \frac{2}{\pi}\frac{S}{W}\right] \tag{7}$$

Expression (7) is valid for $\frac{2l+L}{w} > 1.5$ and $\frac{S}{W} < 0.18$. The average input resistance R_{new} is now given by:

$$R_{new} \simeq R_{\square}\left(\frac{1}{n}\frac{l}{w} + \frac{L}{W} + \frac{1}{n}\frac{l}{w}\right) = R_{\square}\left(\frac{L}{W} + \frac{2}{n}\frac{l}{w}\right) \tag{8}$$

where n is the number of current supplying strips. Since $W \gtrsim nw$, R_{new} is overvalued by:

$$R_{new} \lesssim R_{\square}\frac{1}{n}\frac{2l+L}{w} \tag{9}$$

The average input resistance of the new device is then about n times smaller than the biasing resistance of a rectangular device with the same geometrical correction factor:

$$\begin{aligned} G_{new} = G_{rect} \Rightarrow \left[\frac{2l+L}{w}\right]_{new} &= \left[\frac{L}{W}\right]_{rect} \\ \Rightarrow R_{new} &\lesssim \frac{R_{rect}}{n} \end{aligned} \tag{10}$$

Finally, for a given power supply voltage V_{pow}, the maximal biasing current and, as a consequence, the maximal absolute sensitivity are also about n times greater than for a conventional rectangular Hall device.

D. Numerical simulations

To verify our hypothesis, we have compared the simulated behavior of a four strips device to the simulated behavior of a rectangular plate. These simulations were carried out with ISE-TCAD® since, to

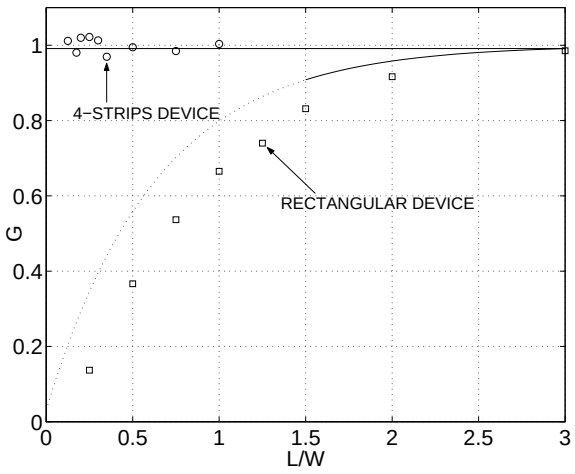

Fig. 4. Simulated (circles and squares) and theoretical (solid lines) geometrical correction factors (eq. (3) and (7))

our knowledge, it is the only three dimensional semiconductor device simulator available on the market that takes account for the magnetic field [7]. We first have simulated the influence of the ratio $\frac{L}{W}$ on the behavior of a rectangular device similar to the one shown on figure 1. Secondly, the influence of the ratio $\frac{L}{W}$ on the geometrical correction factor of a four strips device with $\frac{2l+L}{w} = 3$ has been extracted from simulations. In order to maintain constant the ratio $\frac{S}{W}$ appearing in (7), only L and l were varied while keeping the sum $2l + L$ constant. The simulations results presented on figure 4 clearly show that the influence of $\frac{L}{W}$ on the geometrical correction factor is negligible and that G_{new} essentially depends on the ratio $\frac{2l+L}{w}$ as predicted by (7). As a consequence, the dimensions of the device can be adjusted in order to reduce the average input resistance while keeping a geometrical correction factor close to one. This resistance reduction has also been verified, giving a numerical proof of the validity of relations (7) and (8).

II. Specific biasing circuit

A. Simple biasing circuit

Such a n-strips device needs $2n$ matched current sources ($I_{source} = \frac{I}{n}$) to be correctly biased. Thus, a specific biasing circuit has been developed. It consists in a low noise operational transconductance amplifier with n identical output stages in which the device is inserted as proposed by Frick [8] for the biasing of conventional rectangular devices (figure 5). The non-inverting input of the biasing amplifier is connected to the ground and its inverting input to one of the sensing contacts. The fed back sensing contact

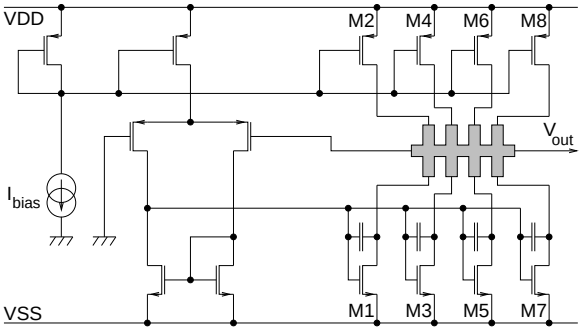

Fig. 5. A simple biasing circuit suitable for a four strips device

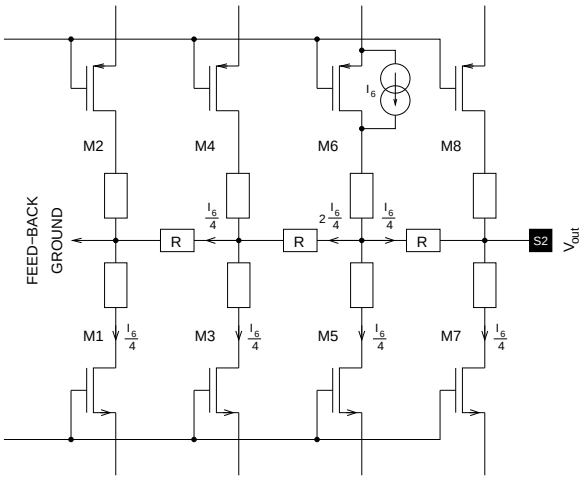

Fig. 6. Noise generated by the resistive coupling of the output stages

is then maintained at the ground potential while it is connected to a high impedance node. The other sensing contact is the output of the resulting system (biasing amplifier + Hall device). As a consequence, the output reads $V_{out} = V_H$ and can be easily amplified for further signal processing. Because of the resistive coupling between the output stages thru the n-strips Hall effect device, this simple biasing circuit leads to a quite low signal to noise ratio, in particular at low frequency where $1/f$ noise is predominant. In order to understand this coupling phenomenon, let us assume that the M6 transistor generates a noise current (figure 6), all others transistors (M1-M5 and M7-M8) being noiseless. This noise current I_6 can't flow to the sensing contacts which are connected to high impedance nodes. As a consequence, assuming a high open-loop gain for the amplifier ($A_{V0} \gtrsim 5000$), the common potential applied on the gates of M1, M3, M5 and M7 is automatically adjusted in order to maintain the fed back sensing contact to the

ground potential and to sink the current I_6. Finally, a part of the noise current I_6 flows horizontally thru the active zone of the sensor, which is modeled by the resistances R on figure 6, and generates a noise voltage V_{out} on the output sensing contact S2:

$$\begin{aligned} V_{out} =& R\frac{I_6}{4} + R\frac{2I_6}{4} - R\frac{I_6}{4} \\ V_{out} =& R\frac{I_6}{2} \end{aligned} \tag{11}$$

In terms of Power Spectral Density (PSD), this reads:

$$< V_{out}^2 >= \frac{1}{4}R^2 < I_6^2 > \tag{12}$$

where $< I_6^2 >$ represents the PSD of the noise current generated in M6, including both thermal and flicker noises, and $< V_{out}^2 >$ the resulting PSD of the output voltage. Following the same reasoning for each transistor of the four output stages, one can show that the PSD of the output voltage due to M1-M8 is given by:

$$\begin{aligned} < V_{out}^2 >= \frac{1}{4}R^2 \Big[& < I_3^2 > + < I_4^2 > + \\ & < I_5^2 > + < I_6^2 > \Big] + \\ \frac{9}{4}R^2 \Big[& < I_1^2 > + < I_2^2 > + \\ & < I_7^2 > + < I_8^2 > \Big] \end{aligned} \tag{13}$$

where $< I_n^2 >$ represents the PSD of the noise current generated in the Mn transistor. Since M1-M8 are biased with a relatively high current, namely a quarter of the Hall effect device biasing current, the PSDs of the noise currents of these transistors are sufficiently large to make M1-M8 the main noise sources of the whole system, assuming the input differential stage of the amplifier to be designed for low-noise as explained in reference [8]. In addition, since all the transistors are biased with the same current intensity, the PSDs of the noise currents of all the NMOSs (resp. PMOSs) are equal. Thus, in the case of a n-strips device biased by a n-output stages circuit, expression (13) can be generalized and the resulting PSD of the output voltage reads:

$$< V_{out}^2 >= R^2 \cdot \big(< I_N^2 > + < I_P^2 > \big) \frac{(n^3 - n)}{12} \tag{14}$$

where $< I_N^2 >$ and $< I_P^2 >$ represent the PSD of the noise current generated in each NMOS and PMOS transistor of the output stages respectively (thermal and flicker noise contributions). It is important to note that in the case of an odd number of strips, the noise current generated by both transistors of the central output stage does not produce any voltage fluctuation on the output sensing contact. Expression (14) has been verified by circuit simulation for $n = 4$ and $n = 5$.

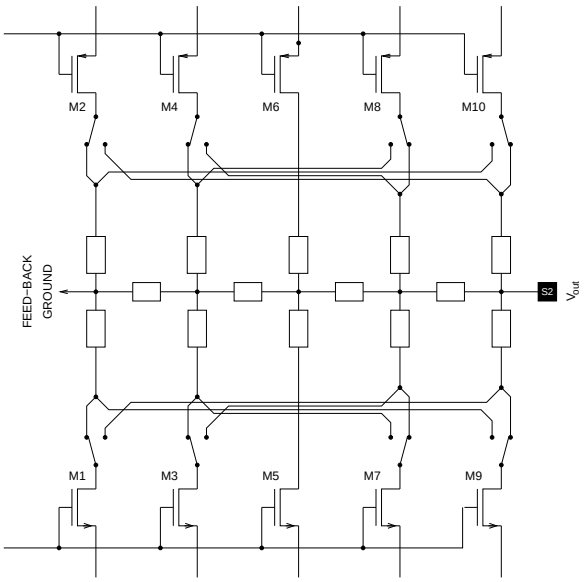

Fig. 7. The chopping technique for the resistive coupling flicker noise modulation

B. Biasing circuit improvement

In order to cancel the flicker noise due to the resistive coupling of the output stages, we propose to use a switching technique based on the same principle as the one used in flicker noise free chopper amplifiers [9]. It consists in modulating the $1/f$ noise generated by the transistors of the output stages by periodically inverting their roles. Such a chopping technique allows to reject the low frequency part of the noise to high frequencies (around the chopping frequency). This technique also rejects the offset induced by the mismatch among the output stages. Using a simple low-pass filter, these extra flicker noise and offset are then removed. The thermal noise due to the resistive coupling (thermal noise contribution in equation (14)) is not affected by this technique and can not be reduced anymore [9]. In order to have a good control on the potential of the fed back sensing contact of the n-strips Hall effect device, even during the switching of the output stages, n must be chosen odd. Moreover, to modulate all the extra $1/f$ noise, the switching of the output stages must be performed symmetrically around this central output stage which does not generate any noise on the output sensing contact. This is schematically described for a five strips Hall effect device on figure 7. The switches that are symbolized on figure 7 are actually realized with differential transistors pairs (NMOSs pairs on the bottom and PMOSs pairs on the top of the schema) as shown on figure 8. The gates of the transistors of these differential pairs are driven by two complementary chopping control signals which are derived from a triangle wave generated by an

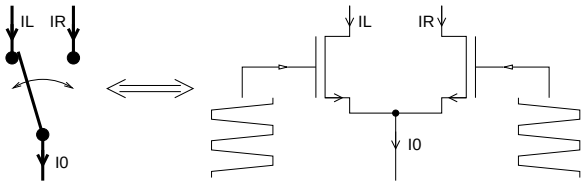

Fig. 8. The actual realization of the switches

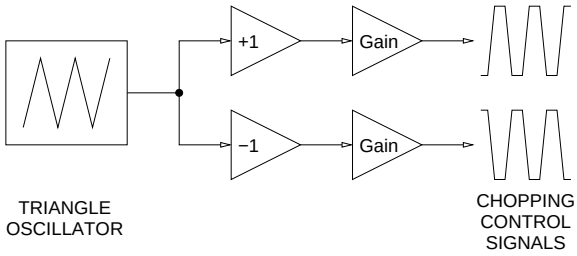

Fig. 9. Generation of the chopping control signals

integrated $45kHz$ oscillator. Taking advantage of the saturation of the amplifiers, this triangle wave is strongly amplified in order to obtain two square shaped waves with smooth transitions between the upper and lower states (figure 9). On one hand, this allows to perform a smooth switching of the output stages and prevents the total biasing current in the device to fluctuate (figure 10). On the other hand, during the switching, all the strips of the device are shorted by the differential pairs and the Hall effect is then annihilated. This reduces the effective sensitivity of the sensor by a switching correction factor which is equal to one minus the switching time to the chopping period ratio.

Finally, the whole microsystem is made up of a five strips Hall effect device biased by an amplifier which implements the chopping technique. This chopper biasing amplifier is controlled by an integrated

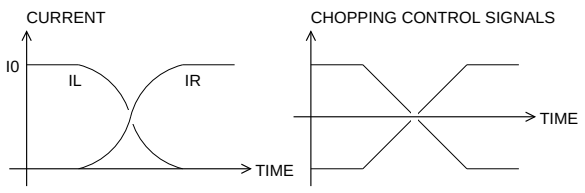

Fig. 10. Smooth switching of the biasing current

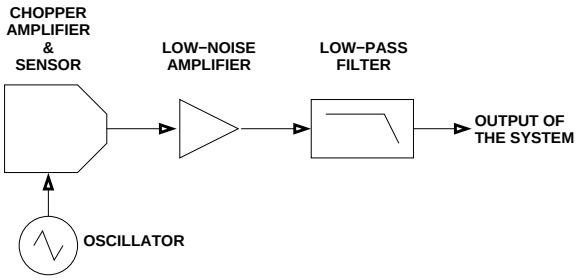

Fig. 11. Block diagram of the whole system

triangle oscillator. The signal on the output sensing contact is amplified and filtered by a fourth order low-pass filter (figure 11). The chopping frequency is chosen high compared to the cut-off frequency of the low-pass filter ($1kHz$) in order to obtain a good attenuation of the modulated $1/f$ noise and offset.

III. Experimental results

A. Prototypes

Two microsystems have been realized using a standard CMOS $0.6\mu m$ integrated circuit technology. The first one uses the simple biasing circuit presented on figure 5 and a four strips Hall effect device ($W = 31.6$, $w = 3.1$, $L = 9.6$, $l = 2.2$ and $S = 3.1\mu m$). The second one is an improved microsystem with a five strips device as described previously ($W = 39$, $w = 3$, $L = 9$, $l = 0.2$ and $S = 3\mu m$). This last microsystem also includes a $45kHz$ oscillator which generates the chopping control signals (figure 11). The two Hall effect devices are made of buried N well with N^{++} ohmic contacts on a P substrate. The square resistance and the thickness (junction depth) of the N well are 1250Ω and $2.5\mu m$ respectively. Both devices are surrounded by a P^{++} guard-ring which prevents parasitic leakage currents to flow under the sensing elements. The so manufactured devices are covered by a silicon oxide and a polysilicon layer similar to a MOSFET gate, forming a MOS junction (figure 12). Connecting this gate to the lowest potential allows to create a depleted zone under the oxide which reduces the effective thickness t of the N well and consequently increases the current related sensitivity $|\frac{V_H}{I \cdot B_z}|$ as much as the square resistance $R_\square$ [8], [10]. Consequently, the maximal absolute sensitivity is not affected by this particular feature which is used to reduce power consumption.

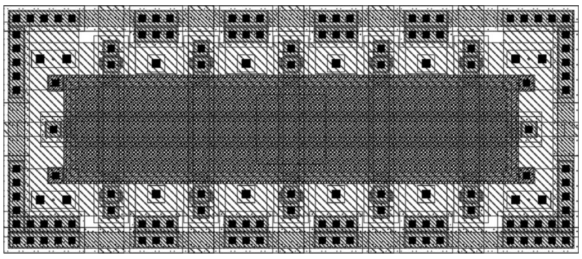

Fig. 12. Layout of the five strips Hall effect sensor ($49.8 \times 21.4 \mu m^2$ including the P^{++} guard-ring, the size of the active area is $39 \times 9.2 \mu m^2$)

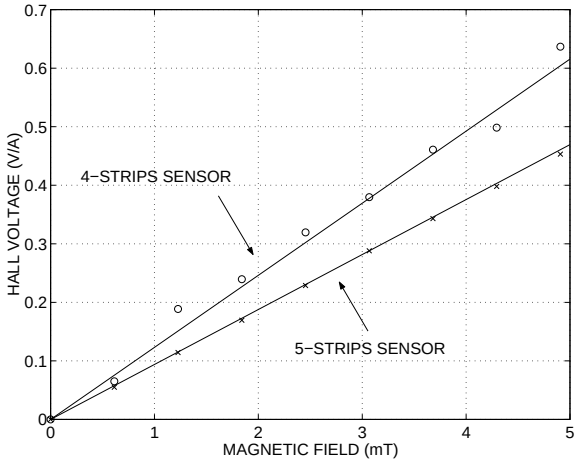

Fig. 13. Compared relative sensitivity of the two sensors

B. Sensitivity

Figure 13 presents the relative sensitivities of both Hall effect devices measured under weak field generated by a set of Helmholtz's coils. The experimental setup is detailed in reference [11]. During the measurements, the four strips and the five strips Hall effect devices were biased by currents of $0.97mA$ and $2.07mA$ respectively and the measured absolute sensitivities were $119mV/T$ and $195mV/T$. The corresponding current related sensitivities are $123V/AT$ and $94V/AT$.

In fact, the value of $94V/AT$ is an effective value which correspond to the current related sensitivity of $117V/AT$ attenuated by a switching correction factor of 0.8 as discussed in section II-B. The small discrepancy between both current related sensitivities ($117V/AT$ and $123V/AT$) can be explained by the batch to batch manufacturing process fluctuations and by the accuracy of the evaluation of the current

which was actually biasing each device during the experiment. For the four strips device the biasing current has been evaluated by circuit simulation, when the biasing current of the five strips device has been precisely measured thanks to a sixth output stage added for this purpose. This sixth output stage is identical to the non-switched central output stage of the biasing amplifier. One external 750Ω resistor was connected between the ground and the drain terminal of the PMOS, while another external 750Ω resistor was connected between the ground and the drain terminal of the NMOS. The resistance has been deduced from equation (8). These resistors emulate one strip and get both transistors into the same biasing conditions as the transistors of the other five output stages. They were also used to evaluate the biasing current of the five strips device by using Ohm's law. Consequently, the value of $117V/AT$ is certainly the more realistic one. In addition, the high noise level (figure 14) of the four strips device based microsystem has strongly affected the accuracy of the measurements made on this microsystem. The great dispersion in these measurements, as observed on figure 13, is directly linked to this high noise level.

The biasing circuit for the five strips sensor was designed to supply $2mA$ into the Hall device. Increasing the current strongly reduces the output resistance of the transistors which no longer behave like good current sources. Nevertheless, the biasing current has been experimentally increased up to $4.56mA$ leading to an absolute sensitivity of $300mV/T$. The voltage drop across the biasing contacts was equal to $1.38V$. In order to keep the transistors of the output stages into saturation, the biasing current cannot be increased any more. Consequently, the value of $300mV/T$ is the maximal absolute sensitivity we can obtain with this microsystem and a $5V$ power supply. However, it is possible to enhance the absolute sensitivity by designing the output stages for supplying a higher current while maintaining a high output resistance.

By comparison, a $50 \times 26\mu m^2$ rectangular Hall effect device designed in the same technology exhibits a current related sensitivity of $111V/AT$. Inserting this rectangular device in the output stage of a conventional operational transconductance amplifier (biasing current of $1.2mA$) allowed to reach an absolute sensitivity of $133mV/T$ [8], while connecting it across the power supply (biasing voltage of $5V$) would achieve a maximal absolute sensitivity of $230mV/T$.

C. Resolution

All noise measurements were performed on a bandwidth of $5Hz$ to $1kHz$ which is usual in contactless AC current measurement for industrial applications [5]. Thus, the resolution of the system is now defined as the square-root of the integral between $5Hz$ and $1kHz$ of the voltage noise PSD at the output of the sensor, divided by its absolute sensitivity. The four strips device based microsystem exhibits a quite

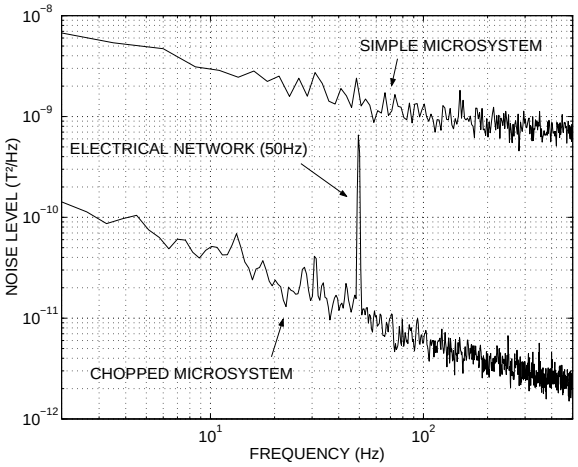

Fig. 14. Compared noise spectrums of the two microsystems

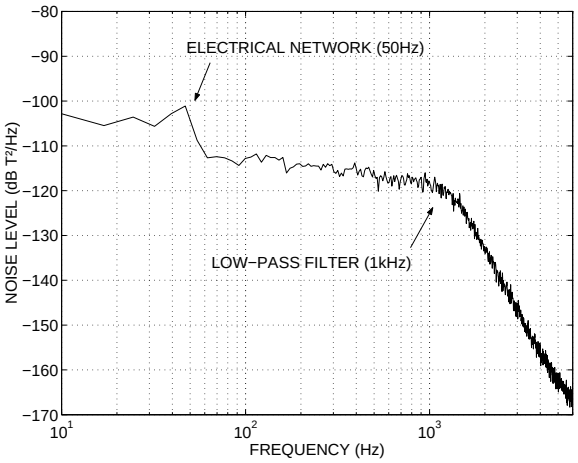

Fig. 15. Noise spectrum of the chopped microsystem

low resolution of about $450\mu T$, which is more than one order of magnitude worse than the resolution of conventional rectangular integrated horizontal Hall effect devices based microsystems realized in CMOS technology [8]. This is due to the resistive coupling between the output stages as explained in the previous section. On the bandwidth of interest, this extra noise is a pure $1/f$ noise as shown on figure 14. The five strips device based microsystem exhibits a better resolution because of the use of the chopping technique in the output stages that totally rejects this extra flicker noise to high frequencies. Thus, the resolution of this last microsystem is only limited by the $1/f$ noise generated by the input differential stage of the

biasing amplifier and by the flicker noise level of the Hall effect device itself, the thermal noise being negligible. In our case the noise comes essentially from the device itself because of its small size. On the bandwidth of interest, a resolution of $32\mu T$ has been reached (figures 14 and 15).

Nevertheless, this resolution can be easily improved by increasing the Hall device dimensions (for flicker noise reduction) and/or the number of strips. Indeed, since a n-strips device is similar to a set of n rectangular Hall devices, the PSD of its voltage noise is n times the PSD of the voltage noise of one elementary rectangular Hall effect device (i.e. of one strip). Moreover, the maximum absolute sensitivity of a n-strips device is also multiplied by a factor n. The signal to noise ratio is then $\sqrt{n}$ times greater than the signal to noise ratio of one elementary device. Consequently any absolute sensitivity can be reached and a high resolution is achievable with such a multiple strips Hall effect device coupled to the presented specific chopper biasing circuit.

Finally, using a flicker noise free chopper biasing circuit, the maximal resolution of a n-strips Hall effect device based microsystem is only limited by the noise of the device itself ($1/f$ noise and thermal noise) and by the thermal noise due to the resistive coupling of the output stages.

IV. Comments and perspectives

The presented experimental results validate the biasing principle for the n-strips Hall device, and show that high absolute sensitivity can be reached. This multiple strips device can be seen as an array of elementary Hall devices as discussed previously. Thus, the n-output stages amplifier designed for our specific n-strips device can also be used to bias an array of any Hall devices. In particular, for accurate DC magnetic field measurement where a low offset is required, an array of symmetrical devices (for instance cross-shaped) associated with a spinning current method in each output stage may be used.

In addition, the presented biasing technique may be very useful when low-voltage technologies have to be used. Indeed, a low voltage power supply limits the maximal absolute sensitivity of Hall effect devices. However, one can take advantage of this biasing technique to compensate the sensitivity loss by increasing the number of strips or the number of devices in the array.

V. Conclusion

A new shape of integrated horizontal Hall effect device has been proposed. The resulting multiple strips device exhibits a lower input resistance than conventional horizontal Hall effect devices while keeping a near unity geometrical correction factor. Since the input resistance directly limits the intensity of the biasing current, this low resistive device presents a higher maximal absolute sensitivity than conventional

rectangular devices. Thus, by increasing as much as needed the number of strips, it is possible to enhance the absolute sensitivity as much as desired. This helps to improve the resolution of the whole microsystem. This particular multiple strips Hall device needs a specific biasing circuit which has been presented first in a simple version and second in an improved one. The simple biasing circuit leads to a high output noise level which deteriorates the signal-to-noise ratio. This extra noise can be strongly attenuated by using a chopping technique in the output stages of the biasing amplifier. With a biasing current of $2.07mA$, the sensor based on a $39 \times 9.2\mu m^2$ five strips Hall effect device exhibits an absolute sensitivity of $195mV/T$ and a resolution of $32\mu T$ on a bandwidth of $5Hz$ to $1kHz$. By modifying the biasing current, the number and/or the size of the strips it is possible to reach any absolute sensitivity and a better resolution.

ACKNOWLEDGEMENTS

We would like to thank the reviewers for the constructive comments they brought during the revision of this work.

REFERENCES

[1] H. BALTES and R. POPOVIĆ, "Integrated semiconductor magnetic field sensors," *Proceedings of the IEEE*, vol. 74, no. 8, pp. 1107–1132, 1986.

[2] R. POPOVIĆ, "A MOS Hall device free from short-circuit effect," *Sensors and Actuators A*, vol. 5, pp. 253–262, 1984.

[3] A. BILOTTI, G. MONREAL, and R. VIG, "Monolithic magnetic Hall sensor using dynamic quadrature offset cancellation," *IEEE Journal of Solid-State Circuits*, vol. 32, no. 6, pp. 829–836, 1997.

[4] L. CHIESI, K. HAROUD, J. FLANAGAN, and R. POPOVIĆ, "Chopping of a weak magnetic field by a saturable magnetic shield," *Sensors and Actuators A*, vol. 60, pp. 5–9, 1997.

[5] V. FRICK, L. HEBRARD, P. POURE, F. ANSTOTZ, and F. BRAUN, "CMOS microsystem for AC current measurement with galvanic isolation," in *Proceedings of IEEEsensors'2002*, (Orlando), pp. 1445–1450, June 2002.

[6] H. BLANCHARD, F. D. MONTMOLLIN, J. HUBIN, and R. POPOVIĆ, "Highly sensitive Hall sensor in CMOS technology," *Sensors and Actuators A*, vol. 82, pp. 144–148, 2000.

[7] *Integrated Systems Engineering (ISE Tcad) manuals*.

[8] V. FRICK, L. HEBRARD, P. POURE, and F. BRAUN, "CMOS microsystem front-end for microtesla resolution magnetic field measurement," in *Proceedings of ICECS'2001*, (Malta), pp. 129–132, September 2001.

[9] C. ENZ and G. TEMES, "Circuits techniques for reducing the effects of the op-amp imperfections: autozeroing, correlated double sampling, and chopper stabilization," *Proceedings of the IEEE*, vol. 84, no. 11, pp. 1584–1614, 1996.

[10] J.-B. KAMMERER, L. HEBRARD, V. FRICK, P. POURE, and F. BRAUN, "Design and modelling of a voltage controlled N-well resistor using the MOS tunneling diode structure," in *Proceedings of ICECS'2002*, (Dubrovnik), pp. 1123–1126, September 2002.

[11] V. FRICK, L. HEBRARD, P. POURE, and F. BRAUN, "Design, characterisation, modelling and performances of magnetic sensors in standard CMOS technology," in *Proceedings of DCIS'2000*, (Montpellier - France), pp. 700–704, November 2000.