# Influence of cell edges on the performance of silicon heterojunction solar cells

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## Abstract

Full size silicon heterojunction solar cells reach conversion efficiencies above 25%. However, photoluminescence pictures of such cells (full or cut) reveal a significant recombination activity at the cell edges. Therefore, mitigating recombination at the edges can in principle represent an interesting path to unlock higher cell efficiencies. This challenge is all the more important for cells with a high perimeter/area ratio, as achieved through the cutting of full size cells. For such technologies, the edges resulting from cutting are cleaved while the remaining edges typically feature a gap where TCO is missing to avoid front to back short-circuit. In this paper, we specify the physical mechanisms involved in the edge-induced performance losses for SHJ cells. In light of these results, we provide guidelines for the mitigation of such losses at the full-size and cut cells scale for M6 to M12 sizes such as the reduction of the TCO-free region and the c-Si bulk resistivity. Having a closer look at cut cells, we calculate the cell performance as a function of its size (from half- to sixth-cell), the size of its mother cell (from M6 to M12) and the passivation quality of the cut-edges. Our results emphasize on the interest to develop suitable repassivation schemes for cut cells to improve or even surpass the efficiency of the mother cell.

## A. Introduction

In a context where silicon heterojunction solar cells (SHJ) are regularly improved in production [1], spatial heterogeneities in the surface passivation may increasingly limit the cell efficiency on the way towards 25%-26% predicted in 2030 [2]. Furthermore, the international roadmap for photovoltaics market [2] predicts a rapid switch of the overall industry to cut-cell formats (1/2 cells to 1/6 cells). Because such cells are obtained through the cutting of full size cells (mother cells) into smaller cells, their perimeter-to-surface ratio is significantly increased. The edge recombination-induced performance losses are expected to increase as the cutting process leaves unpassivated *c*-Si borders. The optimisation of such cells therefore becomes a crucial challenge for the future and the photovoltaics community is currently investigating edge repassivation processes [3][4]. Furthermore, since cut-cells feature both cut edges and native edges inherited from the mother full-size cell, the optimisation of the native edges should also be addressed.

While the study of edge recombination-induced performance losses for silicon homojunction cells has been broadly addressed in the literature [5][6][7], the study of such effects for silicon heterojunction cells is still incomplete. To investigate the impact of edges in SHJ full size and cut-cell edges, we have developed a simulation code for SILVACO [8], already presented and validated in [9] .

The work will first focus on the study of the native edges inherited from the mother cell. To this aim, simulations of full-size cells, for which all edges are native edges, will be run to study the room for improvement related to the optimisation of such edges. These simulations will be used to conduct a parametric study on the influence of the native edges properties on the efficiency of SHJ cells. In particular, we will address the influence of the edge geometry, the edge defect density and the *c*-Si bulk properties on the edge-induced losses. The observed behaviours will be explained on the basis of the calculated spatial variations in the minority carriers quasi-Fermi level, which was shown to be a powerful mean of investigation in a previous paper [10].

In a second part, we will transpose the investigation to cut-cells of different industry-relevant formats. Cut-cells will be simulated with the native edges passivation that best describes their behaviour for CEA-INES cells, as determined in a previous study [9]. In particular, we will use the simulations to predict the cutting-induced performance losses and the achievable recovery with the repassivation of cut edges. In light of the results, we will eventually propose guidelines for the mitigation of the edge losses on cut cells.

## B. Simulation and experimental details

The rear-junction cells studied in this paper were fabricated at CEA-INES on 1Ω.cm and 160µm thick texturized (n) *c*-Si wafers. Further details on cell fabrication can be found in [11]. Hydrogenated amorphous silicon (*a*-Si:H) layers were deposited by PECVD on both front and rear *c*-Si surfaces leading to a rear junction structure. The passivated wafer was then sandwiched between front and rear Transparent Conductive Oxide (TCO) layers simultaneously deposited by Physical Vapour Deposition (PVD). During the PVD step, the cell precursors lay on open pockets on the PVD tray. As a result, the perimeter of the cell rear side is in contact with the tray, and is thereby screened during PVD deposition, leading to the absence of TCO along the cell edge on its rear surface, on a width (*L*) that depends on the tray design (Fig 1b). The metallic grid is then printed on both front and rear surfaces in a busbarless pattern. Such pattern was chosen in order to provide an additional symmetry level to the cell, thereby easing the simulation structure definition.

The 2D simulations presented in this paper were performed using the ALTAS package from the finite elements TCAD software SILVACO. Note that finite elements softwares feature structural limitations, so that the simulation of real size *c*-Si based solar devices is generally not feasible. As presented in a previous paper of our group [9] and in a similar way by A. Fell et al. [7], this problem can be overcome by combining the simulation results obtained for a few well-defined unit cells. Here, we have chosen to divide the cell simulation into a core cell, representing the edge-unaffected central part of the cell, combined with one or more edge cells, representing the different types of edges that can be met in practice in a cut cell (Fig.1). The unit cells were modeled according to the standard cell process at CEA as per 2020 referred as to "practical cells" in the following:

- Fig.1a: Edge with a full rear side TCO covering. Such configuration will be called the "covered edge" unit cell.
- Fig. 1b: Edge with a TCO-free region along the perimeter of the backside, due to the above-mentioned edge masking during TCO deposition (referred to as the "TCO-free edge" unit cell). This TCO-free region is necessary to avoid electrical shunt between the front side and rear side TCO layers. Therefore, the native edges of full-size cells currently produced at CEA-INES are TCO-free. In the following, the TCO-free region will be set to 1mm

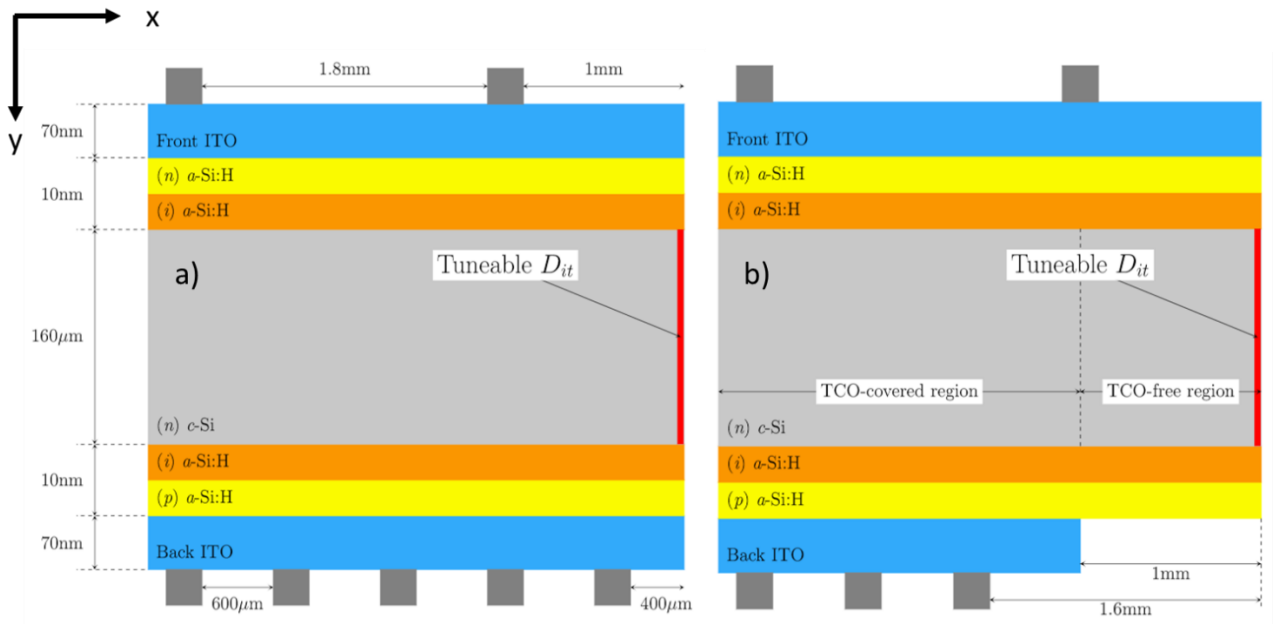


*Figure 1: Schematic of the two studied edge structures: with a TCO full coverage at the rear side (left, "covered edge") and with a rear side TCO gap at the edge (right, "TCO-free edge"). Edge defects are implemented as a variable $D_{it}$.*

For both TCO-covered and TCO-free edges, the edge recombinations were modelled by a midgap interfacial defect density ($D_{it}$). The metallization grid features a 1.8mm pitch on the front side and 0.6mm on the rear side. The distance between the last rear side metallization finger and the cell edge was set to 1.6 mm. For TCO-covered edges, the last finger on the rear side is located at 0.4mm from the edge. Consequently, the distance between the

last metallization finger and the edge of the TCO layer is not the same for TCO-free and TCO-covered edges. Further simulation studies showed that the influence of the length between the last metallization finger and the edge of the TCO on the edge-induced losses are marginal (between the performances of A) a M10 cell with a 400µm gap between the last metallization finger and the TCO edge and B) an other with a 600µm gap the $\eta$ relative variations $100\times\frac{\eta A-\eta B}{\eta A}$ are around 0.1%$_{rel}$). This will therefore not be discussed in this paper. Furthermore, each individual layer was implemented in simulations with properties obtained from characterizations carried out on CEA cells: band gap, optical coefficients, doping atom concentration, etc.

## C. Understanding of the physical mechanisms involved in the edge-induced losses.

The edge recombinations are mainly modulated by the edge $D_{it}$ and the presence or absence of the TCO-free region. We will firstly isolate the effects of the TCO-free region by comparing TCO-free and TCO-covered edges with a "perfect" edge passivation (edge $D_{it}$=0 cm$^{-2}$). We will then insist on the effects of the edge recombinations by studying a totally depassivated edge ($D_{it}$=10$^{14}$cm$^{-2}$).

### 1. Effects of the TCO-free region

Simulations were run for M6 (274cm²) cells without any edge recombination in order to isolate the effects of the TCO-free region on the cell performances. Fig. 2 represents the simulated *I*(*V*) characteristics (Standard Test Conditions) for TCO-free and TCO-covered edges. In order to better describe the variations between these *I*(*V*) curves, the current density relative variations between them is also shown.

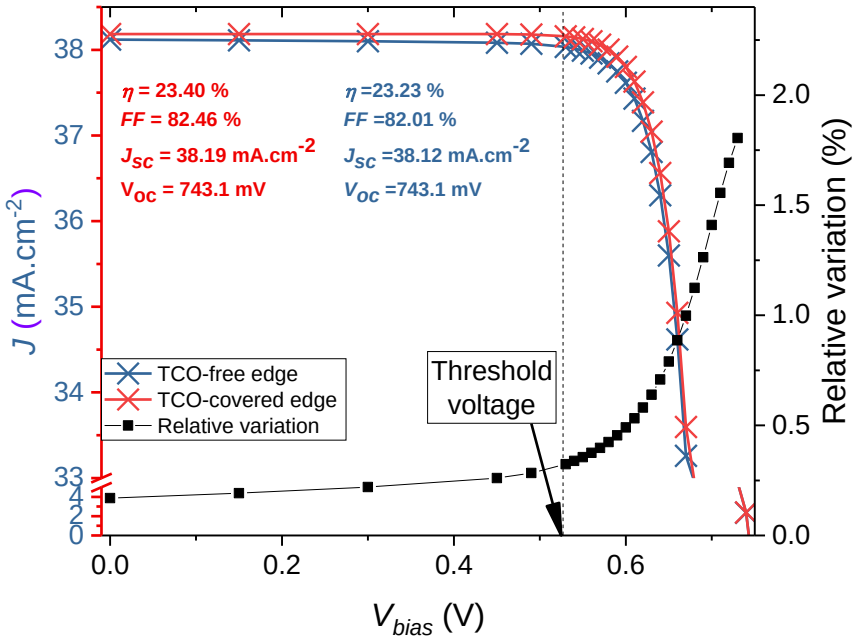


*Figure 2: Simulated I(V) curves for M6 full size cells with rear TCO-free edges (blue) or rear TCO-covered edges (red) with edge $D_{it}$=0cm$^{-2}$. The I(V) parameters of each cells are given with the same colour code. The relative variation between the two curves is plotted in black.*

First of all, it might be noticed that the gap between the two simulated *I*(*V*) curves and the corresponding efficiencies ($\eta$) is very low (23.40% vs 23.23% respectively for cells with TCO-covered and TCO-free edges). This highlights that on a full cell with perfectly passivated edges, the TCO-free region has a detrimental, yet moderate, effect on $\eta$.

Secondly, note that the current density relative variations (black curve) can be divided into two distinct regions before and after the bias voltage $V_{bias}$≈0.5V. While the low $V_{bias}$ region features linear modest variations of the losses induced by the TCO-free region, the high $V_{bias}$ region shows a fast increase of the relative losses. As

a result, the TCO-free region impact on $\eta$ is mainly driven by Fill Factor (*FF)* losses (about 3/4 of the losses) and then by short circuit current ($J_{sc}$) losses (about 1/4 of the losses).

Since the gradient of the hole quasi-Fermi level ($\varepsilon_{F,h}$) describes the force applied to the holes, maps of $\varepsilon_{F,h}$ were extracted from simulations in order to understand the physical mechanisms involved in the performance losses in the presence of the TCO-free region. $\varepsilon_{F,h}$ along the *x* axis (see Fig.1 for position) were extracted at the mid-depth of the cell (Fig.3). Note that $\varepsilon_{F,h}$ is defined as the absolute variation from its value at equilibrium. To make sure that this mid-depth profile is representative, it was beforehand compared to the same profiles extracted in the *c*-Si near the front and the rear *c*-Si surfaces, which revealed the same behaviours.

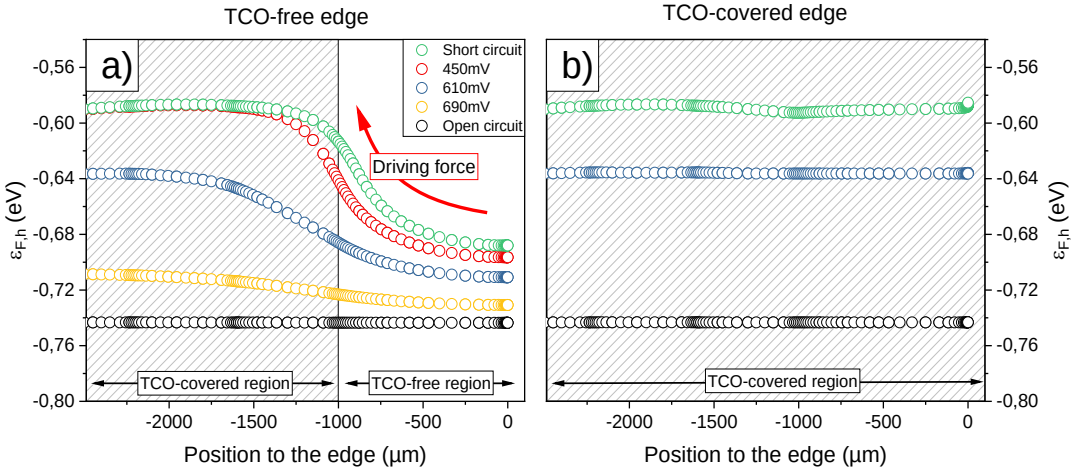


*Figure 3: Spatial variation of $\varepsilon_{F,h}$ along the horizontal axis, at the mid-depth of the cell without defects at the edge ($D_{it}$ = 0 cm$^{-2}$) for TCO-free (a) and TCO-covered edges (b). Different working voltages are studied and the driving force applied to the holes is represented as a red arrow.*

Fig.3 shows the $\varepsilon_{F,h}$ and thus the driving force variations along the horizontal axis for several voltages with (a) and without (b) the TCO-free region, and without any edge defects ($D_{it}$=0 cm$^{-2}$). An important $\varepsilon_{F,h}$ drop can be observed with the TCO-free region, which leads to a driving force directed towards the TCO-covered region. This force is decreasing from the short circuit to the open circuit condition, and the differences between the TCO-free and TCO-covered edge profiles progressively vanish for increasing $V_{bias}$.

The explanation lies in spatial heterogeneities in the holes extraction at the junction. Holes are indeed homogeneously photogenerated along the horizontal axis, but they can be efficiently extracted only where the TCO covers the cell rear side. Consequently, holes can accumulate in the TCO-free region which is illustrated by a low $\varepsilon_{F,h}$ value (Fig.3a). The holes photogenerated in the region with a rear TCO covering can be collected, leading to a higher $\varepsilon_{F,h}$ value in this region. This leads to the establishment of a $\varepsilon_{F,h}$ gradient and thus to a driving force directed from the TCO-free region to the TCO-covered region.

Upon increasing $V_{bias}$, since the current collection is decreased, the injection level in the TCO-covered region increases leading to a reduction of $\varepsilon_{F,h}$ while $\varepsilon_{F,h}$ in the TCO-free region is almost not impacted (there is still no collection in this region). Consequently, the gap between the $\varepsilon_{F,h}$ values in the TCO-free and the TCO-covered region is reduced for increasing $V_{bias}$ and the driving force vanishes. At the open circuit condition, since there is no carrier extraction, the TCO-free and TCO covered edges $\varepsilon_{F,h}$ profiles plotted Fig.3.a and Fig.3.b are the same with no driving force induced by the TCO-free region. This explains the shape of the relative current black curve in Fig.2. The higher $V_{bias}$, the lower the driving force and thus the higher the current losses. Consequently, at the short circuit working point the current losses are weak and they progressively increase for increasing $V_{bias}$.

Above the threshold voltage $V_{bias}$ > 0.5V the sharp increase in the current density relative losses can be explained by the less efficient hole harvesting at the junction, leading to a strong increase in hole concentration in the TCO-covered part of the cell. Consequently, for such $V_{bias}$, as can be seen in Fig,3, the hole driving force in the TCO-free region is weakened, leading to a less effective carrier extraction, and thus an increase in collected current relative losses. Furthermore, in Fig.3.a, the abscissa where $\varepsilon_{F,h}$ gradient is shown to spread along the x axis for increasing $V_{bias}$. This illustrates the lengthening of holes in the *c*-Si.

At the open circuit condition, since there is no carrier extraction, the presence of the TCO-free region has no effect on the carrier motions in the c-Si. The holes have therefore the same recombination path whether the cell edge features a TCO-free region or not, so that there is no overall impact of the edge geometry on $V_{oc}$.

## 2. Addition of the edge $D_{it}$

To probe the effect of $D_{it}$ on the edge losses, simulations with edge $D_{it}$ varying from 0 $cm^{-2}$ (perfectly passivated edge) to $10^{14}$ $cm^{-2}$ (totally depassivated edge) were run. The $I(V)$ parameters simulated for full size M6 cells with TCO-free and TCO-covered edges are plotted in Fig.4.

First of all, the impact of the edge passivation can be divided into three regimes. For $D_{it}<10^{9}cm^{-2}$, the edge defects have only minor effects on the cell performances; for $D_{it} \in [10^{9}; 10^{12}]$ $cm^{-2}$, substantial cell $\eta$ variations are observed; and for $D_{it}>10^{12}cm^{-2}$, the losses are the strongest but with only little dependence on the $D_{it}$ value. From that, we conclude that the native edge passivation quality of bare silicon edges should be efficient enough to reduce by a factor of at least 100 the edge $D_{it}$, in order to increase the cell performance in a detectable way compared to the bare edge case. Furthermore, if we assume a realistic $D_{it}$ value of $3\times10^{10}cm^{-2}$ ( which describes native edges [9]), even a slight improvement in edge passivation quality could provide a significant $\eta$ bonus.

A closer look at $\eta$ variations in Fig.4 brings some dissimilarities between the performances of cells with TCO-covered and TCO-free edges. In the absence of edge defects, the cell with a TCO-covered edge allows for a $0.17\%_{abs}$ higher $\eta$ than with a TCO-free edge, in agreement with Section C.1). Remarkably, with a realistic passivation quality ($D_{it}=3\times10^{10}cm^{-2}$), simulations predict that the suppression of the TCO-free region could allow a $0.22\%_{abs}$ $\eta$ increase. In addition, still for $D_{it}=3\times10^{10}cm^{-2}$, the $\eta$ with TCO-free edges shows a gradual increase by $0.11\%_{abs}$ from the totally depassivated edge condition, which reveals already a clear benefit from the current native passivation [9]. Fig. 4 also reveals that the upmost $\eta$ gain that can be expected from further edge passivation is limited to +0.16%abs. Thus, the reduction of the TCO-free region has in absolute a larger $\eta$ gain potential for the simulated practical cells than the improvement of the edge passivation quality ($\eta$ gain = $0.22\%_{abs}$ vs $0.16\%_{abs}$ respectively). Overall, the reduction of both the TCO-free region and the edge $D_{it}$ could increase $\eta$ of the simulated practical cells by $0.33\%_{abs}$ in the most optimistic case.

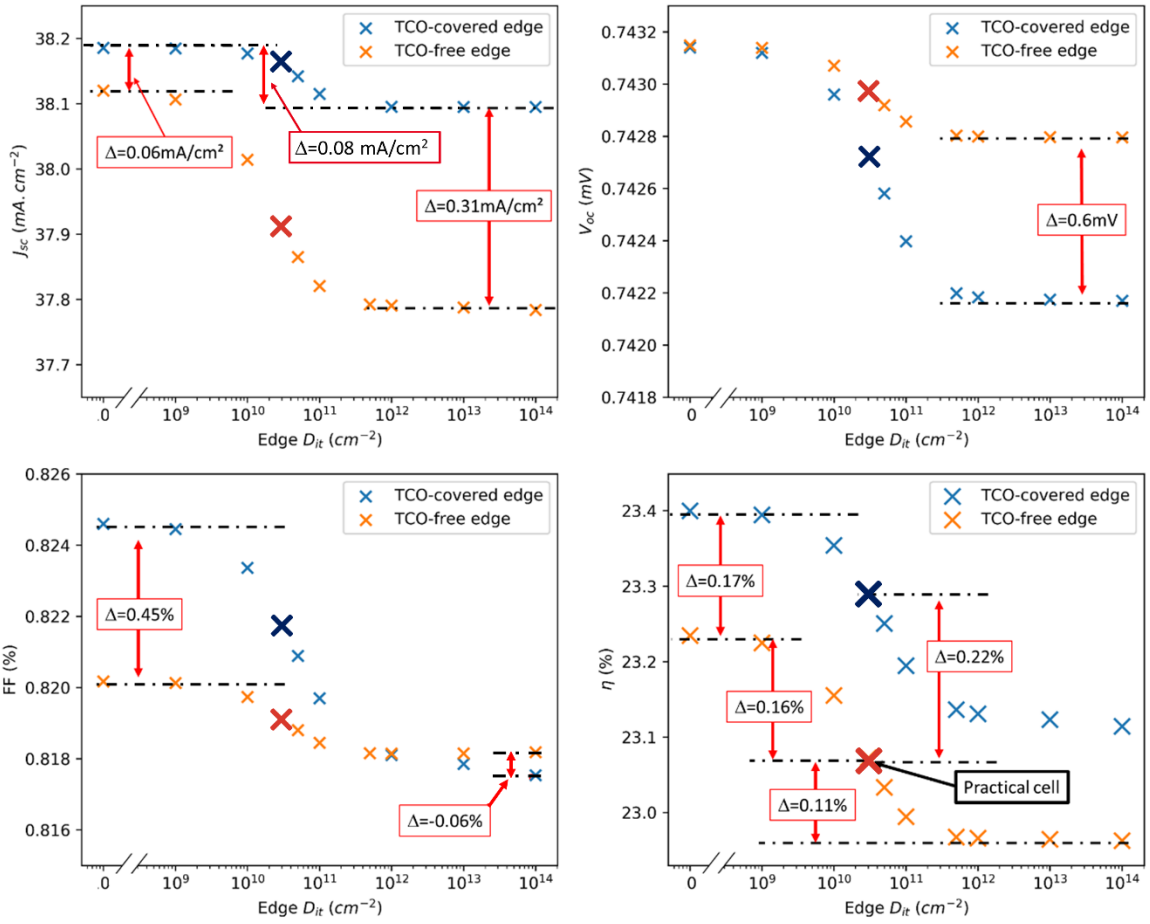


*Figure 4: Simulated I(V) parameters variations as a function of the implemented edge $D_{it}$ for M6 full size cells with TCO-free edges(orange) and TCO-covered edges (blue). The performances of the actual cells appear as bigger bold stars.*

Let us now describe the influence of the edge $D_{it}$ on the other $I(V)$ parameters for TCO-free and TCO-covered edges. $J_{sc}$ is shown to be particularly heavily degraded when edge recombination intensifies and the gap between TCO-covered and TCO-free edges is enlarged for increasing $D_{it}$ (from 0.06mA.cm$^{-2}$ to 0.31mA.cm$^{-2}$). Contrary to the short circuit operating point, at the maximum power point, the TCO-free region seems to mitigate the losses related to edge recombination. Despite the large advantage of the TCO-covered edge at $D_{it}$=0 cm$^{-2}$ (0.45%$_{abs}$), at $D_{it}$=$10^{14}$cm$^{-2}$ the *FF* of the cell with TCO-free edges is 0.06%$_{abs}$ higher than that of the cell with TCO-covered edges. From $D_{it}$=0cm$^{-2}$ to $D_{it}$=$10^{14}$cm$^{-2}$, the edge-induced *FF* losses for TCO-free edge cells are estimated to 0.2%$_{abs}$ versus 0.7%$_{abs}$ for TCO-covered edges.

Concerning the $V_{oc}$ variations, moderate $D_{it}$-induced losses can be observed. At the open circuit operating point, the TCO-free region does not affect the carriers motion inside the cell at $D_{it}$=0cm$^{-2}$ (Fig.3) . However, the simulations suggest a slight mitigation of the $V_{oc}$ losses induced by $D_{it}$=$10^{14}$cm$^{-2}$ for the TCO-free edge compared to the TCO-covered edge (+0.6mV).

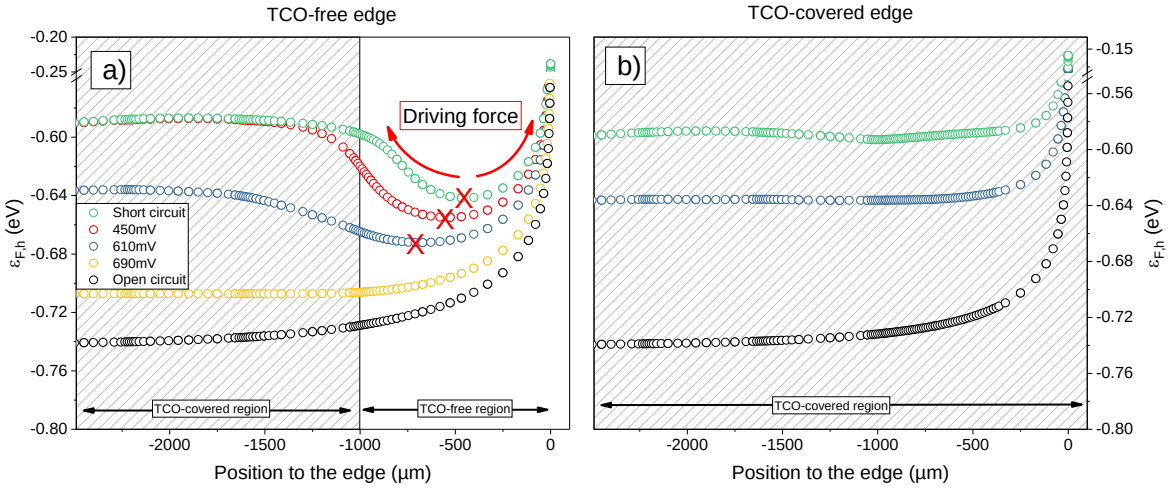


*Figure 5: Spatial variation of $\varepsilon_{F,h}$ along the horizontal axis, at the mid-depth of the cell with defects at the edge ($D_{it}$ = $10^{14}$ cm$^{-2}$) for TCO-free (a) and TCO-covered edges (b). Different working voltages are studied and the driving force applied to the holes is represented as a red arrow.*

In order to understand the variation of individual $I(V)$ parameters for increasing $D_{it}$, the same $\varepsilon_{F,h}$ profiles as those plotted in Fig.3 were extracted from simulations with edge $D_{it}$ = $10^{14}$cm$^{-2}$ (Fig. 5). Holes recombine at the edges in the presence of defects, and their concentration close to the cell edge dramatically drops. This leads to an increase in $\varepsilon_{F,h}$ in the edge vicinity. The driving forces applied to the holes are therefore modified compared to the $D_{it}$=0cm$^{-2}$ case (see Fig 3.). As shown in Fig. 5a, a tip over point can be defined for both TCO-free and TCO-covered edges. This point represents the threshold distance to the edge from which the holes are rather attracted by the edge than by the core of the cell. The differences between Fig.5 a) and b) lies in the driving force induced by the TCO-free region. Indeed, for TCO-covered edges the holes experience at any distance from the edge, a vertical driving force directed towards the junction that partially counterbalance the horizontal component of the overall driving force depicted in Fig. 5. On the contrary, for TCO-free edges, as the tip over point is located in the TCO-free region, there is no additional vertical driving force.

The driving force directed toward the junction must be considered to understand the combined effects of the TCO-free region and the edge passivation quality on the cell performances. First, for the TCO-covered edge, the average $\varepsilon_{F,h}$ gradient directed towards the junction was extracted from the simulations allowing the quantification of the associated driving force for all bias voltages.

Then, the first spatial derivation of the curves plotted in Fig.5 gave the driving force directed towards the edge defects. The comparison between these two driving forces allows to predict if a hole photogenerated at a given distance from the cell edge is eventually recombined at the edge defects or collected at the cell junction.

At the short circuit working point, this analysis revealed that, in the case of TCO-covered edges, the junction-induced driving force is very strong [10] and counterbalances by far the force directed towards the edge defects for holes photogenerated at a distance greater than 100µm from the edge. Thus, only the holes photogenerated within the first 100µm from the edge are lost. For TCO-free edges, since there is no driving force towards the junction at the tip over point (500µm from the edge, so still well into the TCO-free area), all the

carriers photogenerated within the first 500µm from the edge are lost. The edge losses are therefore multiplied by a factor of five from the TCO-covered to the TCO-free configurations. This is consistent with the results plotted in Fig.4 where, for $D_{it}$=$10^{14}$cm$^{-2}$ the recombination-induced $J_{sc}$ drop equals 0.06 mA.cm$^{-2}$ for the TCO-covered edge and 0.31 mA.cm$^{-2}$ for the TCO-free edge.

At the open circuit operating point, the TCO-free region alone (with $D_{it}$=0cm$^{-2}$) does not affect the carriers flow inside the cell (black curve in Fig.3). For increasing $D_{it}$, $V_{oc}$ drops for both structures, but the drop is lower for TCO-free edges. The hypothesis which explains this slight trend, relies on the electrical potential distribution at the rear side of the cell in the vicinity of the edge. For TCO-covered edges, the electrical potential of the rear side of the cell is constant (under the hypothesis of a highly conductive TCO) up to the cell edge. On the contrary, for TCO-free edges, since no conductor (metal or TCO in our case) links the TCO-free region to the metallization grid, the electrical potential of the cell rear side in the TCO-free region is floating. When the edge $D_{it}$ is very high, the induced recombinations tend to reduce the excess carrier concentration and consequently, to lower the local voltage at the cell terminals. This has no additional effects on the carrier spatial distribution in TCO-free edges, since the potential at the rear side of the TCO-free region is floating. On the contrary, in the *c*-Si, an additional hole current density directed towards the cell edge is created for TCO-covered edges in order to counterbalance the unauthorized voltage drop. Consequently, the number of carriers lost through recombination at the edge in open circuit condition is slightly larger for TCO-covered edges.

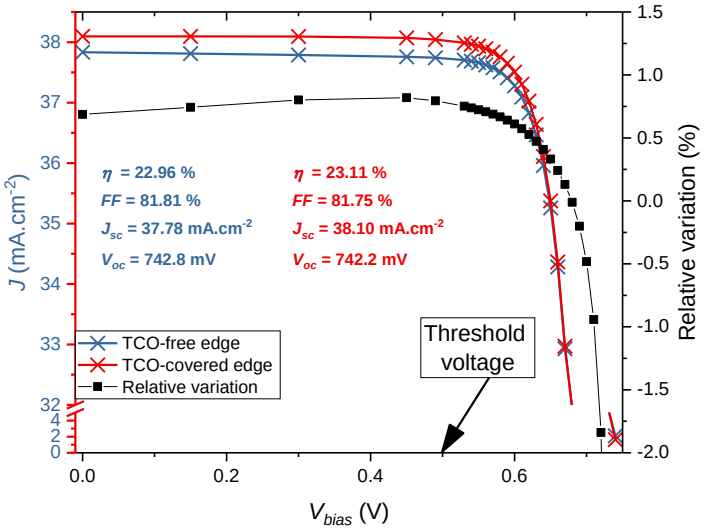


*Figure 6:1 Simulated I(V) curves for M6 full size cells with only rear TCO-free edges (blue) or rear TCO-covered edges (red) with edge $D_{it}$=$10^{14}$cm$^{-2}$. The I(V) parameters of each cells are given with the same colour code as that of the I(V) curves. The relative variation between the two curves is plotted in black.*

Finally, to explain the trend on *FF* (Fig 4.): around the maximum power operating point, the junction-induced (vertical) driving force is much smaller than that at the short circuit operating point, as demonstrated in [10]. Consequently, for both structures, more current is lost at the maximum power point than at $J_{sc}$, explaining the $D_{it}$-induced FF drop.

To understand why the FF drops faster for TCO-covered edges than for TCO-free edges, the $I(V)$ curves of full-size cells with TCO-free and TCO-covered edges and with edge $D_{it}$=$10^{14}$cm$^{-2}$ are plotted in Fig. 6. The relative variation between these two curves is also plotted.

We first note that the relative current variation is almost constant for $V_{bias}$ between 0V and 0.5V, and then drops. For $V_{bias}$>0.68V, the current density is higher for the cell with the TCO-free edge. However, at the maximum power point (around 0.65V) the TCO-free edge is still detrimental to the collected current. Despite this effect, the FF achieved with TCO-free edges is higher than that with TCO-covered edges. This can be explained by the fact that the recombination-induced losses increase faster with $V_{bias}$ for TCO-covered edges. Indeed, from Fig.5a, we observe a shift of the tip over point from 500 to 700µm from the edge going from $V_{bias}$=0V to $V_{bias}$=610mV. The collected current losses are therefore increased by a factor of 700/500=1.4. For the TCO-covered edge, the tilt at the short circuit condition was shown to be at 100µm from the edge. At the maximum power point, the calculation of the $\varepsilon F,h$ gradients in the vicinity of the cell edge allowed to determine that the tip over point is located at

x≈650µm from the edge. The edge recombination-induced current losses are therefore enhanced by a factor of 650/100=6.5 going from $V_{bias}$=0V to $V_{bias}$=0.61V for TCO-covered edges.

To sum up, the stronger FF loss for the TCO-covered edge structure originates from the stronger current loss between $J_{sc}$ and MPP. In the case of TCO-free edges, a significant part of the current was already lost at $J_{sc}$, which is not the case for TCO-covered edges.

## D. Guidelines for the mitigation of edge losses

We intend now to propose guidelines to optimize the design of SHJ cells in order to reduce the performance losses due to edges defects.

### 1. Effects of the c-Si bulk resistivity on the edge losses

In a previous study [10] it was shown that the impact of process-induced localized surface defects ("defectivity") in SHJ cells is a strong function of the substrate resistivity. Furthermore, the TCO-free region at the cell edge increases the collection path for the holes. It is therefore reasonable to expect a significant influence of the conduction properties of the c-Si on the amplitude of the edge effects.

In order to address this point, simulations were run for several resistivity values from 0.4 to 5 Ω.cm chosen within the range of values currently used in industry. For each resistivity value, the hole capture time constant $\tau_{p0}$ was set to 7ms. Given that $\tau_{p0}= (N\times\sigma_h\times v_{th})^{-1}$, where $N$ is the bulk defects concentration, $\sigma_h$ is their capture cross section and $v_{th}$ is the thermal velocity, this parameter therefore represents the purity level of the *c*-Si which was set to the same value for all simulations.

In Fig.7 are plotted the simulated $\eta$ of M6 cells with TCO-free or TCO-covered edges for several resistivities and implemented edge $D_{it}$. Three different $D_{it}$ values were chosen: a perfect edge passivation ($D_{it}$=0cm$^{-2}$), a passivation quality representative of practical cells ($D_{it}$=3×10$^{10}$cm$^{-2}$), and bare silicon edges ($D_{it}$=10$^{14}$cm$^{-2}$). For the sake of clarity, the bulk lifetimes ($\tau_{bulk}$) resulting from intrinsic (radiative & Auger) and bulk Shockley-Read-Hall (SRH) defect recombinations are also given.

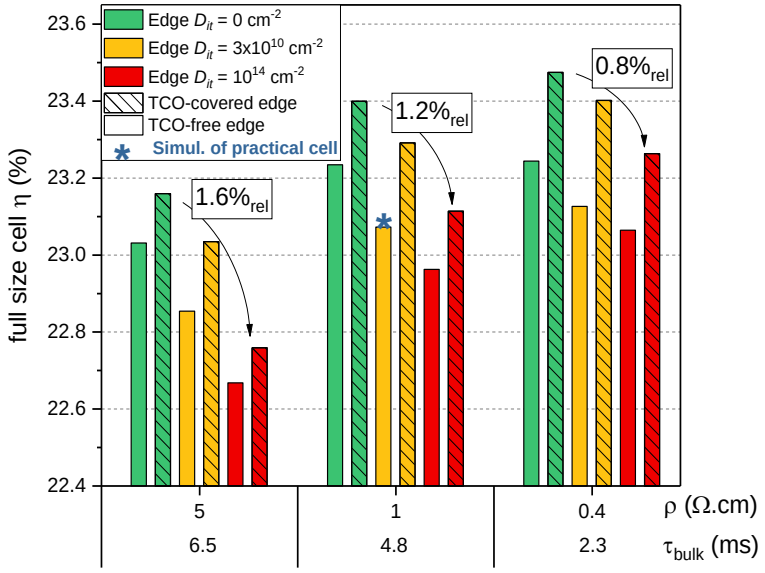


*Figure 7: Simulated efficiencies of full size M6 cells with masked TCO or covered edges at a given $\tau_{p0}$ for several resistivities and edge $D_{it}$. $\tau_{bulk}$ were calculated @ $\Delta p=5\times10^{14}$cm$^{-3}$. The efficiency simulated for practical cells is represented as a blue star.*

From Fig.7 it is apparent that decreasing $\rho$ is modulating edge effects. In particular, it leads to an increase in the gap between the performances of cells with TCO-free and TCO-covered edges, making the reduction of the TCO-free region an even more interesting lever for the optimisation of the cell performance. Furthermore, it can be seen in Fig.7, that the $\rho$ decrease is beneficial for two reasons:

- The rise of the cell $\eta$ without edge defect (+0.2%$_{abs}$ observed between ρ=5Ω.cm and 0.4Ω.cm). These results are consistent with findings in [12]
- The mitigation of edge defect-induced losses: they are reduced by 50% between ρ=5Ω.cm and 0.4Ω.cm (from 1.6% rel. down to 0.8% rel.)

For practical cells ($\rho$ =1 Ω.cm, $D_{it}$=3×10$^{10}$cm$^{-2}$) with TCO-free edges, the reduction of $\rho$ from 1Ω.cm to 0.4Ω.cm could allow a 0.05%$_{abs}$ $\eta$ increase. If this is combined with the suppression of the TCO-free region, $\eta$ could be increased by 0.33%$_{abs}$ which is much better than the improvement predicted after a "perfect" repassivation of the native edge (0.16%$_{abs}$ $\eta$ increase). Furthermore, in addition to mitigate the influence of any process-induced defectivity [10], reducing the resistivity also bears the potential to significantly alleviate the influence of edge defects which is an additional beneficial effect allowing the improvements of the mother full-size cell performances.

Let us focus now on the understanding of the physical mechanisms behind the behaviours observed in Fig.7. The reduction of $\rho$ at a given $\tau_{p0}$ goes hand-in-hand with a $L_{diff}$ lowering. It can be calculated that $L_{diff}$ halves going from 5Ω.cm to 0.4Ω.cm, irrespective of the cell operating point. Consequently, the losses induced by the lengthening of the path for the holes in the presence of the TCO-free region are increased for decreasing $\rho$. This results in the widening of the gap between the two cases TCO-free and TCO-covered edges for decreasing $\rho$ (green bars in Fig. 7). However, as presented in [10], at a given bias voltage the junction-induced driving force is increased for decreasing $\rho$. The carrier extraction in the TCO-covered region is therefore improved at a given bias voltage. In the same way, the driving force resulting from the TCO-free region increases too for decreasing $\rho$ at a given $V_{bias}$ since the $\varepsilon_{F,h}$ in the TCO-covered region is increased. In presence of edge $D_{it}$=10$^{14}$cm$^{-2}$, this strengthening of the driving force induced by the TCO-free region allows to mitigate the edge-induced losses.
As a conclusion, since the resistivity reduction allows to increase the core cell $\eta$ and to mitigate the $\eta$ losses induced by a total edge-depassivation, it represents an efficient lever for the mitigation of the detrimental effect of edge recombination.

## 2. Practical guidelines for edge repassivation experiments

Until now, we referred to edge recombination using the quantity $D_{it}$. However, this quantity is not readily accessible in practical developments. We have therefore investigated the amplitude of edge recombination losses as a function of physical quantities routinely measured for the characterization of passivation layers. The photovoltaics research community often relies on either implied $V_{oc}$ ($iV_{oc}$) or effective surface recombination velocity ($S_{eff}$) values. Such values are usually calculated from PhotoConductance Decay measurements (PCD) [13] carried out on symmetrically passivated samples. Furthermore, since $iV_{oc}$ strongly depends on the c-Si bulk properties ($\tau_{bulk}$, $\rho$ and thickness) and $S_{eff}$ only depends at the first order on the bulk $\rho$, the latter allows to provide more universal guidelines. However, as $iV_{oc}$ is easier to quantify directly from PCD measurements, the correspondence between implemented $D_{it}$ and $iV_{oc}$ will be given here for a specific yet standard set of wafer properties ($\tau_{bulk}$, $\rho$ and thickness) that can be sourced from wafer providers.
In order to correlate efficiency losses to $iV_{oc}$ values, simulations of such symmetrical structures were run with the same *c*-Si properties as above (160µm thick, ρ=1Ω.cm and $\tau_{p0}$=7ms, which is representative of state-of-the-art wafers used in mass production). A variable $D_{it}$ was also implemented on both top and bottom surfaces (keeping yet the same $D_{it}$ value for both surfaces). From these simulations, charge carriers concentrations were integrated and averaged over the *c*-Si thickness, allowing the calculation of i$V_{oc}$ using $iV_{oc} = \frac{kT}{e} Ln\left[\frac{p \times n}{{n_i}^2}\right]$ where *k*, *T*, *q* and $n_i$ have their usual textbook meanings, and *p* and *n* were taken from the calculated average hole and electron densities.
$S_{eff}$ associated with a given surface was also calculated for various $D_{it}$ values from the same PCD simulation outputs using:

$$S_{eff} = \sqrt{D\frac{1}{\tau_s}} \times tan\left(\frac{W}{2}\sqrt{\frac{1}{D}\left(\frac{1}{\tau_s}\right)}\right) \text{ [14]}$$

where *W* is the structure thickness and *D* the ambipolar carrier diffusion coefficient, and $\tau_s$ is the lifetime limited by surface recombination. In order to extract $\tau_s$ from the simulations, the structure was solved at Δn=10$^{15}$cm$^{-3}$ and chosen thin enough to ensure and homogeneous effective lifetime $\tau_{eff}$ in the c-Si (W=5µm). In doing so, $\tau_{eff}$ converges towards $\tau_s$ which eases the extraction of $\tau_s$ from the simulations.

Ultimately, the performances of a M6 full size cell with TCO-free edges were then simulated as a function of the edge $D_{it}$ and the corresponding i$V_{oc}$ and $S_{eff}$. The cell features the same bulk properties as the symmetrical structure and included a TCO-free edge (L=1mm). The results are plotted in Fig.8.

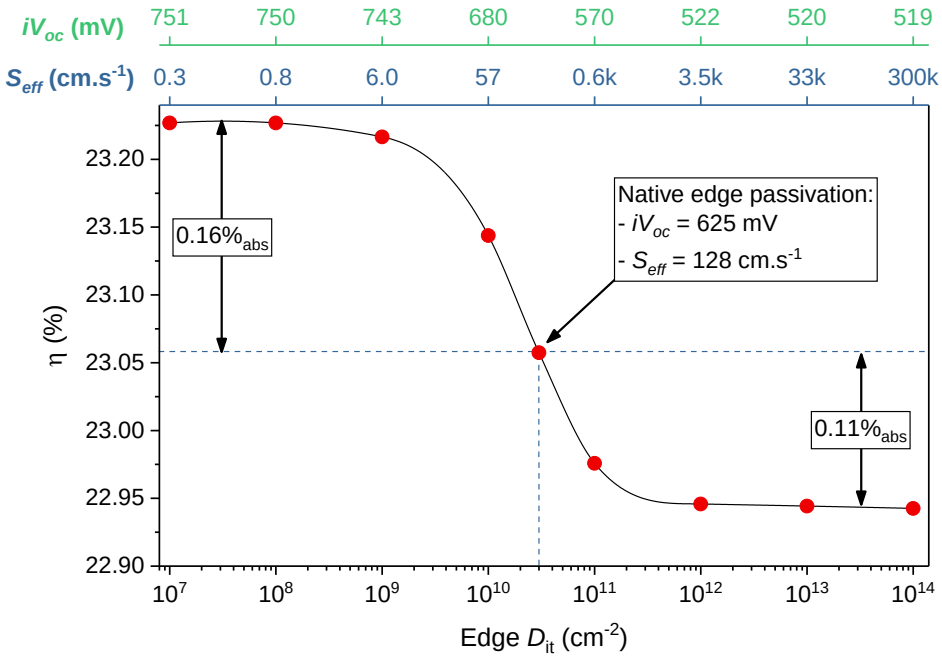


*Figure 8: Variation of the efficiency ($\eta$) for a full size cell as a function of the implemented $D_{it}$ on the TCO-free edges and the corresponding values of $S_{eff}$ and $iV_{oc}$ calculated from PhotoConductance Decay (PCD) simulations. Resistivity = 1Ω.cm and bulk carrier lifetime is 4.5ms (injection level of $1\times10^{15}cm^{-3}$)*

From Fig.8, it can be derived that the native edge passivation quality for SHJ practical cells would lead to $iV_{oc}$ = 625mV (for the chosen wafer bulk properties) and $S_{eff}$ = 128 cm.s$^{-1}$ (at $\Delta n=10^{15}cm^{-3}$) on the symmetrically passivated wafer structure. Such passivation level is significantly lower than what is achieved in practice using state-of-the-art a-Si:H layer stacks [14]. Nevertheless, Fig. 8 demonstrates that with such "medium" passivation quality, the $\eta$ can already be improved by 0.11% abs. with respect to the case without any edge passivation. In addition, if one assumes an optimistic passivation scenario associated with an $S_{eff}$ = 0.3cm.s$^{-1}$ or below such passivation qualities are presented in [14]), the corresponding expected gain with respect to the case without any passivation is pushed to 0.28% abs., which is 0.16% higher than cells with native edges characterized by Dit = $3\times10^{10}cm^{-2}$.

In summary, the combination of the reduction of $L$ and $\rho$ associated with a slight improvement in edge passivation quality bears a non-negligible potential to increase the SHJ cell $\eta$. Although the beneficial effects of these optimisations are likely not cumulative, their association remains an efficient lever for the mitigation of edge-induced losses, even more for cut-cells, which are investigated in the following section.

## E. Transposition to Cut-cells

Cut-cells are obtained through the division of entire cells into smaller cells. In doing so, the current generated by each cut-cell is lowered in proportion to the surface reduction. The resistive losses per individual cell are thereby reduced but their perimeter/surface ratio is increased, giving potentially more weight to edge recombination, particularly in the case where the cut edges are left unpassivated.

In this section, the corresponding losses are assessed for different cut-cell types. We assume that the uncut edges are TCO-free edges with edge recombination characterized by $D_{it}$ = $3\times10^{10}$ cm$^{-2}$. The c-Si properties were unchanged (160µm thick, ρ=1Ω.cm and $\tau_{p0}$=7ms). The investigated cell formats are M6, M10 and M12 full size, each declined into half, third, quarter and sixth-cells. Regarding simulation details, note that the performances for each of the 20 configurations were simulated without interconnection considerations. Also, the pitch between two consecutive fingers as well as that between two consecutive measurement wires (Busbarless design) were kept constant. The performances variations between formats can thus be exclusively attributed to variations in the nature of the edges and in the perimeter/surface ratio.

Note that for a full-size cell cut into n cut-cells with n≥3, two specific types of cells need to be considered:

- Cut-cell cut out of the center of the mother full-size cell, referred to as "α-type cut-cell"
- Cut-cell cut out of the border of the mother full-size cell, referred to as "β-type cut-cell".

While α-type cut-cells feature two TCO-covered (cut) long edges and two TCO-free edges, the β-type cut-cells have three TCO-free edges and only one TCO-covered long edge. The 1/2-cells can therefore be considered as β-type cut-cells. In a first sequence, the cut-cells performances were simulated without repassivation of the cut edge(s) ($D_{it}$ = $10^{14}$ $cm^{-2}$). The predicted $\eta$ are plotted in Table 1.

| | a) α-type cut-cell simulated $\eta$ (%) | | | b) β-type cut-cell simulated $\eta$ (%) | | |
|---|---|---|---|---|---|---|
| | M6 | M10 | M12 | M6 | M10 | M12 |
| Full size | 23.07 | 23.09 | 23.14 | 23.07 | 23.09 | 23.14 |
| 1/2 Cell | 22.91 | 22.94 | 23 | 22.91 | 22.94 | 23 |
| 1/3 Cell | 22.74 | 22.79 | 22.87 | 22.74 | 22.8 | 22.87 |
| 1/4 Cell | 22.59 | 22.64 | 22.74 | 22.58 | 22.65 | 22.75 |
| 1/6 Cell | 22.27 | 22.35 | 22.48 | 22.27 | 22.37 | 22.5 |

*Table 1: Predicted efficiency for full size to 1/6 cells from M6 to M12 cells. For 1/3, 1/4 and 1/6 cells, α-type cut-cells and β-type cut-cells $\eta$ are separated in a) and b) respectively. The $\eta$ of cut-cells were calculated without any cut-edge repassivation ($D_{it}$=$10^{14}$$cm^{-2}$)*

Table 1 a) and 1 b) call for several comments. First, we can see that the smaller the cut-cell, the larger the $\eta$ loss compared to full-size cell, with up to 0.8%$_{abs.}$ loss for the M6 1/6 cell. Interestingly, η appears to be virtually insensitive to the origin of the cut-cell, be it α- or β-type, despite the significantly different nature of the edges in both cases. From these two observations, we can infer that the nature of the cut-cell edges (native or cut) does not drive at first order the cut-cell $\eta$, which is rather driven by the perimeter/surface ration. In order to ascertain this, the $\eta$ presented in Table 1 are plotted as a function of this ratio in Fig.9.

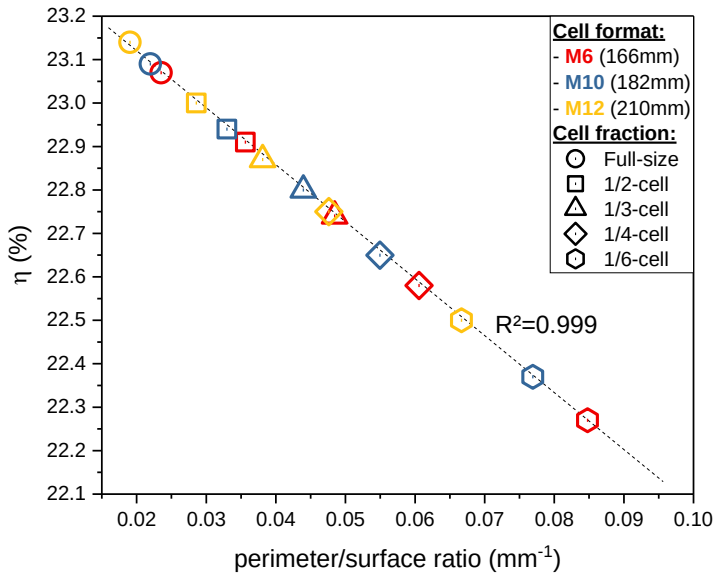


*Figure 9: Cut-cells efficiency as a function of their perimeter/surface ratio. Edge $D_{it}$=$3\times10^{10}$$cm^{-2}$ for native edge, $D_{it}$=$10^{14}$$cm^{-2}$ for cut edge. Since a-type and b-type cells have the same performance in the as-cut condition, only the performances of a-type cells are given here.*

The very clear linear trend in Fig.9 confirms that the $\eta$ variation is mainly driven by the $\frac{Perimeter}{surface}$ ratio. The residual negligible variations around the linear trend are driven by the proportion of masked and covered edges.

One may have expected a stronger influence of the different edge natures in α- and β-type cut-cells. This can however be well explained in light of the learnings from section C.2. Indeed, the results plotted in Fig. 4 show that the mother cell with native edges (TCO-free and $D_{it}$=3×10$^{10}$cm$^{-2}$) have approximately the same performance than with totally depassivated TCO-covered edges. Since all the edges of the cut cells right after the cutting step have the same impact on their performances for CEA cells, the similarities between α-type and β-type cut cells are consistent. For other cells with a different TCO-free region length or/and native edge passivation the efficiencies of α-type and β-type cut-cells may be different.

As a consequence, since the α-type and β-type cut cells have the same $\eta$ just after the cutting step in an industrial line, the dispersion of the cut-cells $\eta$ is therefore expected to be very low if measured before any repassivation step.

Our group have reported on edge repassivation schemes to improve the final cut-cell efficiency [3][4]. In order to assess the potential of repassivation, complementary simulations were run to estimate the achievable $\eta$. The edge passivation was applied to all cut cells, *i.e* on two edges for α–type cells and one for β-type cells. The cut edge $D_{it}$ for both α-type and β-type cut-cells was set to $D_{it}$ = 3×10$^{10}$ cm$^{-2}$ in order to simulate a realistic case. Calculation results are given in Table 2.

| | a) α-type cut-cell simulated $\eta$ (%) | | | | b) β-type cut-cell simulated $\eta$ (%) | | |
|---|---|---|---|---|---|---|---|
| | M6 | M10 | M12 | | M6 | M10 | M12 |
| Full size | **23.07** | **23.09** | **23.14** | | **23.07** | **23.09** | **23.14** |
| 1/2 Cell | **23.01** | **23.07** | **23.08** | . | **23.01** | **23.07** | **23.08** |
| 1/3 Cell | **23.04** | **23.07** | **23.12** | | **22.9** | **22.93** | **22.99** |
| 1/4 Cell | **23.02** | **23.02** | **23.07** | | **22.79** | **22.83** | **22.9** |
| 1/6 Cell | **22.86** | **22.9** | **22.97** | | **22.57** | **22.62** | **22.72** |

*Table 2: Predicted $\eta$ after realistic repassivation of the cut edge(s). For 1/3, 1/4 and 1/6 cells, predicted efficiencies values differ whether α-type (a) or β-type (b) cut-cells are considered.*

As can be observed from Table 2, this realistic yet challenging repassivation level is predicted to efficiently recover the cutting-induced performance losses. Discussing the practical repassivation of cell edges is beyond the scope of this study. However several groups have already successfully developed very promising processes [15,16], demonstrating the practical feasibility of edge repassivation. The maximum amplitude of that recovery is observed for the M6 α-type 1/6-cells (highest perimeter/surface ratio), where 0.6%$_{abs}$ of the 0.8%$_{abs}$ cutting-induced $\eta$ drop are recovered (post cutting: 22.27% to post-passivation: 22.86%). Repassivation is therefore a strong lever to improve $\eta$ of cut cells, provided that repassivation levels close to what is observed for native edges can be reached.

Interestingly, the beneficial effects of repassivation are significantly reduced for β-type cut-cells since they only have one repassivated cut edge. The differences in $\eta$ between α-type and β-type cut-cells are particularly pronounced for M6 1/6-cells (largest perimeter/surface ratio) for which the $\eta$ recovery are doubled from the α–type to the β-type cut-cells (α-type: 0.6%$_{abs}$ vs β-type: 0.3%$_{abs}$ recovery).

It also can be noticed that, even if the perimeter/surface ratio for α-type 1/3-cells is less favourable than for 1/2-cells, $\eta$ of 1/3-cells is predicted to be higher after edge repassivation, still owing to the strong $\eta$ recovery reached with edge $D_{it}$=3×10$^{10}$cm$^{-2}$ associated to the TCO-covered edges.

In order to better illustrate the advantages of α-type over β-type cut-cells, let us compare for a given M10 mother cell, the variation of the α-type cut-cell with the highest perimeter/surface ratio (1/6-cell) to that of the β-type cut-cell with lowest perimeter/surface ratio (1/2-cell) as a function of the cut edge passivation quality. The predicted $\eta$ are plotted in Fig.10 as a function of the edge $D_{it}$, as well as $iV_{oc}$ and $S_{eff}$.

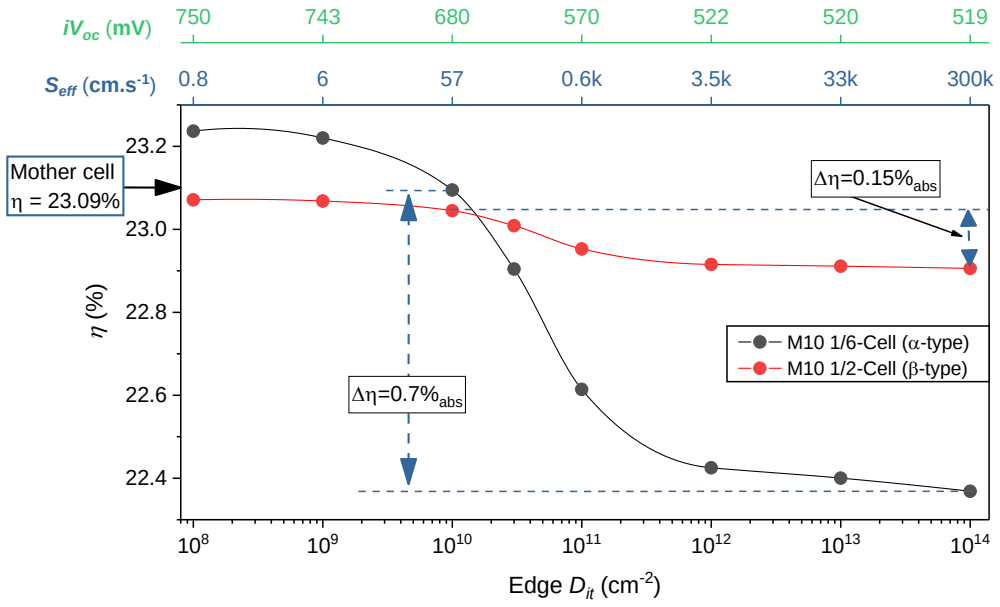


*Figure 10: simulated $\eta$ of a M10 α-type 1/6-cell (black) and a M10 1/2-cell (red) as a function of the passivation quality of the cut edge(s). The efficiency of the cell before the cutting step (mother cell) is also shown on the vertical axis.*

If the edge passivation quality can reach $iV_{oc}$≈680mV ($D_{it}$ =$10^{10}$ $cm^{-2}$) on the symmetrical test architecture, the $\eta$ is expected to be improved by 0.15%$_{abs}$ and 0.7% $_{abs}$ from the post-cutting situation for 1/2 and 1/6-cells. Although the $\frac{Perimeter}{surface}$ ratio of the α-type 1/6-cell is three times higher than that of the 1/2-cell (see Fig. 9), its $\eta$ would end up at a higher level than that of the 1/2-cell. Furthermore, for passivation quality characterized by $iV_{oc}$>680 mV the 1/6-cell can even outperform its mother cell while the 1/2-cell $\eta$ is capped at this limit. Moving the industrial production to cut-cells could therefore unlock higher module performances, by combining resistive losses mitigation with the increase of the maximum power point reachable for a given active surface, provided that a cut edge passivation step is implemented. This is particularly promising to 1/6-cells as shown in Fig. 10.

As a practical application for shingle modules, we recommend to overlap shingling cells on the TCO-free edges, whatever the cut edge passivation quality. Such edges were shown to be more detrimental to the cut-cell performances than the TCO-covered edges. This statement is all the more true when the cut edges are repassivated.

## F. Conclusion

In this work, we used simulations to investigate the effects of the cell edges on the performance of silicon heterojunction cut-cells. We first studied the influence of the TCO-free native edges on the performance of full-size cells. Although this region is necessary to avoid shunt between the front and rear sides of the cell, our results suggest that the TCO-free region hinders the cell performances (Δη=0.17%$_{abs}$ for full size M6 cell) even without any edge defects. These losses result from a lengthening of the collection path for holes photogenerated in this region. In a second investigation, the efficiency of cells with TCO-free or TCO-covered edges were simulated as a function of the edge $D_{it}$. The TCO-free region was shown to limit the *FF* losses attributed to edge recombination, while the $J_{sc}$ degrades more. From considerations based on the study of quasi-Fermi levels in the wafer, we were able to explain these trends in qualitative and quantitative ways. Then, the simulation results were used to derive pratical guidelines for the mitigation of the edge-induced losses. In particular, the reduction of the wafer resistivity was evidenced as a powerful lever to reduce the impact of edges and eventually optimise the cell performance, whatever the edge geometry (from TCO-free to TCO-covered). We conjecture that the benefits of a resistivity reduction also apply to cut-cells for which the perimeter/surface ratio can be very high and TCO-free and TCO-covered edges coexist.

Transposing our investigations to cut cells, the losses induced by the cutting step of the mother cell were shown to be the same whether the cut-cell is generated from the lateral or the central part (respectively β-type and α-type) of the mother cell, which should ease cell sorting in a production environment. However, we highlighted that this result is expected to change if repassivation of the cut edges is implemented, as this step may lead to

significant efficiency discrepancies between α-type and β-type cut-cells. In extreme conditions (1/6-cells and very efficient edge repassivation) the efficiency of a cut-cell with repassivated cut-edges could in principle even surpass that of its mother cell.

As a conclusion, the combination of the optimisations made on the TCO-free region, the edge passivation quality and the wafer properties can significantly contribute to the increase of cut-cells efficiency. To illustrate this, we estimated that, for a $\alpha$-type 1/6-cell, the repassivation of the cut edge close to the level of the native edge passivation on full cells could unlock a $0.6\%_{abs}$ efficiency improvement from the post cutting condition (see table.1 and Table.2). In the case the edge can not be passivated, the reduction of the c-Si $\rho$ could allow to mitigate the losses induced by the bare silicon cut edge.

## Aknowledgements

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## References

[1] J. Zhao, M. König, Y. Yao, YC. Wang, R. Zhou, T. Xie, H. Deng, >24% Silicon Heterojunction Solar Cells on Meyer Burger's on Mass Production Tools and How Wafer Material Impacts Cell Parameters, in: 2018 IEEE 7th World Conference on Photovoltaic Energy Conversion (WCPEC) (A Joint Conference of 45th IEEE PVSC, 28th PVSEC 34th EU PVSEC), 2018: pp. 1514–1519. https://doi.org/10.1109/PVSC.2018.8547908.

[2] International Technology Roadmap for Photovoltaics (ITRPV) - 2021, https://itrpv.vdma.org/documents/27094228/29066965/20210ITRPV/08ccda3a-585e-6a58-6afa-6c20e436cf41 (accessed July 3, 2021).

[3] B. Portaluppi, S. Harrison, V. Giglia, A. Sekkat, D. Munoz-Rojas, Insights on Cell Edge Defects Impact and Post-Process Repassivation for Heterojunction, 37th European Photovoltaic Solar Energy Conference and Exhibition; 504-507. (2020) 4 pages. https://doi.org/10.4229/EUPVSEC20202020-2DV.3.16.

[4] S. Harrison, A. Bettinelli, B. Portaluppi, V. Giglia, C. Carrière, A. Sekkat, D. Munoz-Rojas, V. Barth, Challenges for Efficient Integration of SHJ Based Solar Cells in Shingle Module Configuration, 37th European Photovoltaic Solar Energy Conference and Exhibition; 223-227. (2020) 5 pages. https://doi.org/10.4229/EUPVSEC20202020-2BO.5.5.

[5] F. Haase, S. Schafer, C. Klamt, F. Kiefer, J. Krugener, R. Brendel, R. Peibst, Perimeter Recombination in 25%-Efficient IBC Solar Cells With Passivating POLO Contacts for Both Polarities, IEEE J. Photovoltaics. 8 (2018) 23–29. https://doi.org/10.1109/JPHOTOV.2017.2762592.

[6] Z. Hameiri, F.-J. Ma, The impact of surface damage region and edge recombination on the effective lifetime of silicon wafers at low illumination conditions, Journal of Applied Physics. 117 (2015) 085705. https://doi.org/10.1063/1.4913451.

[7] A. Fell, J. Schon, M. Muller, N. Wohrle, M.C. Schubert, S.W. Glunz, Modeling Edge Recombination in Silicon Solar Cells, IEEE J. Photovoltaics. 8 (2018) 428–434. https://doi.org/10.1109/JPHOTOV.2017.2787020.

[8] Silvaco, Silvaco. https://silvaco.com/

[9] V. Giglia, J. Veirman, R. Varache, B. Portaluppi, S. Harrison, E. Fourmond, Influence of Edge Recombinations on the Performance of Half-, Shingled- and Full Silicon Heterojunction Solar Cells, 37th European Photovoltaic Solar Energy Conference and Exhibition; 282-285. (2020) 4 pages, https://doi.org/10.4229/EUPVSEC20202020-2CO.15.4.

[10] V. Giglia, R. Varache, J. Veirman, E. Fourmond, Understanding of the influence of localized surface defectivity properties on the performances of silicon heterojunction cells, Prog Photovolt Res Appl. 28 (2020) 1333–1344. https://doi.org/10.1002/pip.3330.

[11] A. Danel, S. Harrison, B. Martel, C. Roux, K. Aumaille, A.-S. Ozanne, M. Van Den Bossche, N. Rey, A.

Valla, F. Medlège, B. Novel, B. Commault, P. Lefillastre, R. Varache, P. Carroy, S. Bancel, F. Ozanne, D. Muñoz, D. Heslinga, E. Gerritsen, P.J. Ribeyron, Recent Progress on the CEA-INES Heterojunction Solar Cell Pilot Line, 31st European Photovoltaic Solar Energy Conference and Exhibition; 279-283. (2015) 5 pages. https://doi.org/10.4229/EUPVSEC20152015-2BP.1.4.

[12] J. Veirman, R. Varache, M. Albaric, A. Danel, B. Guo, N. Fu, Y.C. Wang, Silicon wafers for industrial n-type SHJ solar cells: Bulk quality requirements, large-scale availability and guidelines for future developments, Solar Energy Materials and Solar Cells. 228 (2021) 111128. https://doi.org/10.1016/j.solmat.2021.111128.

[13] R. A. Sinton and A. Cuevas, "Contactless determination of current–voltage characteristics and minority-carrier lifetimes in semiconductors from quasi-steady-state photoconductance data," Applied Physics Letters 69(17), 2510 (1996). https://doi.org/10.1063/1.117723.

[14] R.S. Bonilla, B. Hoex, P. Hamer, P.R. Wilshaw, Dielectric surface passivation for silicon solar cells: A review, Phys. Status Solidi A. 214 (2017) 1700293. https://doi.org/10.1002/pssa.201700293.

[15] S. Harrison, B. Portaluppi, P. Bertrand, V. Giglia, B. Martel, A. Sekkat, D. Munoz-Rojas, Low Temperature Post-Process Repassivation for Heterojunction Cut-Cells, 38th European Photovoltaic Solar Energy Conference and Exhibition; 167-171. (2021) 5 pages. https://doi.org/10.4229/EUPVSEC20212021-2BO.15.3.

[16] Munzer, Anna, Puzant Baliozian, Anamaria Steinmetz, et al. « Post-Separation Processing for Silicon Heterojunction Half Solar Cells With Passivated Edges ». IEEE Journal of Photovoltaics 11, no 6 (novembre 2021): 1343‑49. https://doi.org/10.1109/JPHOTOV.2021.3099732.