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***Abstract*—This work presents a new transistor architecture developed by reusing already existing fabrication process steps in an embedded non-volatile memory (eNVM) CMOS technology. The proposed transistor is derived from an existing high-voltage transistor and is free in terms of photomasks and process steps, making it ideal for low-cost products. The new transistor is fabricated then electrically characterized, showing good analog performances. A SPICE (Simulation Program with Integrated Circuit Emphasis) model of the new device is developed to assess its circuit-level performances through electrical circuit simulation. The in-circuit performances of the new device are evaluated based on different ring oscillator circuits. A comparison with the existing high-voltage transistor is carried out considering performance parameters such as the oscillating frequency to demonstrate the appeal of our new transistor.**

Keywords—transistor, MOSFET, CMOS, zero-cost, analog, ring oscillator, middle-voltage, circuit simulation

I. Introduction

Low-cost transistor architectures requiring a reduced number of photomasks and fabrication process steps are highly desirable for low-cost electronics products found in IoT (Internet of Things) or smart cards for example. An ideal CMOS technology contains a multitude of transistor architectures, each one addressing different voltage ranges, with adjusted implants, gate oxide thicknesses, and spacers. This ideal approach is no longer economically viable in low-cost technology. The number of transistor architectures must be reduced to its minimum. This is particularly true when the technology includes embedded Non-Volatile Memory (eNVM), which requires different types of transistor to operate, including High-Voltage (HV) transistors [1].

In the targeted sub-40 nm eNVM low-cost technology, a single HV transistor architecture is used in all circuit designs that need to withstand a voltage higher than the one supported by the Low-Voltage (LV) digital transistor. There is no middle-voltage (MV) transistor architecture, and no dedicated IO (Input/Output) transistor architecture. This is not optimized, as HV transistors are designed firstly to withstand high-voltages, and not necessarily to have good analog performances, or to provide the smallest silicon footprint. Thus, there is a need for a "zero-cost" device to address the MV range (between 3 and 5 V), which is often neglected in favor of LV or HV transistors in low-cost technology.

In this work, we investigate the possibility of reusing already existing process steps to develop a new zero-cost transistor for MV applications, that have better analog performances than the existing HV transistor. In section II the proposed zero-cost process optimization is presented. The newly fabricated MV transistor has been electrically characterized, the results are shown in section III. These measurements are used to develop a SPICE model of the new transistor; it is presented in section IV. Finally, the transistor model is used in section V in a circuit-level simulation to evaluate its performances compared to the existing HV transistor.

II. New transistor architecture

The new MV transistor reuses most of the process bricks of the HV device which is engineered to withstand voltages up to 10 V on its source, drain and gate. To achieve this, a thick oxide, large spacers, anti-punch-through well implants and large lightly-doped-drain (LDD) implants are used. This is good for high-voltage applications, but not necessarily optimized for low or middle-voltage ones. Compared to the existing HV device, our new MV device uses a thinner oxide, that already exist in the technology and serves as the tunnel oxide for the embedded non-volatile memory. Fig. 1 shows the Transmission Electron Microscopy (TEM) images of our new MV device.

The gate oxide thickness is reduced by 40 %, which has the immediate effect of increasing the gate capacitance C_{OX} (1), lowering the threshold voltage V_T (2) and increasing the drive current I_{ON} (3). We can also predict an enhancement of the threshold voltage matching parameter A_{VT} (4) that is known to be proportional to the gate oxide thickness [2].

Fig. 1. Transmission Electron Microscopy (TEM) images of the new MV device.

$$C_{ox} = \frac{\varepsilon_0 \cdot \varepsilon_{ox}}{T_{ox}} \quad (1)$$

$$V_T \approx \emptyset_m + 2 \cdot \psi_B + \frac{Q_{SS}}{C_{ox}} + \frac{\sqrt{4 \cdot \varepsilon_0 \cdot \varepsilon_{Si} \cdot q \cdot N_A \cdot \psi_B}}{C_{ox}} \quad (2)$$

$$I_{ON} \approx \frac{1}{2} \cdot \mu \cdot C_{ox} \cdot \frac{W}{L} \cdot (VGS_{ON} - V_T)^2 \quad (3)$$

$$A_{VT} \propto T_{ox} \cdot \sqrt[4]{N_A} \quad (4)$$

A low threshold voltage V_T is desirable in analog applications because, for the same polarization voltage, the drive current I_{ON} is higher. It also allows the reduction of the supply voltage because of the wider voltage headroom above the V_T. On the other hand, it is usually accompanied by a higher OFF-state leakage current I_{OFF} [3].

III. Electrical Caracterisation

A. Performance metrics

Important device parameters are the linear and saturated threshold voltages $V_{T\text{-}LIN}$ and $V_{T\text{-}SAT}$, measured at a fixed constant drain current I_D of 100 nA multiplied by the width/length ratio W/L of the transistor, and with a drain-source voltage V_{DS} equal to 0.1 V and 3.3 V, respectively. We are particularly interested in the variations of these parameters with the gate length L of the device, as it can highlight Short Channel Effects (SCE) [4]. We will also study the ON-state saturated drain current I_{ON} at a V_{DS} and gate-source voltage V_{GS} both of 3.3 V, and the OFF-state leakage current I_{OFF} at a V_{DS} of 3.3 V. Finally, the transistor matching performance will be assessed with the threshold voltage matching parameter A_{VT} which is calculated by measuring the standard deviation of the difference of threshold voltages $\sigma(\Delta V_T)$ of many pairs of identical adjacent transistors [2]:

$$A_{VT} = \frac{\sigma(\Delta V_T)}{\sqrt{W \cdot L}} \quad (5)$$

B. Electrical results

The threshold voltage $V_{T\text{-}LIN}$ of both HV and new MV transistors has been measured for different gate lengths (L) between 0.5 and 10 µm, with a width of 10 µm. The results for NMOS are shown in Fig. 2 Those results show the expected V_T shift associated with thinner gate oxide. This is close to a rigid curve shift, and the V_T roll-off indicative of Short-Channel Effects (SCE) is present in both HV and MV transistors. The V_T curve of our new MV device is in an interesting range above 200 mV. This value is low (good for analog applications) but high enough to account for the decrease in V_T with temperature, as the transistor should still have a positive V_T at 125 °C.

The drive current I_{ON} is shown in Fig. 3 for the NMOS. As expected, it is higher than the one for the existing HV transistor. This is a consequence of using a thinner gate oxide, which lowers the V_T.

The leakage current IOFF has been measured and the results for NMOS are shown in Fig. 4. As expected, the OFF-state leakage current is higher with a thinner gate oxide and lower V_T.

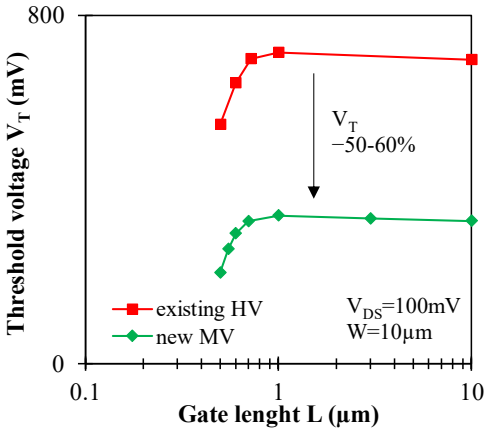

Fig. 2. $V_{T\text{-}LIN}$ versus L for the NMOS of the HV and new MV devices. W=10µm, V_{DS}=0.1V.

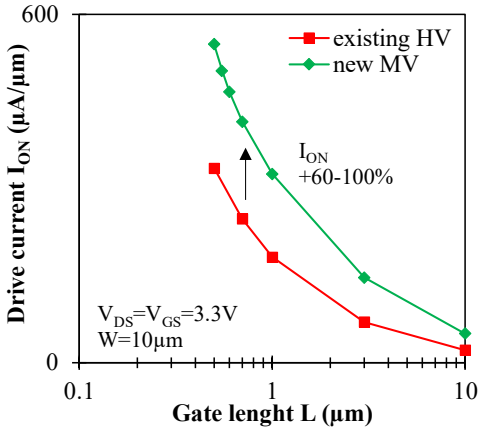

Fig. 3. I_{ON} versus L for the NMOS of the HV and new MV devices. W=10µm, V_{DS}=V_{GS}=3.3V.

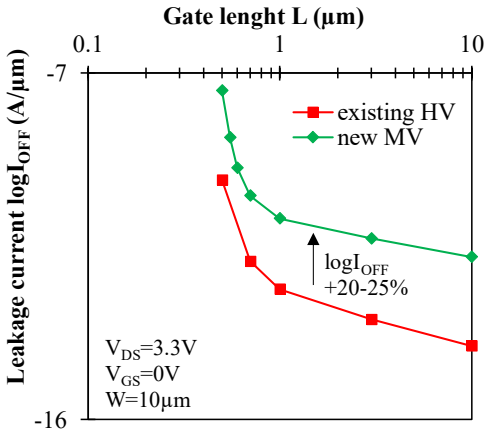

Fig. 4. $\log I_{OFF}$ versus L for the NMOS of the HV and new MV devices. W=10µm, V_{DS}=3.3V, V_{GS}=0V.

The results for the transistor matching performances are presented in the form of a Pelgrom Plot [2] in Fig. 5. The A_{VT} dependence with gate oxide thickness is observed, as our new MV device shows an improved A_{VT} compared to the HV device. A small A_{VT} is highly desirable for analog designs, usually containing a lot of differential pairs and current mirrors, which are fundamental circuit blocks relying on the matching of transistor parameters for optimal performance [2].

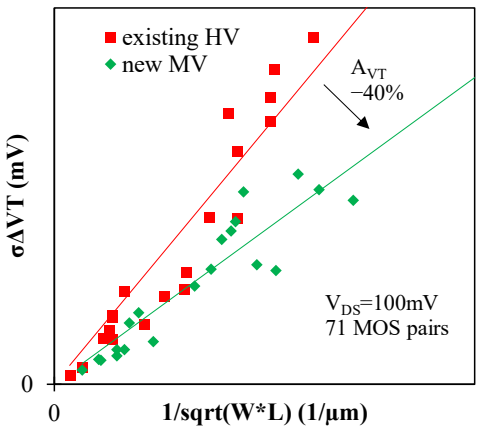

Fig. 5. Pelgrom plot (transistor matching) for the NMOS of existing HV and new MV transistors. V_{DS}=0.1V.

By reusing a thinner oxide already available in the technology, we have obtained a new transistor with enhanced performances that can be made for free in terms of process steps and photomasks. It has a lower V_T (an improvement for analog design), a higher I_{ON} and a better A_{VT} compared to the HV transistor. The main drawback is that SCE limits the L reduction to no lower than 0.7 µm due to V_T roll-off (risking a negative V_T at high temperature or high drain voltage) and increased leakage current I_{OFF} (a maximum acceptable OFF-state leakage current of 100 pA/µm is usually chosen).

IV. Electrical Modelisation

A SPICE electrical model has been developed based on electrical measurement on our new MV transistor for various gate lengths and widths, various drain-source voltages, various gate-source voltages, various bulk-source voltages, and various temperatures. The model is based upon the PSP MOSFET model card [5], and its various parameters are set to fit the experimental data. A similar electrical model already exists for the HV transistor.

The model card parameters have been validated against measurements. For instance, Fig. 6 and Fig. 7 show the comparison between measurement and our SPICE model for two important characteristics, respectively the transconductance curve $I_{DS}(V_{GS};V_{BS})$ for four different substrate voltages, and the capacitance-voltage curve C(V). Model data are in good agreement with the measurements; therefore, the model of the new transistor can be used confidently for circuit-level simulations.

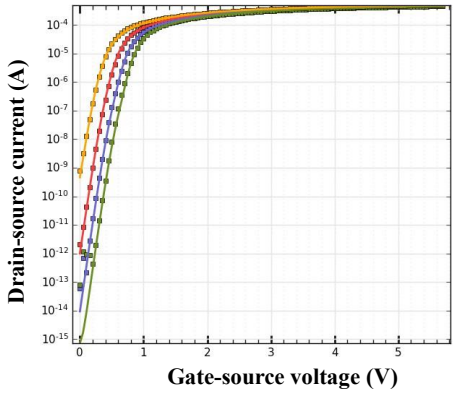

Fig. 6. Model-measurement comparison, $I_{DS}(V_{GS};V_{BS})$ transconductance characteristic, for 4 differents bulk-source bias, for the new MV NMOS transistor. Squares are the measurment points, lines are model data.

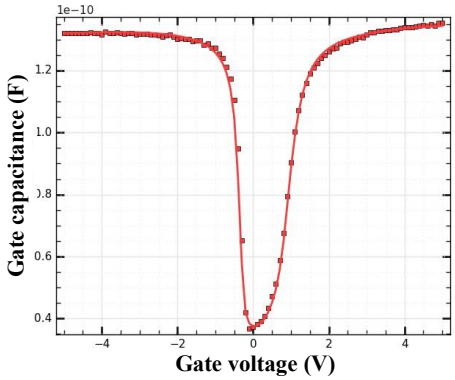

Fig. 7. Model-measurement comparison, capacitance-voltage C(V) curve, for the new MV NMOS transistor. Squares are the measurment points, lines are model data.

V. Circuit-level Evaluation

To evaluate the actual performance gains that our new MV transistor can provide compared to the existing HV transistor, circuit-level simulations have been performed using the newly created SPICE model presented in section IV.

A. Circuit presentation

To assess the performances, a ring oscillator (RO) circuit has been chosen, as it is quite simple and can directly highlight the transistor strengths, with criteria such as oscillation frequency and current consumption. Ring oscillators are basic building blocks of several digital and analog circuits, including voltage-controlled oscillators (VCO) used in phase-locked loops (PLL) [6] and random number generator jitter sources [7]. It is also used to monitor fabrication process variations [8]. In our case it is used as a technology demonstrator, a simple circuit that only need power to operate, to easily compare different transistor technologies.

A ring oscillator consists of an odd number of inverters connected in a ring configuration (Fig. 8a). Fig. 8b shows the schematic of a RO. Each inverter is composed of one NMOS and one PMOS transistor. The outputs of the inverters oscillate between two states at a frequency (f) inversely proportional to the propagation delay (t_d) of one inverter and the number of inverters (n) in the ring [9]:

$$f = \frac{1}{2 \cdot n \cdot t_d} \tag{6}$$

The propagation delay of one inverter is usually expressed with the total capacitance (C_{tot}), the power supply voltage (V_{DD}), and the current (I_D) in the inverter branch:

$$t_d = \frac{C_{tot} \cdot V_{DD}}{I_D} \tag{7}$$

C_{tot} includes all the parasitic capacitances of the two transistors of the inverter (mainly the gate-drain overlap capacitance C_{gd} and the drain-bulk junction capacitance C_{db}) and the input capacitance of the next inverter [9, 10].

Ring oscillators containing 7, 13, 25 and 49 inverters have been simulated, corresponding to oscillating frequencies of f, $f/1.8$, $f/3.6$ and $f/7$, respectively. The gate lengths of the transistors are 0.7 µm, and the gate widths are 0.7 µm for all the NMOS and 1.8 µm for all the PMOS to balance the drive currents of the two types (N and P) of transistors. The same transistor geometries are used for both the existing HV transistor and our new MV to provide an accurate comparison.

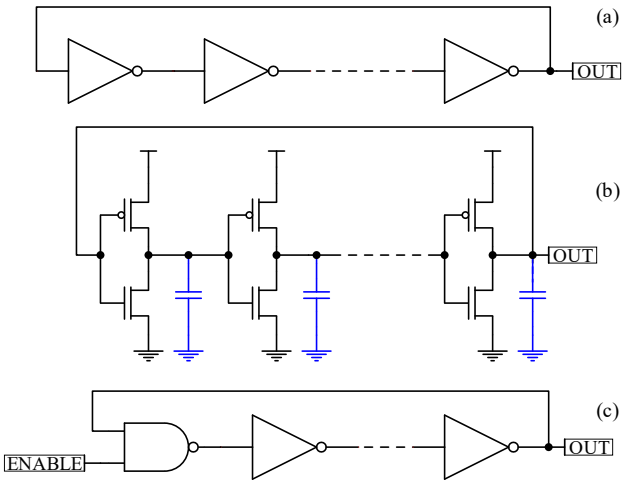

Fig. 8. Gate-level schematic of a RO (a). Electrical schematic of a CMOS RO with and without load capacitors (in blue) (b). Gate-level schematic of a RO with NAND starter (c).

To start the ring oscillators, the first inverter is in the form of a NAND gate, one of its inputs being part of the ring, and the other acting as a circuit-enable input (Fig. 8c).

To illustrate what gains can be achieved at the circuit-level with a transistor having a higher drive current I_{ON}, a second ring oscillator circuit with load capacitors of 40 fF between each inverter is also studied (Fig. 8b with blue capacitors). The transistors will stand out by their ability to quickly charge and discharge these capacitors, impacting the oscillating frequency of the oscillator. Load capacitors increases the propagation delay, corresponding to an increased C_{tot} in (6).

The input parameters of the simulation are the power supply voltage (V_{DD}) and the temperature. Output parameters are the oscillating frequency and the current consumption.

B. Circuit simulation results

Electrical transient simulations have been performed using the Cadence ELDO SPICE simulator.

The oscillating frequency of the smallest simulated ring oscillator (RO), containing 7 inverters and no load capacitors, for a power supply of 3.3 V is 680 MHz for the existing HV transistor and 820 MHz for our new MV transistor, corresponding to a 20 % frequency increase (Fig. 9a). The gate capacitance of the transistors constituting the RO has been increased by 40 % for the new MV transistor compared to the existing HV. A decrease in the RO frequency is therefore expected according to (7), but the drive current I_{ON} has also been increased by ~70 % for the transistor geometries in question (Fig. 3), thus taking over and increasing the oscillating frequency.

When 40 fF load capacitors are connected between each inverter output and the ground, the oscillating frequency of the 7-inverters RO drops to 85 MHz for the existing HV and 150 MHz for our new MV transistor (Fig. 9b). This corresponds to a 75 % frequency increase for our new MV transistor. The frequency gain that a designer can achieve by replacing the existing HV transistor by our new MV transistor is higher when a load is connected, because the drive current I_{ON} of the MV is almost twice that of the HV for the same transistor geometry (L and W) used in the RO.

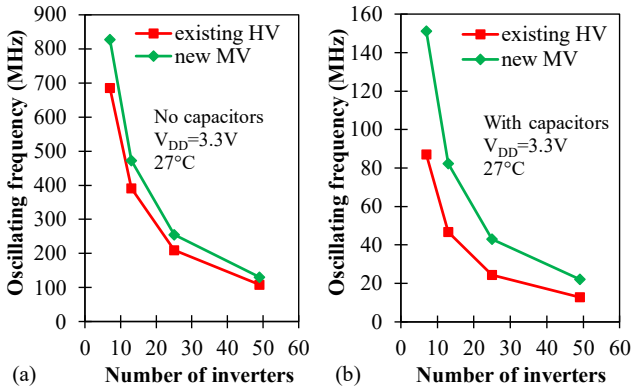

Fig. 9. RO frequency versus the number of inverters, without load capacitors (a) and with 40 fF load capacitors (b) at a supply voltage of 3.3 V for MV and HV based RO.

Fig. 10 shows the dependence of the oscillating frequency of the 7-stage RO on the power supply voltage V_{DD} (a) and on the temperature (b) for both MV and HV RO without load capacitors. The slope of the RO frequency in function of the power supply voltage and the temperature is the same for the two transistors, demonstrating that our new MV does not increase the sensitivity to those two parameters. This is expected, given that the process optimization only targets the gate oxide thickness of the transistor.

Power consumption in ring oscillators originates from two main phenomena: cross-conduction loss, which happens when both NMOS and PMOS transistors conduct at the same time in one inverter, and capacitive loss caused by the parasitic capacitances of the transistors [11]. The MV RO oscillates faster, thus an increase in current consumption is expected. The 7-stage RO without load capacitors composed of HV transistor consumes 650 µW of power at 3.3 V to oscillate at 680 MHz, while the MV-based one consumes 1200 µW of power at 3.3 V and oscillates at 820 MHz. The higher oscillating frequency is paid in terms of current consumption, which increased by 75 %. Decreasing the power supply voltage of the 7-stage MV RO so that it matches the 680 MHz oscillating frequency of HV one, results in a supply voltage of 2.7 V. At that voltage, the MV RO consumes the same 650 µW of power that the HV one consumes at 3.3 V.

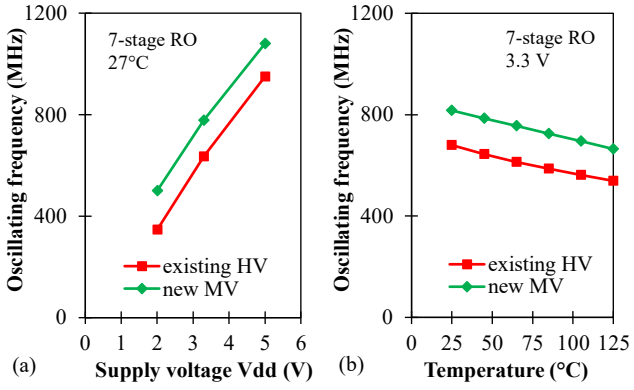

Fig. 10. RO frequency versus power supply voltage (a) and versus temperature (b) for the 7-stage RO without load capacitors, for MV and HV RO.

TABLE I.

	Studied RO parameters for MV and HV transistors			
	Oscillating frequency (7-stage w/o load cap)	***Current capability***	***Supply voltage and temperature sensibility***	***Power consumption (7-stage w/o load cap)***
HV	680 MHz	Lower	Identical	650 µW
MV	820 MHz	Better	Identical	1200 µW

Table I proposes a summary of the MV and HV ROs output parameters. The higher oscillating frequency of the MV RO is correlated with the MV transistor current capability which is higher than the HV transistor. No difference in sensibility to power supply voltage and temperature variation is reported for the MV RO compared to the HV one. Finally, the current consumption is almost two times larger for the MV RO for oscillating frequency increasing from 680 MHz to 820 MHz. To reduce current consumption in a real-world utilization, the designer may want to use circuit optimizations, for example by using current-limiting transistors in the inverter branches [12].

VI. CONLUSION

A simple process optimization is proposed to build a new zero-cost transistor in terms of photomask and fabrication process steps, to address the 3 to 5 V middle-voltage (MV) range in an eNVM technology. The new transistor is aimed to replace an existing high-voltage (HV) transistor not optimized for analog applications. The process optimization lowers the V_T, increases the $I_{ON,}$ and enhance the matching parameter A_{VT} at the cost of an increased I_{OFF} compared to the HV device. The new MV device is benchmarked at the circuit-level against the existing HV in simulations of ring oscillators (RO) circuits. Simulation results show a more important oscillating frequency for the MV device at the cost of an increased power consumption. When load capacitors are inserted between each inverter output composing the RO and the ground, the oscillating frequency difference between the HV and the new MV device is even bigger. This last result demonstrates the higher current driving capability of the new MV transistor.

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