Neutron-Induced Failure Dependence on Reverse Gate Voltage for SiC Power MOSFETs in Atmospheric Environment

K. Niskanen, Rosine Coq Germanicus, A. Michez, Frédéric Wrobel, Jérôme Boch, Frédéric Saigné, Antoine Touboul

Neutron induced failure dependence on reverse gate voltage for SiC Power MOSFETs in atmospheric environment

K. Niskanen, R. Coq Germanicus, A. Michez, F. Wrobel, J. Boch, F. Saigné and A. D. Touboul

***Abstract*—The mechanisms responsible for the neutron-induced single event burnout (SEB) in commercial Silicon Carbide power MOSFETs under atmospheric-like neutron spectrum was investigated and analyzed. Combined effect of applied reverse gate voltage and drain voltage was evaluated. First, local analysis of the packaged device at the wafer level is performed to reveal the failure mechanism inside the semiconductor lattice. Secondly, based on gate stress testing of survived devices and looking at the influence of reverse gate bias during irradiation, we demonstrated an enhanced failure sensitivity especially for drain voltage values close to the safe operating area. In addition to support this assumption, TCAD simulations with damage sites were performed in order to address physical mechanisms related to gate leakage degradation and SEB.**

***Index Terms*—Silicon carbide, power MOSFET, neutrons, single event burnout**

I. Introduction

Power MOSFETs have been known for decades to be susceptible to atmospheric environment [1], [2]. In particular, it is well known that their failure probability increases with applied drain-to-source voltage (V_{DS}). For device qualification, the most common method for assessing the radiation sensitivity of power MOSFET is to test with different V_{DS} values while gate-to-source voltage (V_{GS}) is kept at 0 V. This is to ensure that the transistor is in off-state which means there is no current flowing through the channel of the transistor. In this context, several studies focused on the effect of applied drain voltage on destructive failure sensitivity of SiC power MOSFETs under atmospheric neutron environment [3]–[7] and heavy ion irradiations [8], [9]. However, the impact of gate voltage on the sensitivity to radiation induced failure has not been considered in such studies.

For silicon devices, the effect of gate voltage on the single event burnout (SEB) sensitivity under atmospheric neutron environment has been investigated in some studies for IGBTs [10] and power MOSFETs [11], [12]. The contribution of gate voltage is often related to single event gate rupture (SEGR). For SiC MOS power devices, SEGR sensitivity has been reported to be lower compared to Si devices [13]. Therefore, SEGR is not supposed to be the main failure mechanism to be expected for SiC devices.

When power MOSFET devices are used in operation, such as in switching power converter, the V_{GS} is likely to vary between negative and positive values. For example, in switching power converter utilizing SiC power MOSFET, V_{GS} can vary from -4 V to 15 V during switching operation [14]. Therefore, it is important to assess, if the off-state gate voltage plays a role in the sensitivity to destructive failure while operating in radiation environment.

In this paper, the effect of reverse applied gate voltage on the SEB sensitivity of SiC power MOSFET during neutron irradiation is investigated. For this, three different drain bias voltages are used during the test for two different V_{GS} values: 0 V and maximum negative value. For failed devices, a failure analysis at the wafer level has been performed in order to identify and well understand the SEB mechanisms and consequences. In addition, to perform a comprehensive study, post irradiation gate stress (PIGS) testing and simulations are performed for survived devices in order to reveal possible latent damage induced by neutron radiation

II. Experimental details

Devices under test (DUT) in this study are discrete commercial 3rd generation SiC power MOSFETs manufactured by CREE (part number C3M0120090D, lot number W14918). Each device has the same lot number. The devices have vertical structure and the package type is TO-247-3. Nominal maximum ratings are V_{DS} = 900 V, V_{GS} = -4/+15 V, I_{DS} = 23 A and R_{on} = 120 mΩ. Electrical characterizations, including $I_{DS}V_{GS}$ and $I_{GS}V_{GS}$ measurements, have been performed before and after irradiation. In addition, forward $I_{DS}V_{DS}$ characteristics of the body diode were also measured.

In total, 120 devices and 6 voltage configurations during irradiation were tested. 20 DUTs per configuration were irradiated at room temperature in parallel configuration. During irradiation, devices were biased at V_{DS} = 675 V, V_{DS} = 765 V and V_{DS} = 900 V (75%, 85% and 100% of V_{DSmax} respectively).

K. Niskanen, A. D. Touboul, A. Michez, F. Wrobel, J. Boch, and F. Saigné are with IES, Univ Montpellier, CNRS, Montpellier, France (corresponding authors; e-mail: kimmo.niskanen@ies.univ-montp2.fr, antoine.touboul@umontpellier.fr).

R.Coq Germanicus is with Normandie Univ, Unicaen, Iut, Ensicaen, CNRS, Crismat, 14000 Caen, France.

This work has received funding from the European Union's Horizon 2020 research and innovation programme under the Marie-Skolodowska-Curie grant agreement number 721624.

For each V_{DS} value, gate voltage configurations V_{GS} = 0 V and V_{GS} = -4 V were tested. As indicated, the devices for each test configuration were from the same manufacturing lot and therefore, no process related effects on the device behavior should be expected.

A. Facility description

Neutron irradiations were performed at the ChipIr facility [15] in Rutherford Appleton Laboratory, UK. The facility provides atmospheric-like neutron spectrum with acceleration factor of 10^9 compared to ground level neutron flux. The nominal neutron flux was 5.4×10^6 n/cm^2/s ($E_n > 10$ MeV) at the test position. A comparison between the ChipIr neutron energy spectrum and atmospheric neutron energy spectrum is given in [15].

B. Irradiation test setup

For the experimental study, test board schematics follows the MIL-STD-750E test standard [16]. The test board containing DUTs was placed under beam while drain and gate voltages were controlled and total currents were monitored with PC and SMUs in the control room. Drain voltage was applied and total drain current was measured with Heinzinger EVO HV power supply. Gate voltage was applied and corresponding current measured with Keysight B2902A precision source meter unit (SMU). Schematics of the test setup is presented in Fig. 1.

During irradiation, destructive failure of the DUT was identified by step increase of the total current caused by low resistance path inside the device structure.

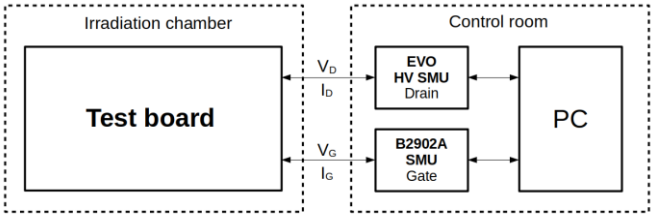

Fig. 1. Test setup schematics. Control instruments were placed in the control room while only the test board containing DUTs was placed under beam in the irradiation chamber.

III. Results and Discussion

A. Reliability extraction from failure data

Based on literature [4], [7], regarding the drain bias, the most sensitive configuration for SEB is the highest drain voltage during the irradiation. Then for this configuration, DUTs were kept under beam until all of the devices were failed. For other configurations, the beam was stopped, when at least 65 % of the DUTs were failed, in order to gain sufficient statistics and plot an accurate reliability law.

To determine statistical failure behavior of the irradiated devices, a Weibull analysis has been performed on the failure data. Y-value for the data points for the Weibull plot were obtained after Benard's approximation [17], which is given in (1):

$$F = \frac{i - 0.3}{N + 0.4}, \tag{1}$$

where i is the running number of the failure and N is the total number of devices. Thus, the value of the fluence for each failure is then determined and represented on the x-axis (Fig. 2). Failure plots for each irradiation run are done in Fig. 2 for all bias configurations. Weibull parameters were extracted by using software library [18] and by using maximum likelihood estimation (MLE). As a cross correlation procedure, second analysis on the failure data was performed by using linear regression (LR) method in which linear fit is performed on the Weibull data by using least squares method.

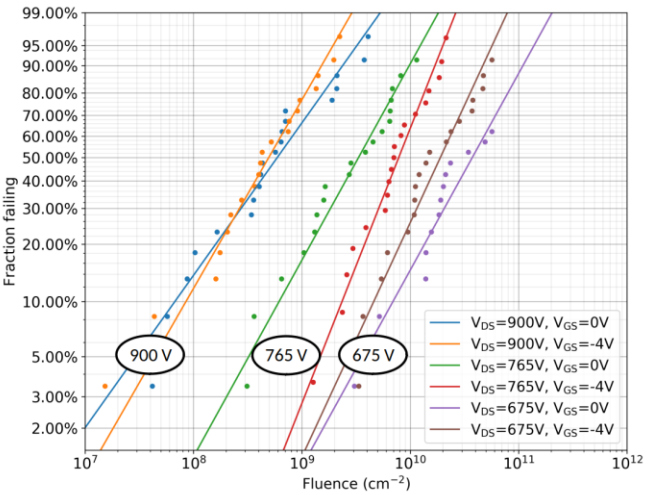

Fig. 2. Weibull plots for different bias voltage configurations during irradiation. Fits are performed with MLE method.

Based on the Weibull parameters, we have also extracted mean fluence to failure (MFTF) which in turn can be derived from extracted Weibull parameters with (2). All the extracted parameters are given in Table I.

$$MFTF = \eta \times \Gamma\left(1 + \frac{1}{\beta}\right) \tag{2}$$

The Weibull shape parameter β is an indicator of failure rate behavior over time. If $\beta < 1$, the distribution will show a decreasing failure rate with time, which is representative of early life failures. If $\beta > 1$, it implies increasing failure rate with time. Finally, $\beta = 1$ implies random failures which means constant failure rate over time. When dealing with neutron-induced failure, a $\beta = 1$ is to be expected.

TABLE I
EXTRACTED RELIABILITY PARAMETERS FOR EACH IRRADIATION CONFIGURATION BY MLE AND LR METHODS

V_{DS} (V)	V_{GS} (V)	Survived/ Failed	β_{MLE}	β_{LR}	η_{MLE} (cm^{-2})	η_{LR} (cm^{-2})	$MTFF_{MLE}$ (cm^{-2})	$MTFF_{LR}$ (cm^{-2})	Stopping fluence (cm^{-2})
675	0	7/13	1.12	1.26	5.19×10^{10}	4.39×10^{10}	4.99×10^{10}	4.08×10^{10}	5.98×10^{10}
	-4	1/19	1.33	1.34	2.49×10^{10}	2.46×10^{10}	2.30×10^{10}	2.26×10^{10}	5.92×10^{10}
765	0	1/19	1.12	1.07	4.63×10^{9}	4.59×10^{9}	4.44×10^{9}	4.47×10^{9}	2.41×10^{10}
	-4	0/20	1.56	1.46	8.98×10^{9}	9.59×10^{9}	8.36×10^{9}	9.79×10^{9}	2.25×10^{10}
900	0	0/20	0.87	0.92	9.06×10^{8}	8.75×10^{8}	9.75×10^{8}	9.11×10^{8}	4.50×10^{9}
	-4	0/20	1.07	0.96	6.96×10^{8}	7.11×10^{8}	6.78×10^{8}	7.23×10^{8}	2.35×10^{9}

B. The effect of combined applied drain and gate voltages on SEB sensitivity

As mentioned earlier, the goal of this study is to investigate the role of applied gate voltage either during irradiations on the SEB occurrence and also on the long term reliability for unfailed devices. Therefore, considering at first the influence of reverse gate bias on SEB sensitivity, two different V_{GS} values for each V_{DS} configuration were tested during irradiations.

By comparing the MFTF values in Table I, we can see, as expected, that the applied bias on the drain strongly increases the risk of failure. The lower the applied V_{DS}, the higher the fluence needed for the device to fail. However, beyond those well-known considerations, this figure rises some questions about the contribution of the reverse gate voltage on the risk of failure during irradiation.

Indeed, looking more closely on the MFTF (Table I) for the lowest applied V_{DS} value (675 V), we can see that the MFTF seems to be affected by the applied gate voltage. This might indicate an enhanced sensitivity to SEB when V_{GS} = -4 V. In literature, similar negative gate bias dependence on the SEB sensitivity has been observed for trench Si IGBT technology [10]. This behavior is not so clearly observed for higher drain voltage, though the behavior at 900 V is unclear. Indeed, if the mean fluence to failure values tend to indicate a higher sensitivity when a reverse gate bias is applied, the minimum and maximum values are overlapping for the two configurations. We assume thus that the contribution of the reverse gate bias to SEB increases as the drain voltage is closer to the safe operating area (SOA) limit, which for this reference has been found to be between 50% and 75% of the applied drain voltage [19]. Indeed, applied drain voltage results in electric field across the drift layer which is an important contributor to the SEB triggering for such devices [20], especially at maximum electrical rating.

In addition to MFTF parameter, we should also pay attention to the number of failed devices for different irradiation configurations in Table I. For irradiation configuration V_{DS} = 675 V, V_{GS} = 0 V, after the beam was stopped, we observe 13 failures over 20 devices irradiated. However, while the reverse gate bias was applied, with the same V_{DS} and same stopping fluence, we observe 19 failures over 20 devices irradiated. This can indicate an enhanced SEB sensitivity for V_{DS} = 675 V configuration when reverse gate bias is applied. For higher V_{DS} values, no such differences between V_{GS} configurations are observed.

Finally, looking at the reported results in Table I, we can see that β values are close to 1 for each configuration, confirming random failures, which is expected failure mode for neutron induced-failures since the interaction is considered stochastic. However, for each V_{DS} voltage configuration, β values for configurations with negative gate voltages are relatively greater compared to configurations with V_{GS} = 0. This behavior might be related to the possibility that reverse gate bias might act as a complementary stressor for the device, giving an increase to the failure rate over time.

Those three aforementioned parameters (MFTF, number of failures, β) give us indication of enhanced SEB sensitivity of SiC MOSFET close to the SOA limit while negative gate bias is applied.

In order to well understand the failure mechanism of SiC power MOSFET and evaluate with precision the parameters which impact the SEB occurring, we performed following investigations:

- On one hand, a failure analysis at the wafer level has been performed for devices having suffered a SEB (section C).
- On the other hand, a Post Irradiation Gate Stress (PIGS) test has been performed for unfailed devices irradiated at V_{DS} = 675 V (section D-1).
- Then, in order to support experimental results and related hypothesis, TCAD simulations have been performed (section D-2).

C. Neutron-induced damage failure analysis at wafer level

In order to increase the understanding of the destructive mechanism, a failed device (having suffered a SEB) was analyzed at the SiC wafer level. For the semiconductor analysis, scanning electron microscopy (SEM) observations were performed at the failure location.

IV-characteristics in Fig. 3 show the electrical signature of the SEB for a device irradiated at V_{DS} = 675 V and V_{GS} = 0 V. Note that I_{DS} reaches the compliance limit of the measurement unit at 1A. A drain to source shortening signature is observed while the gate leakage shows a linear behavior with gate voltage (Fig. 3). This linear gate leakage behavior indicates that the oxide exhibits a resistive response typical of a low resistance current path on the gate.

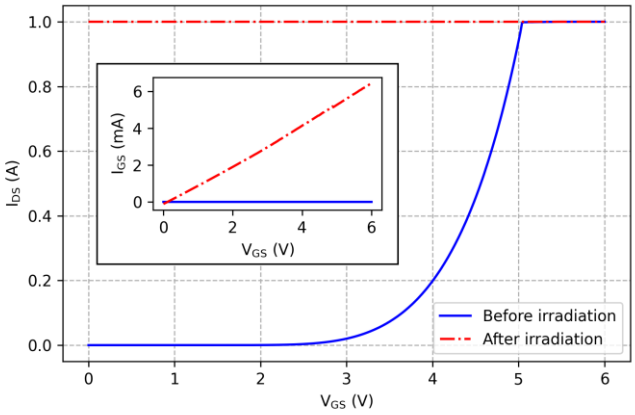

Fig. 3. $I_{DS}V_{GS}$ and $I_{GS}V_{GS}$ characteristics of the failed device before and after irradiation. Device was irradiated at V_{DS} = 675 V and V_{GS} = 0 V Both drain-source and gate failures can be observed after irradiation induced failure. I_{DS} reaches the compliance limit of the measurement unit at 1 A.

In this case, the challenge was to locate the failure. In fact, for SEB failure, the device degradation is the consequence of a single probabilistic neutron interaction with the SiC material of the packaged device. This first interaction originates in the generation of one or several secondary ions themselves able to generate electron-hole pairs in the semiconductor. Thus, because of the stochastic aspect of the interaction, a simple cross-section along an axis parallel to the gates is not suitable. Indeed, the probability to find out the failure signature would be too low. In addition, in our case, it is important to note that the epoxy molding component (EMC) material of the TO-247-3 packaging did not present any defects (holes, peeling, cracks, etc...) allowing to have a first indication of the possible location of the failure signature. This complicated the localization of the SEB defect.

Therefore, before the cutting of the SiC packaged device, a fine localization of the SEB signature at the wafer level is necessary. To this end, an original sample preparation was developed. To be sure to find out and analyze the local degradation for a failed device, several steps are required: packaging opening, localization of the defect, cutting, polishing and observation. Obviously, all steps must maintain the integrity of the defect, which means that the device preparation must not introduce additional defects. For that, after the mechanical opening of the resin package on the back side, the SiC die was thinned from the drain side in order to achieve a thin SiC layer which becomes optically transparent (Fig. 4). After that, we were able to locate the failure point through the thin SiC material. A defect with a diameter of 202 µm was thus optically located from the back side of the thinned SiC. The sample cutting line was then located at the center of the observed failure location and to finish the sample preparation, the cross section of the SiC device was polished. After sample preparation, the device was observed with scanning electron microscopy (SEM). Results are presented in Fig. 5. The cross-sectional SEM view indicates the failure inside the SiC MOSFET structure.

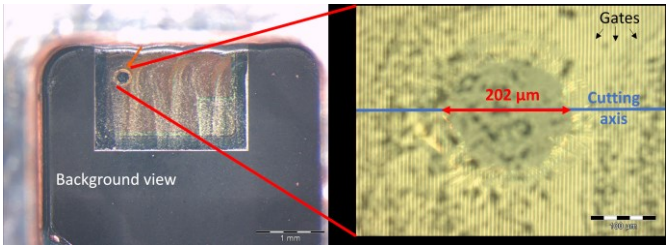

Fig. 4. Localization of the SEB signature at the wafer level after backside opening.

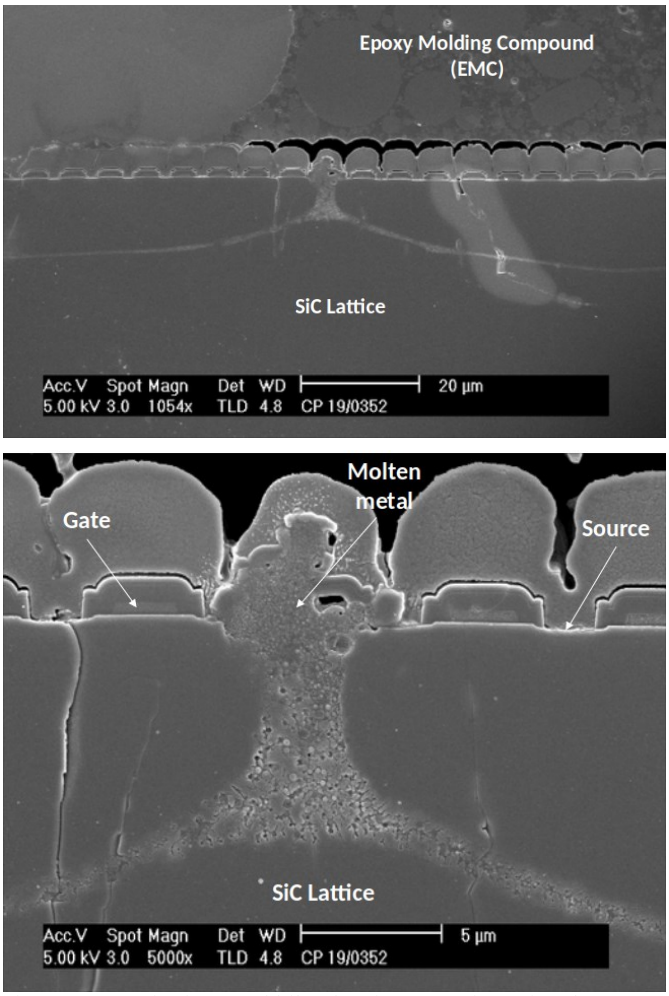

Fig. 5. Cross-section images of failure location. Lower image is a closer zoom of the same location than in the top image. Localized heating point has melted the semiconductor material resulting in low resistance path between the gate, the source and the drain terminals. Device was irradiated at V_{DS} = 675 V and V_{GS} = 0 V.

As expected, no degradation is observed in the EMC material. The neutron passed completely through the EMC packaging without damage. However, a strong detachment of the epoxy matrix is to be noted. Surely a signature of a strong energy release during the SEB. Moreover, a melted area which due to the high localized current and subsequent thermal expansion of the SiC material, is revealed.

We can see in Fig. 5 that width of the damage site is similar to the width of the elementary cell. In particular, we can observe that the oxide region has been melted for a single cell. According to our best knowledge, this is the first time that

neutron SEB failure is located and analyzed by SEM while there are no cracks on the packaging of the commercial SiC power MOSFET. In addition to the damage caused by the melting of the metallic contact at the device surface leading to the melting of the oxide region, the melting occurs also deeper below in the SiC material. We also identified two main cracks inside the lattice of the device localized in the N^- drift region. For this region, the doping has a lower value and therefore the layer material has higher resistance compared to highly doped drain layer. Higher resistance led thus to higher power dissipation and further higher temperature along the current path which eventually led to cracking of the semiconductor material. From this local analysis of the SEB signature at the wafer level, we turned our attention to gate oxide for the following.

D.Post-irradiation gate stress for survived devices and TCAD simulations

In this section, the long term reliability of survived devices is investigated. Indeed, though those devices have not suffered a SEB, they have very likely suffered non-destructive neutron interactions. This means that, due to the high electric fields inside each device cell, some current transients might have been generated inducing possibly some latent defects. Thus, a post irradiation gate stress (PIGS) has been performed on those devices in order to determine whether they were weakened due to irradiation (Section D-1). In section D-2, a hypothesis will be raised thanks to TCAD simulation focusing in particular on the contribution of the reverse gate bias.

1) Post-irradiation stress test

Looking at the lowest SEB sensitivity irradiation configuration (V_{DS} = 675 V, V_{GS} = 0 V), 7 devices over 20 did not exhibit SEB when the beam was stopped. In order to reveal possible latent damage induced by the neutron interaction, PIGS measurements were performed for these survived devices.

During the PIGS test, drain terminal was shorted with source terminal (V_{DS} = 0 V) and gate voltage was swept from -8 V to +19 V, which is the safe dynamic gate voltage range for this technology. Before this stress test, note that no differences were observed in $I_{DS}V_{GS}$ characteristics or in body-diode forward $I_{DS}V_{DS}$ characteristics between pre- and post-irradiation measurements. However, in the survived devices lot, 3 devices over 7 show an increased gate current level during PIGS after neutron irradiation (Fig. 6). Due to a high sensitivity to SEB (only one survived device), the sensitivity to PIGS test of the other gate bias configuration (V_{DS} = 765 V, V_{GS} = -4 V) was not able to be investigated.

This means that for experimental data shown on Fig. 6, the gate degradation observed is only related to the influence of the electrical field induced by the V_{DS} which resulted in transient currents through the oxide, generating subsequent latent damage sites within the oxide or at its interface. Therefore, though the latent damage generation should be emphasized by the reverse gate bias (as this will be discussed in section D.2 with the TCAD analysis), it was observed that the applied drain-to-source voltage during irradiation is enough to generate latent damage sites within the oxide. Similar post-irradiation gate leakage has been observed also after heavy ion impact for SiC power MOSFETs [21], [22], confirming our hypothesis.

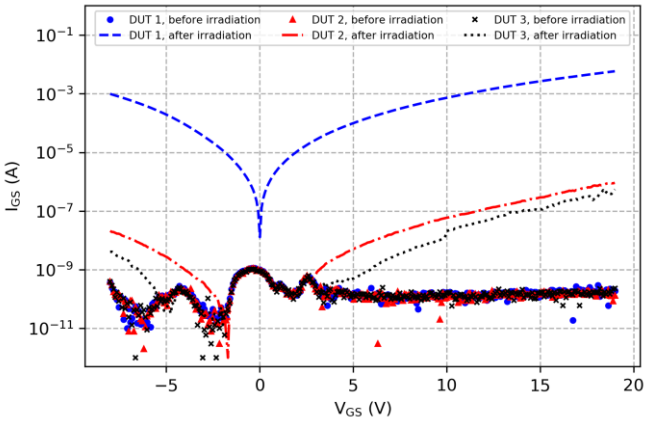

Fig. 6. Gate current (absolute value) of the survived devices before and after irradiation. Devices were irradiated at V_{DS} = 675 V, V_{GS} = 0 V. 3 of 7 survived devices show increased gate current levels during post-irradiation gate stress.

Indeed, looking at the devices having survived to neutron-irradiation, a clear gate oxide degradation has been revealed for almost the half of them (3 over 7). Concerning their functional capabilities, devices still maintained their blocking and switching capabilities.

However, those survived devices clearly exhibit a weakening of the gate oxide which might lead to a decrease of their lifetime. As an assumption, secondary ions generated by the primary neutron interaction, have induced free carrier generation. Depending on the location of the primary interaction, carriers have drifted or diffused. Due to the electric filed repartition, some interactions might have generated carriers which have drifted in the neck region below the oxide region leading to localized stresses by transient current through the oxide layer. Such localized electrical micro stress might induce localized interface and oxide traps originating in a decrease of local oxide resistivity and leading to an overall device reliability degradation.

2) TCAD simulation study

TCAD simulations were performed in order to address the physical mechanism of the device degradation and the impact of drain and gate bias on the failure behavior. TCAD tool ECORCE specifically developed for radiation effects studies [23] was used for this purpose. ECORCE uses a drift-diffusion model coupled with the heat equation (i.e., thermodynamic simulation with lattice temperature) and provides an automated and dynamic mesh generator that optimizes the mesh distribution for all modeling steps for either DC or transient analysis, and for 1D, 2D and axisymmetric geometries.

The implemented device geometry is presented in Fig. 7 and the simulation parameters are based on the previous work [19]. Charge deposition subsequent to neutron interaction is modelled by Si-ion hit in the device active volume. In the following simulations, the ion impact occurs at t = 1×10^{-14} s.

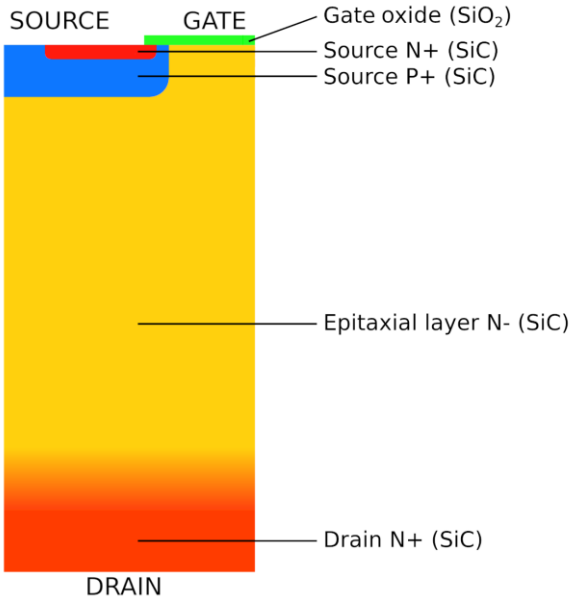

Fig. 7. SiC MOSFET geometry implemented in TCAD simulation tool ECORCE.

a) The effect of radiation impact on gate degradation

At first we have focused on the non-destructive interaction impact on the gate oxide. For that, the hole density (Fig. 8) and the electric field (Fig. 9) in the gate oxide layer were observed during charge deposition and transport inside the device structure. The impacting Si-ion energy was 30 MeV which has a range of 7.1 µm in SiC and a linear energy transfer (LET) value of 15.5 MeV cm^2 mg^{-1}. During simulations, investigated bias configurations were fixed at V_{DS} = 675 V for two applied gate bias V_{GS} = 0 V and V_{GS} = -4 V.

Due to neutron impact and secondary recoiling ion, electron-hole pairs are generated along the ion track in the SiC epitaxial layer. Observing the hole density right under the oxide layer brings a crucial information on the possibility that transient currents induced by secondary generated ions might create a localized micro stress of the oxide leading to the subsequent creation of latent damage sites. Investigation with TCAD the transport of holes for a specific ion track location in the neck region, a significant hole accumulation under the gate oxide layer is observed (Fig. 8). We can note that this result is similar to the SEGR mechanism observed in Si power MOSFETs [24] though no SEGR has been observed during experiments. Based on experimental results and on TCAD simulations, it is thus expected that an applied negative gate bias would reinforce the probability of localized latent damage creation within the oxide, since the electric field in the oxide layer will reach higher value. Fig. 9 represents the simulated electric field in the device at t=0 ps and t = 3 ps after the ion impact.

A strong increase in electric field in the gate oxide during the ion impact is observed and can be related to hole accumulation as observed on Fig. 8 at t = 3 ps. Such electric field is not high enough to induce direct oxide failure [25] but can result, as discussed earlier, in charge injection within the oxide layer. This charge injection is likely to create latent defects in the oxide layer which may impact the long term reliability of the device during operation when a switching V_{GS} is applied.

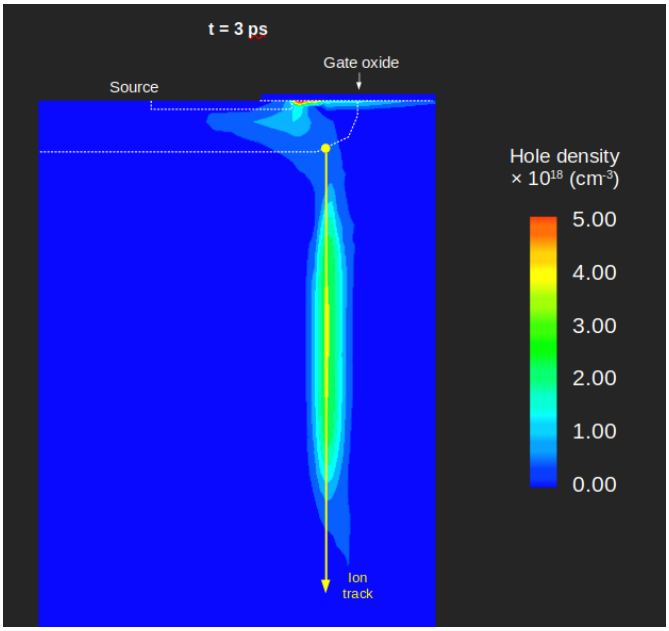

Fig. 8. Hole density after the ion impact. Holes are transported and accumulated at the gate oxide surface due to the electric field in the drift layer.

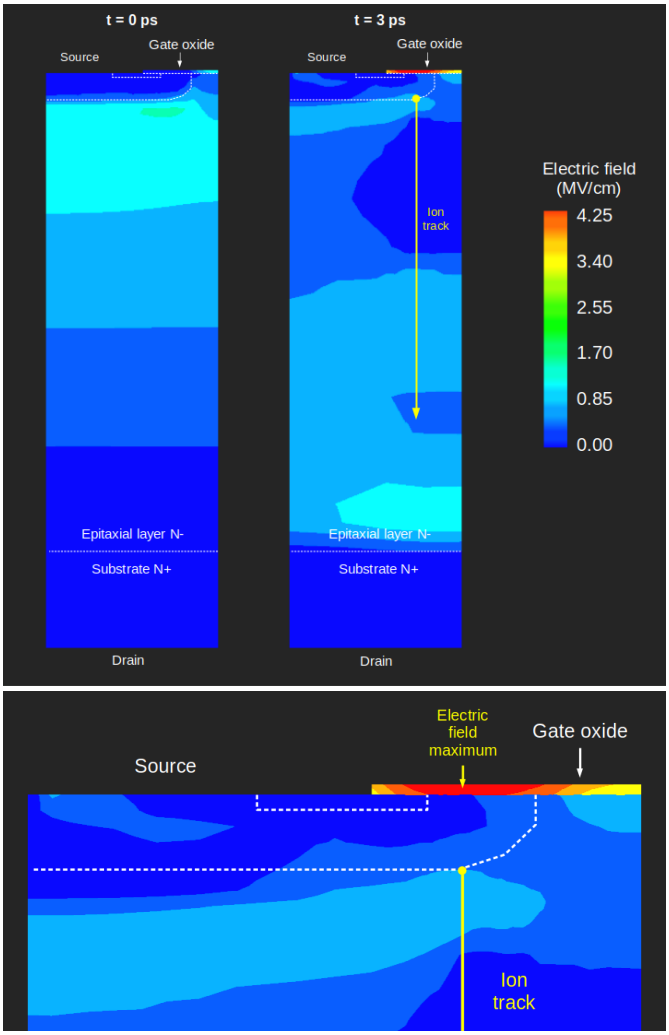

Fig. 9. Simulated electric field before (left) and after (right) the ion impact. Zoom in the gate oxide area with the maximum electric field location is presented in the bottom figure.

In order to assess the impact of applied gate voltage on the gate oxide degradation, TCAD simulations were performed for both V_{GS} = 0 V and V_{GS} = -4 V configurations. Simulated time evolution of electric field values in the gate oxide layer during the ion impact for V_{DS} = 675 V bias configuration are presented in Fig. 10. The measurement point is at the location where the electric field reached its maximum value (indicated in Fig. 9). It is important to note that this simulation study has focused on the impact of neutron-induced ion impact in the neck region of the SiC Power MOSFET. Indeed, the applied reverse bias on the gate will in this specific case enhance the electric field within the oxide layer compared to grounded gate configuration. Such behavior was expected since the electric field in the oxide during ion impact originates from holes accumulated under the gate oxide layer. Therefore, by applying negative voltage at the gate terminal, the difference in electrostatic potential across the oxide layer is increased. The maximum values of electric field transients for each voltage configuration have been plotted in Fig. 11, pointing out that such behavior might be expected whatever the V_{DS} value is applied. However, as will be shown in subsection D2b, the impact of V_{DS} far above the SOA may mask this post irradiation behavior by increasing the probability of SEB during irradiation as was observed in our experimental results.

b) The effect of gate degradation on SEB triggering

First, it has to be reported that TCAD simulations (not presented here) have been performed at the different V_{DS} values and for both V_{GS} configurations, grounded and reverse biased, in order to analyze the influence on overall transient drain current. Though it has been observed that the reverse gate bias was responsible for an increase of the electric field in the channel region close to the source contact due to hole accumulation, TCAD simulations did not allow to report an increase of the drain current with a negative gate voltage. This means that we cannot conclude that the SEB sensitivity is increased by the gate bias on top of the drain voltage. However, it also indicates that due to the location of hole accumulation close to the source region, there might be mutual effects between gate oxide degradation and subsequent SEB triggering. Moreover, such mutual effects are emphasized by the fact that at the irradiation fluence used during experiments, the mean number of n-Si or n-C interactions leading to secondary ions generation in each elementary cell is about 160 considering events of ≥ 100 fC generated charge. Such statistics has been estimated by using MC-ORACLE monte carlo code [26], calculating for the device geometry with a Rectangular Parallelepiped (RPP) approach the overall cross section of the irradiation facility neutron spectrum. Then multiplying the cross section by the fluence has given the number of events in the elementary cell. The critical charge of 100 fC was chosen since in TCAD simulations, it was observed to induce significant increase in gate oxide electric field during the event. It should be noted though, that compared to our test conditions, in atmospheric environment we should expect lower accumulated fluence during the device lifetime. However, based on the statistics obtained from MC-ORACLE simulation, we should still expect about 15 events per elementary cell in avionic applications.

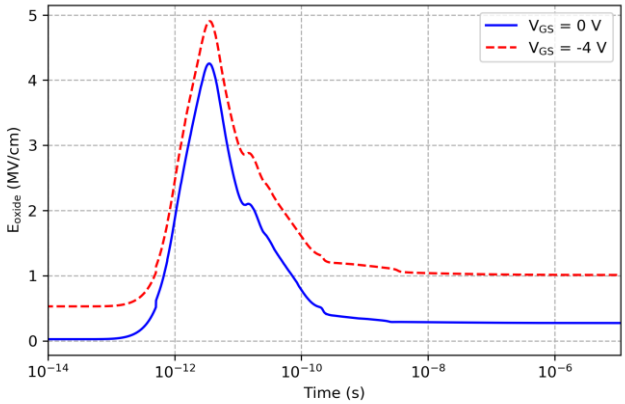

Fig. 10. Simulated time evolution of electric field in the gate oxide layer during the ion impact for V_{DS} = 675 V bias configuration. The applied reverse gate bias results in higher electric field in the oxide during the charge deposition in the device for an ion impact in the neck region.

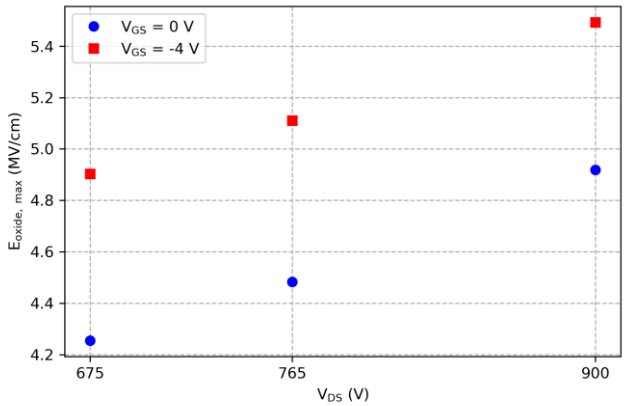

Fig. 11. Simulated maximum values of electric field transient in the oxide layer for different irradiation voltage configurations. For each V_{DS} configuration, maximum electric field value is higher when reverse gate bias is applied compared to grounded gate configuration.

Moreover, this number does not include neutron interactions generating less than 100 fC of charge, which also might contribute on the gate degradation.

Thus, starting from the observation that the neutron irradiation can induce several interactions in one elementary cell and that each time transient currents are able to be generated, the second part of the TCAD study focuses on the effect of degraded gate oxide on the SEB triggering. Since the degradation and increased gate leakage current does not imply the immediate device failure, we assume that devices which eventually exhibited SEB, could have suffered gate damage prior to SEB. For that purpose, we created a simulation model, in which the gate damage is modeled by replacing a small portion of the gate oxide with SiC material. Based on a recent publication for Si MOSFET [27], in our case we simulated the damage sites by creating a SiC path through the gate oxide layer just on the top of the source well (Fig. 12) which corresponds to the current behavior observed during PIGS test. With this simulated structure, the impact on SEB triggering of the injected charge through the gate is evaluated.

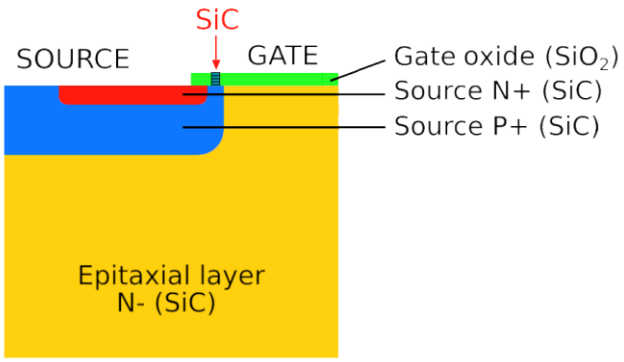

Fig. 12. Gate leakage current in TCAD simulation is modeled by replacing a portion of gate oxide with SiC material. Width of the region is 50 nm and n-doping density is 1×10^{14} cm^{-3}.

As reported as accurate parameters in previous studies [9], [28], simulated currents and impact ionization rates for the two simulation models (with non-degraded oxide and with gate oxide degradation) are respectively presented in Fig. 13 and in Fig. 14. Note that simulations were still performed under such ion energy conditions (reducing from 30 MeV to 20 MeV) that at the given position, no SEB was able to be triggered. Such simulation parameters have been chosen in order to determine if the localized oxide degradation might enhance the SEB triggering sensitivity. In Fig. 13, the global currents at the device terminals have been plotted as a function of time.

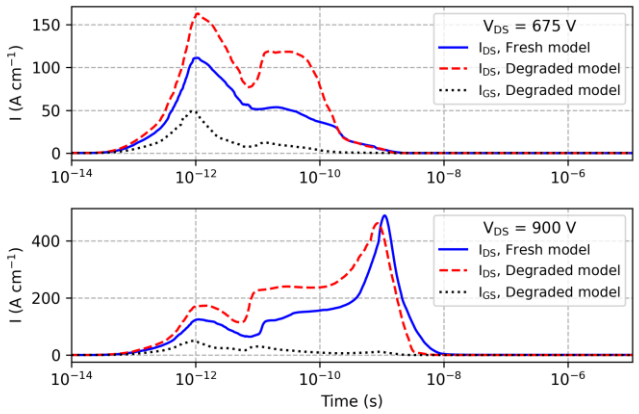

Fig. 13. Simulated time evolution of drain (I_{DS}) and absolute value of gate currents (I_{GS}) during the ion impact for two different irradiation V_{DS} configurations and for original model and model with degraded gate.

Comparing the drain current shapes between $V_{DS} = 675$ V and $V_{DS} = 900$ V, we confirm the fact that without any degradation in the oxide (Fresh models), a SEB might be triggered more likely at higher drain voltage. However, looking at the drain current transients at $V_{DS} = 675$ V for non-degraded oxides (Fresh model) and for degraded oxide model (Degraded model), a 50% increase in the first drain current peak value at t = 1 ps and a 100% increase in the sustained drain current value between 10 ps and 100 ps are observed. Considering then the higher drain bias configuration at $V_{DS} = 900$ V, the first I_{DS} peak value of the degraded model is still higher compared to the fresh model but the maximum value of the second drain current peak value in the sustained region at t = 1 ns is similar for both models.

Whatever the V_{DS}, one can note that the difference in the drain current values between the two models can originate from the current path through the gate oxide and resulting gate current, as shown in Fig. 13. However, this gate current contribution to the overall drain current takes only place in the very first picoseconds since the gate current recovers after this time dynamic. Looking at what happens in the sustained region, the degraded model shows a significant impact, especially for the lowest drain voltage value ($V_{DS} = 675$ V). This could indicate that the injected charge in the gate oxide and leading to a localized conductive path in the beginning of the event brings a contribution to the charge enhancement mechanism occurring later.

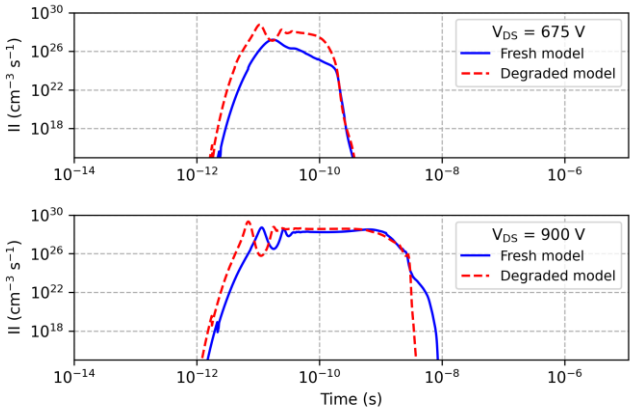

Fig. 14. Simulated impact ionization rates (II) during the ion impact for two different irradiation V_{DS} configurations and for two different simulation models.

This is confirmed in Fig. 14 where the maximum impact ionization rates at the epitaxial layer/drain (N-/N+) interface are reported. In particular, the difference in impact ionization rates between the fresh and degraded models is much more significant for $V_{DS} = 675$ V configuration whereas for the $V_{DS} = 900$ V configuration, the simulated impact ionization rate difference is almost non-existent. From these TCAD simulation results, we have shown that the contribution of the reverse gate bias is significant for bias close to the SOA. Furthermore, we reported that if at high V_{DS} values (far above the SOA limit), the single contribution of the internal drain to source electric field dominates the SEB triggering, this is not the case for lower bias configurations close to the SOA. Indeed, in the experimental section, an enhanced sensitivity to SEB for the reverse gate biased has been reported for the lowest V_{DS} value. We have brought up a physical understanding using a phenomenological conductive path model for the oxide degradation in the TCAD simulation section. Thus, we have concluded that for bias configurations close to the SOA, the reverse gate bias might result in charge injection, contributing to higher drain current transients and higher impact ionization rates, favoring finally the SEB mechanism.

IV. Conclusion

Gate voltage dependence on failure rate of SiC power MOSFETs under neutron irradiation is investigated. We address in this paper the contribution of the reverse gate bias on the risk of failure, in particular at lower V_{DS}, closer to the safe operating area (SOA) limit. For SEB failed device, failure analysis at wafer level supported by current behavior after the failure event revealed the material failure at the gate/oxide region.

In the meantime, latent gate damages were revealed by post-irradiation gate stress on irradiated devices having not suffered a SEB. Increased post-irradiation gate leakage current were observed. Using TCAD simulations, an accumulation of carriers (holes) has been observed in the channel region below the oxide layer and close to the source contact, suggesting some similar mechanisms to the ones involved in SEGR. Such latent damages are expected to be more severe when additional negative gate bias is applied since the hole accumulation below the oxide has been shown to be enhanced with a negative gate bias. Based on the statistics of neutron interactions into a single cell during our experiments obtained using MC-Oracle, Monte Carlo calculation tools, we demonstrated that the applied negative V_{GS} will affect the probability of gate degradation and therefore the SEB failure rate of a last generation SiC device under neutron environment. Such result is particularly to be considered when the device is integrated into a system for example in a switching power converter, where for power yield considerations, a negative gate bias is often used by designers.

Acknowledgements

Authors would like to thank Maria Kastriotou and Carlo Cazzaniga from ChipIr facility for their help during the experiments.

References

[1] D. L. Oberg, L. L. Wert, E. Normand, P. P. Majewski, and S. A. Wender, "First observations of power MOSFET burnout with high energy neutrons," *IEEE Trans. Nucl. Sci.*, vol. 43, no. 6 PART 1, pp. 2913–2920, Dec. 1996.

[2] E. Normand, J. L. J. L. Wert, D. L. D. L. Oberg, P. P. P. Majewski, P. Voss, and S. A. Wender, "Neutron-induced single event burnout in high voltage electronics," *IEEE Trans. Nucl. Sci.*, vol. 44, no. 6 PART 1, pp. 2358–2366, Dec. 1997.

[3] D. J. Lichtenwalner, A. Akturk, J. McGarrity, J. Richmond, T. Barbieri, B. Hull, D. Grider, S. Allen, and J. W. Palmour, "Reliability of SiC power devices against cosmic ray neutron single-event burnout," *Mater. Sci. Forum*, vol. 924 MSF, pp. 559–562, Jun. 2018.

[4] A. Akturk, J. M. McGarrity, N. Goldsman, D. Lichtenwalner, B. Hull, D. Grider, and R. Wilkins, "Terrestrial Neutron-Induced Failures in Silicon Carbide Power MOSFETs and Diodes," *IEEE Trans. Nucl. Sci.*, vol. 65, no. 6, pp. 1248–1254, Jun. 2018.

[5] A. Akturk, R. Wilkins, J. McGarrity, and B. Gersey, "Single Event Effects in Si and SiC Power MOSFETs Due to Terrestrial Neutrons," *IEEE Trans. Nucl. Sci.*, vol. 64, no. 1, pp. 529–535, Jan. 2017.

[6] D. R. Ball, B. D. Sierawski, K. F. Galloway, L. Fellow, R. A. Johnson, M. L. Alles, A. L. Sternberg, A. F. Witulski, R. A. Reed, R. D. Schrimpf, A. Javanainen, J. Lauenstein, M. Carlo, and M. Carlo, "Estimating Terrestrial Neutron-Induced SEB Cross Sections and FIT Rates for High-Voltage SiC Power MOSFETs," *IEEE Trans. Nucl. Sci.*, vol. 66, no. 1, pp. 337–343, Jan. 2019.

[7] H. Asai, I. Nashiyama, K. Sugimoto, K. Shiba, Y. Sakaide, Y. Ishimaru, Y. Okazaki, K. Noguchi, and T. Morimura, "Tolerance against terrestrial neutron-induced single-event burnout in SiC MOSFETs," *IEEE Trans. Nucl. Sci.*, vol. 61, no. 6, pp. 3109–3114, Dec. 2014.

[8] E. Mizuta, S. Kuboyama, H. Abe, Y. Iwata, and T. Tamura, "Investigation of single-event damages on silicon carbide (SiC) power MOSFETs," *IEEE Trans. Nucl. Sci.*, vol. 61, no. 4, pp. 1924–1928, Aug. 2014.

[9] A. F. Witulski, D. R. Ball, K. F. Galloway, A. Javanainen, J. M. Lauenstein, A. L. Sternberg, and R. D. Schrimpf, "Single-Event Burnout Mechanisms in SiC Power MOSFETs," *IEEE Trans. Nucl. Sci.*, vol. 65, no. 8, pp. 1951–1955, Aug. 2018.

[10] L. L. Foro, A. D. Touboul, A. Michez, F. Wrobel, P. Rech, L. Dilillo, C. Frost, and F. Saigné, "Gate voltage contribution to neutron-induced seb of trench gate fieldstop IGBT," *IEEE Trans. Nucl. Sci.*, vol. 61, no. 4, pp. 1739–1746, Aug. 2014.

[11] A. Hands, P. Morris, K. Ryden, C. Dyer, P. Truscott, A. Chugg, and S. Parker, "Single event effects in power MOSFETs due to atmospheric and thermal neutrons," *IEEE Trans. Nucl. Sci.*, vol. 58, no. 6 PART 1, pp. 2687–2694, Dec. 2011.

[12] S. Liu, J. L. Titus, C. Dicienzo, H. Cao, M. Zafrani, M. Boden, and R. Berberian, "Recommended test conditions for SEB evaluation of planar power DMOSFETs," *IEEE Trans. Nucl. Sci.*, vol. 55, no. 6, pp. 3122–3129, Dec. 2008.

[13] M. Deki, T. Makino, K. Kojima, T. Tomita, and T. Ohshima, "Single event gate rupture in SiC MOS capacitors with different gate oxide thicknesses," *Mater. Sci. Forum*, vol. 778–780, pp. 440–443, Feb. 2014.

[14] "CRD-60DD12N 60kW Interleaved Boost Converter, Application Note."

[15] "ChipIr facility website." [Online]. Available: https://www.isis.stfc.ac.uk/Pages/ChipIR.aspx. [Accessed: 13-Nov-2020].

[16] "Test Method Standard," *MIL-STD-750E*, 1996.

[17] R. B. Abernethy, *The new Weibull handbook : Reliability & statistical analysis for predicting life, safety, survivability, risk, cost and warranty claims*, 5th ed. North Palm Beach, USA: Robert B. Abernethy, 1996.

[18] M. Reid, "Reliability – a Python library for reliability engineering." 2020.

[19] K. Niskanen, A. D. Touboul, R. C. Germanicus, A. Michez, A. Javanainen, F. Wrobel, J. Boch, V. Pouget, and F. Saigné, "Impact of electrical stress and neutron irradiation on reliability of silicon carbide power MOSFET," *IEEE Trans. Nucl. Sci.*, vol. 67, no. 7, pp. 1365–1373, Jul. 2020.

[20] T. Shoji, S. Nishida, K. Hamada, and H. Tadano, "Analysis of neutron-induced single-event burnout in SiC power MOSFETs," *Microelectron. Reliab.*, vol. 55, no. 9–10, pp. 1517–1521, Jun. 2015.

[21] C. Martinella, R. Stark, T. Ziemann, R. G. Alia, Y. Kadi, U. Grossner, and A. Javanainen, "Current Transport Mechanism for Heavy-Ion Degraded SiC MOSFETs," *IEEE Trans. Nucl. Sci.*, vol. 66, no. 7, pp. 1702–1709, Jul. 2019.

[22] C. Abbate, G. Busatto, D. Tedesco, A. Sanseverino, F. Velardi, and J. Wyss, "Gate damages induced in SiC power MOSFETs during heavy-ion irradiation-Part I," *IEEE Trans. Electron Devices*, vol. 66, no. 10, pp. 4243–4250, 2019.

[23] A. Michez, S. Dhombres, and J. Boch, "ECORCE: A TCAD Tool for Total Ionizing Dose and Single Event Effect Modeling," *IEEE Trans. Nucl. Sci.*, vol. 62, no. 4, pp. 1516–1527, Aug. 2015.

[24] M. Allenspach, J. R. Brews, I. Mouret, R. D. Schrimpf, and K. F. Galloway, "Evaluation of SEGR Threshold in Power MOSFETs," *IEEE Trans. Nucl. Sci.*, vol. 41, no. 6, pp. 2160–2166, Dec. 1994.

[25] M. Deki, T. Makino, K. Kojima, T. Tomita, and T. Ohshima, "Instability of critical electric field in gate oxide film of heavy ion irradiated SiC MOSFETs," *Mater. Sci. Forum*, vol. 821–823, pp. 673–676, Jun. 2015.

[26] F. Wrobel and F. Saigné, "MC-ORACLE : A tool for predicting Soft Error Rate," *Comput. Phys. Commun.*, vol. 182, no. 2, pp. 317–321, Oct. 2011.

[27] S. Kuboyama, E. Mizuta, Y. Nakada, and H. Shindou, "Physical Analysis of Damage Sites Introduced by SEGR in Silicon Vertical Power MOSFETs and Implications for Postirradiation Gate-Stress Test," *IEEE Trans. Nucl. Sci.*, vol. 66, no. 7, pp. 1710–1714, Jul. 2019.

[28] S. Kuboyama, E. Mizuta, Y. Nakada, H. Shindou, A. Michez, J. Boch, F. Saigne, and A. Touboul, "Thermal Runaway in SiC Schottky Barrier Diodes Caused by Heavy Ions," *IEEE Trans. Nucl. Sci.*, vol. 66, no. 7, pp. 1688–1693, Jul. 2019.