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**Abstract:** The paper investigates the management of drain voltage and current slew rates (i.e., dv/dt and di/dt) of high-speed GaN-based power switches during the transitions. An active gate voltage control (AGVC) is considered for improving the safe operation of a switching cell. In an application of open-loop AGVC, the switching speeds vary significantly with the operating point of the GaN HEMT on either or both current and temperature. A closed-loop AGVC is proposed to operate the switches at a constant speed over different operating points. In order to evaluate the reduction in the electromagnetic disturbances, the common mode currents in the system were compared using the active and a standard gate voltage control (SGVC). The closed-loop analysis carried out in this paper has shown that discrete component-based design can introduce limitations to fully resolve the problem of high switching speeds. To ensure effective control of the switching operations, a response time fewer than 10 ns is required for this uncomplex closed-loop technique despite an increase in switching losses.

**Keywords:** GaN HEMT; active voltage gate control; slew rate; manage switching speed; EMI



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## 1. Introduction

Very high frequency operation capabilities of wide band-gap semiconductor devices (such as GaN and SiC) made them good candidates for high efficiency of static converter [1–5]. However, the safe operation of the devices in converters degrades during very fast transitions of both current and voltage [6–8]. Most commonly, passive control techniques are used in managing transitions [9–14]. The methods applied in passive control adjust either/or both the gate resistance and the parasitic gate capacitance of a transistor. One of the main disadvantages of passive control is a lack of compensation against the variations of the current and voltage parameters of the converter, which, therefore, increase switching losses. An open-loop passive control technique is presented in References [15–17] to mitigate this issue. In this technique, the switching process has been divided into several sequences while introducing a passive element for each sequence. Compared to the basic methods, this open-loop method reduces the losses. However, additional losses remain significant since the open-loop passive controls are unable to compensate for the variation in the converter parameters.

A closed-loop active driver for silicon-based IGBTs (Insulate Gate Bipolar Transistor) and MOSFETs (Metal Oxide Semiconductor Field Effect Transistor) has been proposed in References [17–20]. The active driver circuit in Reference [19] presented the current

transient (di/dt) control of an IGBT, based on a 50-nH common parasitic inductance between the power and the control paths. For GaN-based designs, the introduction of such a parasitic value is unacceptable as the parasitic transients can damage the device during fast transitions. An active closed-loop control based on a capacitor lower than 20 nF has been proposed for a GaN HEMT (High Electron Mobility Transistor) in References [21,22]. However, this technique under-utilized the fast switching capability of the GaN HEMTs as it used a switching speed lower than that of an Si-based MOSFET or IGBT.

In all those GaN transistor-based solutions, discrete components and complex circuits were used to solve the issue of high-speed switches. In this paper, we are proposing a less complex closed-loop to manage potential limits of switching speed. The evaluation of this discrete component-based circuit can be used to determine the response time, switching speed, and the losses. Furthermore, we determined the limitations of the AGVC (Active Gate Voltage Control) technique built using a discrete component to control switching speed of a GaN HEMT.

Firstly, a study of an analysis of active gate drive techniques for GaN power transistors is summarized. The mathematical analysis for switching speeds is discussed in Section 2. Section 4 details a proposal of an open-loop active gate voltage control (AGVC) technique. By addressing the issues in the open-loop approach, a new closed-loop control technique is introduced in Section 5. Finally, Section 6 concludes by summarizing the findings.

## 2. Open-Loop Active Gate Voltage Control during Turn-On

Figure 1 illustrates a schematic diagram of a simple switching cell in a buck configuration. The fluctuations in drain voltage and current slew rates (dv/dt and di/dt) are due to the fast switching operation of the converter. GaN-based switch designs are more sensitive to these fluctuations. Besides, they depend on (i) the transistor parameters: threshold voltage (Vth), gate-drain capacitance ($C_{gd}$), gate-source capacitance ($C_{gs}$), and the gain ($g_m$), (ii) the characteristics of the driver: output voltage ($V_{gr}$) and gate current ($I_g$) of the driver, and (iii) passive elements of the gate control circuit ($R_g$ and $L_S$) [20–22]. The transition current during turn-on of the GaN transistor is given by Equation (1):

$$\frac{di_{d,on}}{dt} = \frac{g_m\left(V_{grmax} - V_{th}\right)}{R_g\left(C_{gd} - C_{gs}\right) + g_m \cdot L_S} \quad (1)$$

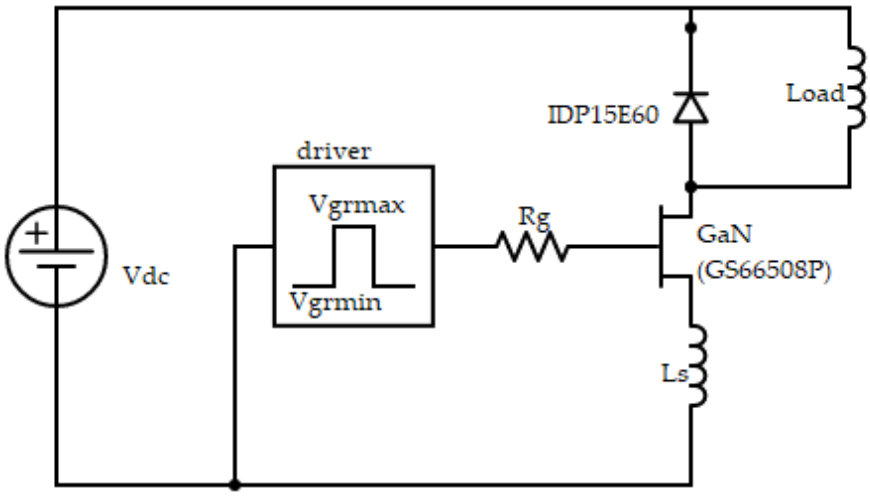



**Figure 1.** A simplified schematic of a transistor/diode switching cell in a buck configuration.

The reduction in the switching speed can be carried out by two methods: passive or active control of the gate drive. In general, the passive method is achieved by adjusting the passive elements of the driver loop ($R_g$ or and $C_{gd}$). The high losses generated by these

elements are one of the drawbacks that make the passive control method less interesting. The active control method is achieved by adjusting the electrical parameters of the driver such as the maximum gate supply voltage ($V_{grmax}$) and the gate maximum current ($I_{gmax}$). This second approach is superior to the first in terms of low power losses. As per Equation (1), the difference between $V_{grmax}$ and $V_{th}$ will be at its highest to maximize the current slew rate during turn-on. In order to reduce the high-speed of dv/dt and or di/dt of the GaN switch, an AGVC can adjust the gate driver supply voltage $V_{gr}$ dynamically. The proposed AGVC is a modified version of the originally developed technique in Reference [17] for IGBT transistors, which addresses switching speed 10 times slower than the one of a GaN device.

The proposed technique controls the transistor gate with an intermediate voltage $V_{grmin}$ ($V_{grmin} < V_{grint} < V_{grmax}$) close to $V_{th}$ for a duration of $t_{int}$ (during the switching phase of current). Once the switching of current is completed, a nominal voltage level $V_{grmax}$ controls the transistor during switching of the voltage in order to minimize the turn-on power losses. Figure 2 shows the typical gate driver signals that address the issue of the current curve during the turn-on for both AGVC and standard gate voltage control (SGVC) strategies. Figure 3 shows two gate drive circuit configurations of an AGVC strategy. A brief description of an experimental validation of the two configurations in GaN HEMT-based circuit is described in the next section. Furthermore, a well-explained content of the operating principles and the advantages and disadvantages of the two configurations can be found in Reference [22].

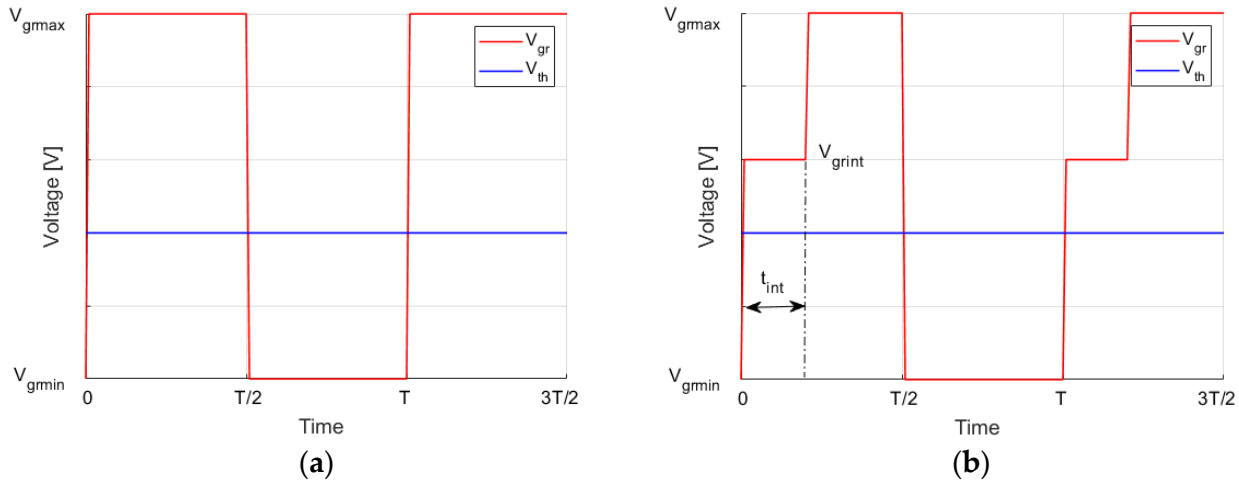



**Figure 2.** Typical gate driver signals: (**a**) standard two stage gate-drive control signal, (**b**) di/dt turn-on control using AGVC.

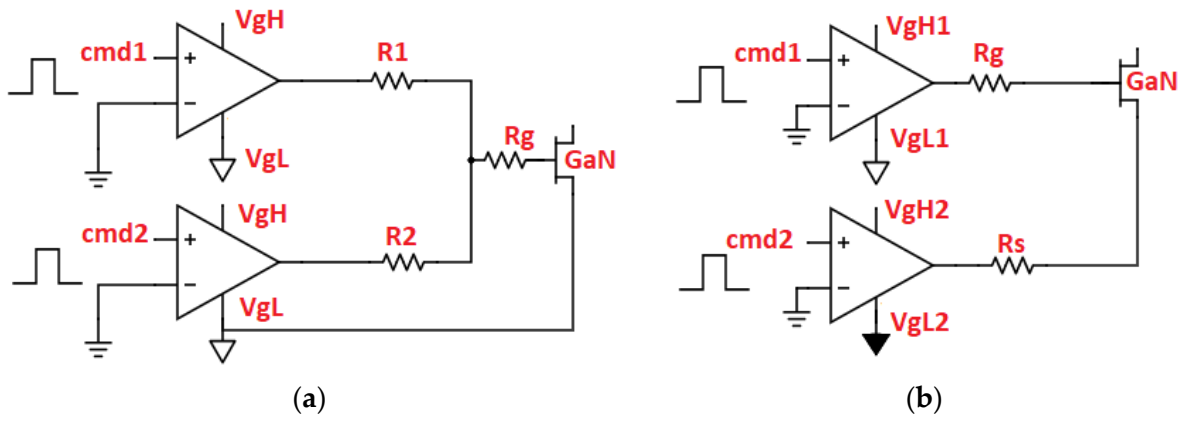



**Figure 3.** Possible gate drive circuit configurations for AGVC: (**a**) configuration-1 with a common-voltage at the source, (**b**) configuration-2 with a varying voltage at the source.

## 3. Experimental Setup and Results for AGVC Open-Loop Control

To evaluate the interests of the active gate-voltage control, the circuit in Figure 1 was used as the test prototype (the gate driver circuit configuration-2 in Figure 3 was built using two SI8261ABC drivers from Silicon Labs) [23]. The diver has a minimum supply voltage of 6.5 V (high-to-low > 6.5 V), which limits the application to the GS66508P as it can easily exceed the absolute gate voltage limit of 7 V in the continuous mode [24]. Since the converter was tested in a pulsed mode, the GaN HEMT can be well controlled under 10 V (pulsed limit voltage) without any damage. For the continuous mode of operation, the SI8261ABC driver is not recommended. The experimental setup and the converter prototype are shown in Figure 4. Figures 5–10 illustrate the experimental results of AGVC-based design and a comparison of the SGVC results obtained during turn-on.

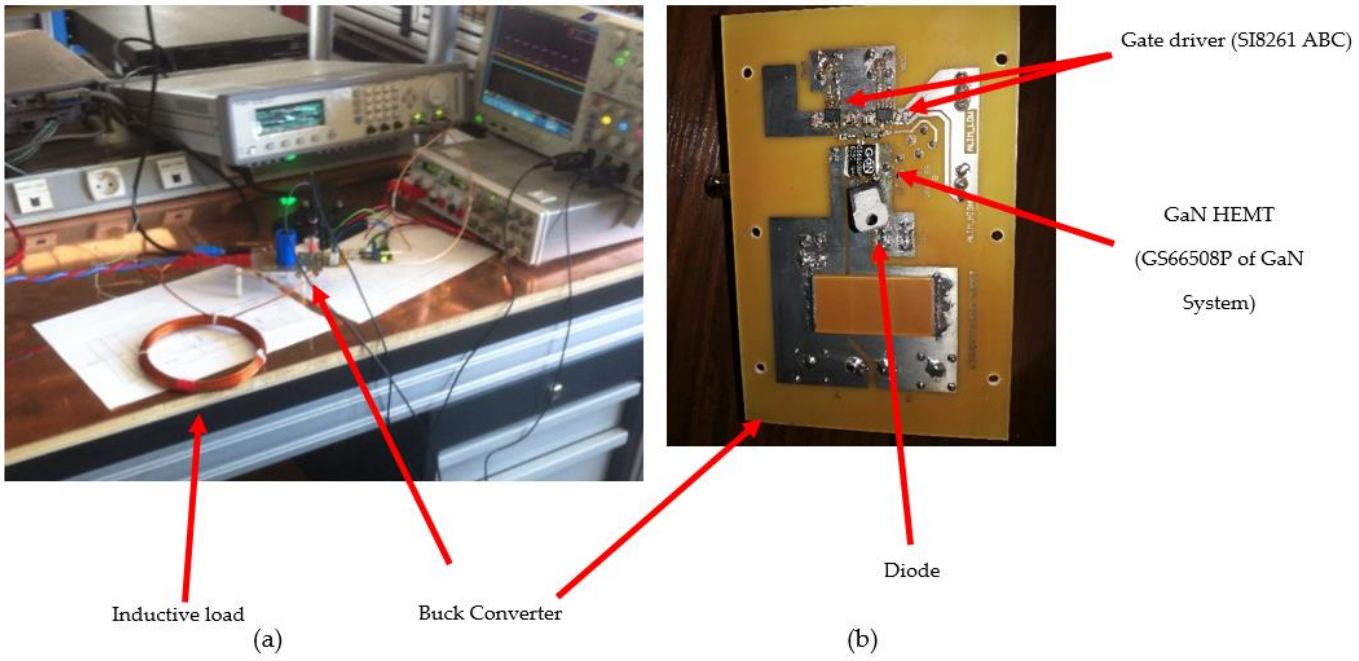



**Figure 4.** (**a**) Test setup and (**b**) the prototype.

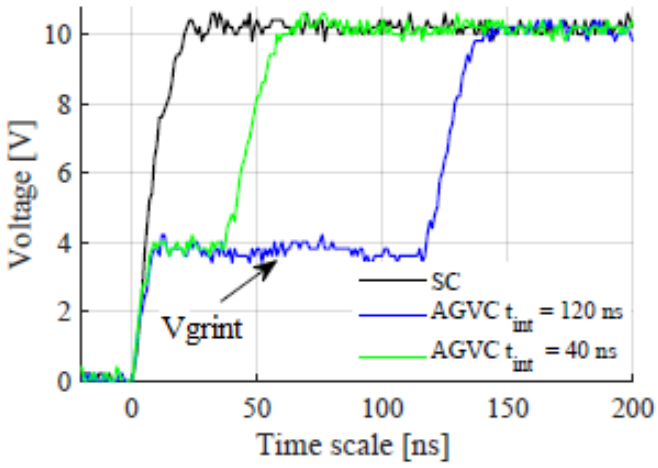
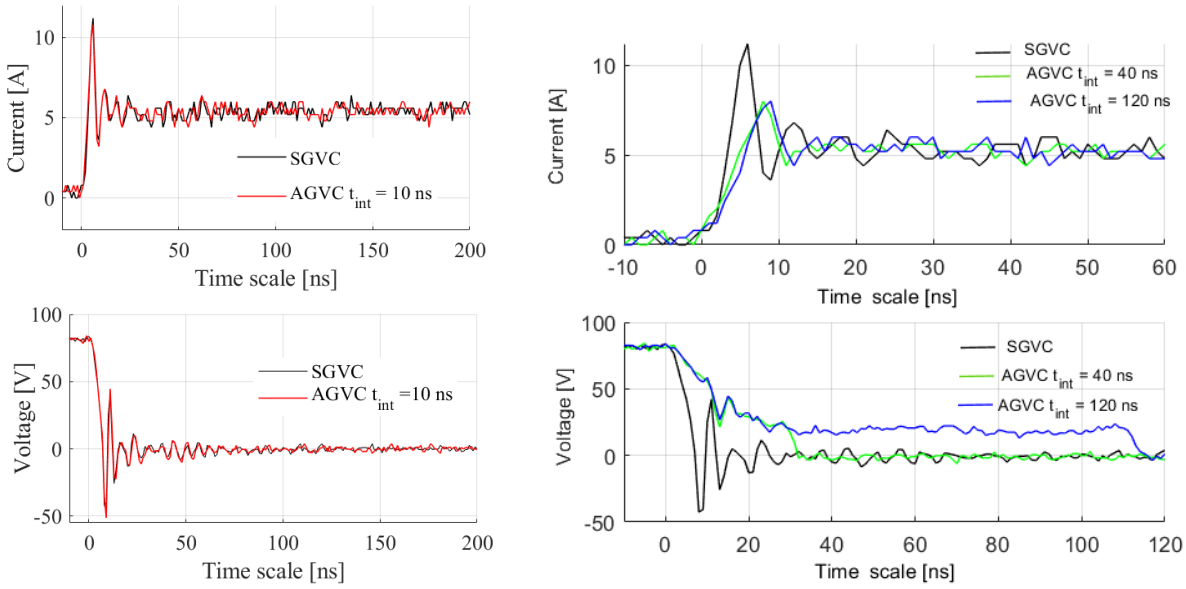
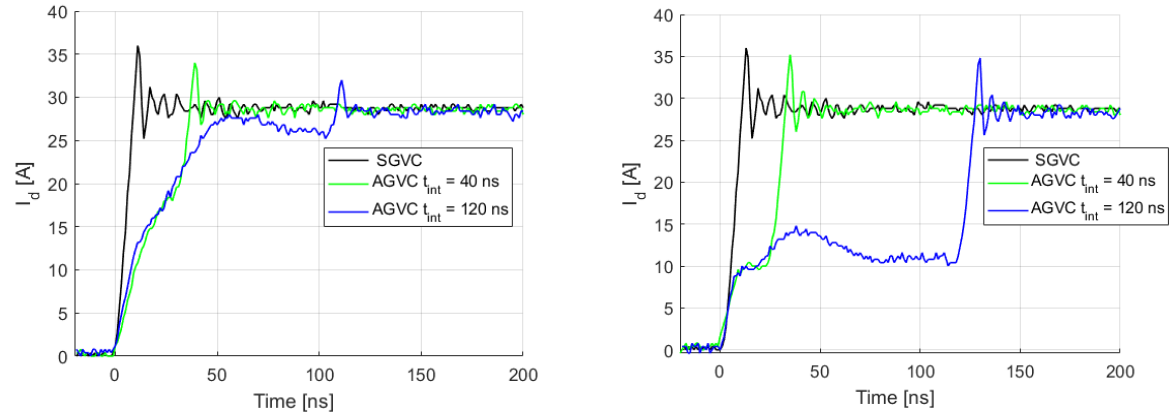



**Figure 5.** $V_{gs}$ waveforms ($R_g$ = 3 Ω and $V_{grint}$ = 4 V).



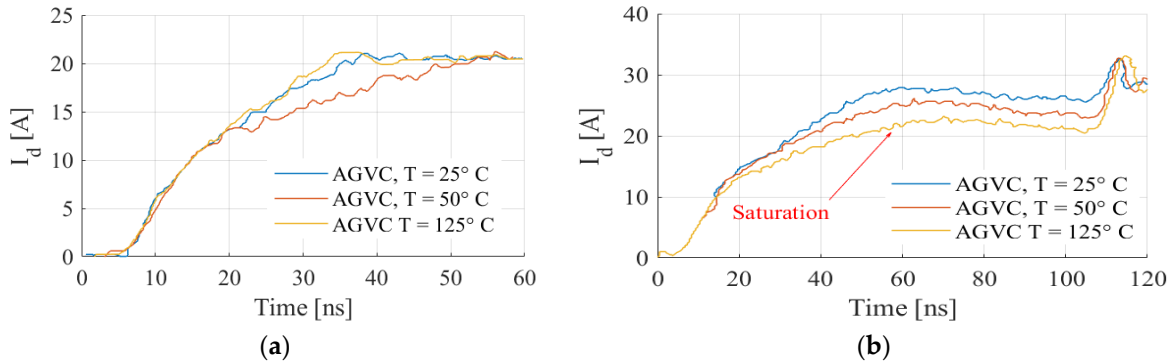

(**a**) (**b**)

**Figure 6.** $V_{ds}$ and $I_d$ waveforms depending on parameter tint of AGVC (current load 5 A, $R_g$ = 3 Ω and $V_{grint}$ = 4 V): (**a**) low $t_{int}$ ($t_{int}$ = 10 ns), (**b**) high $t_{int}$ ($t_{int}$ > 10 ns).




(**a**) (**b**)

**Figure 7.** Current waveforms during turn-on using AGVC for different load current values and different tint values. (**a**) $V_{grint}$ = 4 V, (**b**) $V_{grint}$ = 3.5 V.




(**a**) (**b**)

**Figure 8.** Drain current waveforms during turn-on for different temperature values ($R_g$= 3 Ω and $V_{grint}$ = 4 V, $t_{int}$ = 120 ns) (**a**) $I_d$ = 20 A, (**b**) $I_d$ = 28 A.

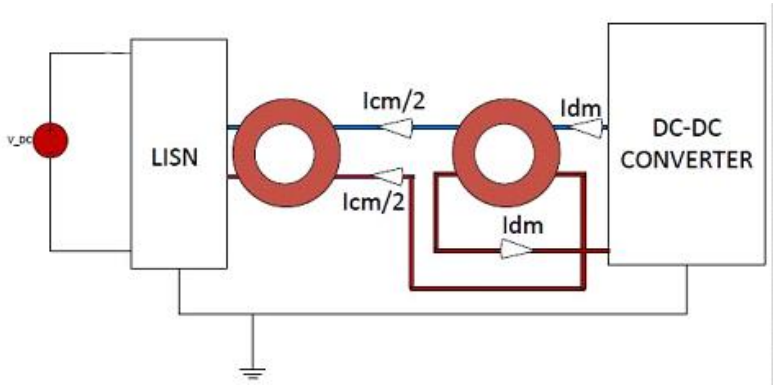



**Figure 9.** Test bench for conducted emission measurements with current probes.

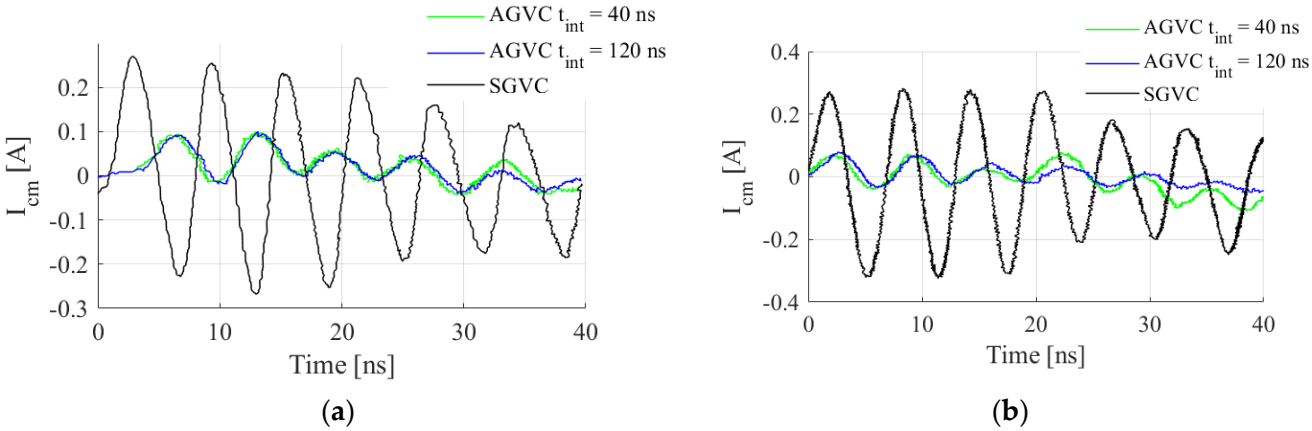



**Figure 10.** Common mode current ($I_{cm}$) during turn-on for $R_g$ = 3 Ω, $V_{grint}$ = 4 V, and Vdc = 50 V, (**a**) $I_d$ = 2 A, (**b**) $I_d$ = 6 A.

## 4. Experimental Results with an Open-Loop Active Gate Voltage Control

### *4.1. Parameter $t_{int}$*

To assess the impact of $t_{int}$ in the AGVC voltage pattern, two cases were tested using the GS66508P GaN transistor with $V_{th}$ = 1.2 V. In the first case, an intermediate voltage of 4 V ($V_{grint}$ = 4 V) was applied for a very short duration of $t_{int}$ ($t_{int} \leq 10$ ns). For the second case, the voltage $V_{grint}$ is applied for a longer time ($t_{int} > 10$ ns). Figure 6 compares the results of the two cases.

As seen in the results, the signals obtained with the SGVC and the AGVC for a duration of $t_{int}$ of 10 ns are identical, which implies the AGVC gate voltage cannot slow down di/dt for a short duration of $t_{int}$ ($t_{int} < 10$ ns) of a GaN transistor (Figure 6a). The long response time of the driver (SI8261ABC) can be the main cause of the impossibility of being able to slow the di/dt of the GaN transistor when applying the AGVC technique.

With an increase in the duration of $t_{int}$, the AGVC slow down the di/dt because the drain current takes more time than the SGVC to reach the load current (Figure 6b). For low load currents ($I_{Load}$ = 5 A), the same di/dt is obtained with a $t_{int}$ of 40 ns and a tint of 120 ns ($I_d$ of Figure 6b). However, they do not have the same impact on the switching speed of the voltage. The larger the $t_{int}$ (120 ns), the greater the effect on the dv/dt ($V_{ds}$ in Figure 6b). To reduce conduction losses, it is essential to minimize the $t_{int}$ dependent effect on the dv/dt when applying AGVC.

Due to the operation of the GaN transistor in the linear zone (during the turn-on switching phase), the application of a long $t_{int}$ (120 ns) can also have other negative consequences. As illustrated as a red arrow of Figures 7b and 8, an appearance of the saturation phenomenon occurred in high load currents. Because, during the application of the intermediate voltage ($V_{grint}$), the transistor has reached its maximum current for the

given $V_{grint}$. In order to avoid the generation of additional losses due to the saturation phenomenon, the value of $t_{int}$ must be optimized. A closed-loop AGVC can be applied to optimize the value of $t_{int}$, which corresponds to the moment when the drain current $i_d$ reached its final value (load current). Furthermore, the saturation current increases with the increase in $V_{grint}$ (Figure 7a) whereas it decreases with increasing temperature (Figure 8). The GaN characteristics deteriorate with the increase in temperature. As can be seen in Figure 8, the increase in temperature also causes a decrease in di/dt obtained with the AGVC action (Figure 8a). To limit these negative effects, a closed-loop control requires adjusting $t_{int}$ and $V_{grint}$ dynamically for each operating point.

### *4.2. Switching Losses during Turn-On*

A comparison of the energy losses and variations in di/dt among the applications of AGVC and SGVC are summarized in Table 1. The di/dt varies from 2.5 A/ns to 0.5 A/ns with the application of AGVC (with 4 V of $V_{grint}$ during 40 ns of tint). When the $t_{int}$ value increases to 120 ns, similar di/dt can be obtained, but the losses are increasing. To approach a similar di/dt (0.8 A/ns) using the SGVC ($R_g$ is 39 Ω), the losses are even more prominent than those obtained using the AGVC with $V_{grint}$ being 4 V and $t_{int}$ being 40 ns.

**Table 1.** Comparison of energy losses using AGCV and standard gate control with load current without saturation ($I_d$ = 5 A).

| | **di/dt [A/ns]** | **dv/dt [V/ns]** | **$E_{on}$ [µJ]** |
|---|---|---|---|
| AGVC ($R_g$ = 3 Ω and $t_{int}$ = 40 ns) | 0.8 | −2.6 | 6.6 |
| AGVC ($R_g$ = 3 Ω and $t_{int}$ = 120 ns) | 0.8 | −0.74 | 14 |
| Standard gate voltage control ($R_g$ = 3 Ω) | 1.5 | −1.8 | 2.6 |
| Standard gate voltage control ($R_g$ = 39 Ω) | 0.6 | −1.8 | 13 |

As seen in Table 2, the extra losses introduced in AGVC are less important than those related to the SGVC ($R_g$ = 39 Ω) when the saturation phenomenon occurs. However, the AGVC is less advantageous in the case of large tint due to the high impact on dv/dt.

**Table 2.** Comparison of energy losses using AGCV and standard gate control with load current without saturation ($I_d$ = 28 A).

| | **di/dt [A/ns]** | **dv/dt [V/ns]** | **$E_{on}$ [µJ]** |
|---|---|---|---|
| AGVC ($R_g$ = 3 Ω and $t_{int}$ = 40 ns) | 0.84 | −3 | 39 |
| AGVC ($R_g$ = 3 Ω and $t_{int}$ = 120 ns) | 0.48 | −0.9 | 189 |
| Standard gate voltage control ($R_g$ = 3 Ω) | 3.2 | −10.8 | 12 |
| Standard gate voltage control ($R_g$ = 39 Ω) | 1.2 | −0.7 | 50 |

### *4.3. Impact of AGCV on Conducted Electromagnetic Disturbances*

The results obtained in the previous parts imply that it is possible to slow down the GaN switching speeds at turn-on with AGVC. GaN high switching speed and high-frequency operation generate oscillations in common mode current waveforms that AGVC may help attenuate. Oscillations introduce conducted disturbances that are studied in time and frequency domains using the test bench illustrated in Figure 9. In these experiments, the common mode current ($I_{cm}$) and the differential mode current are measured using magnetic probes (Pearson current monitor model 6595). Figures 10 and 11 show the experimental results.

The reduction of the di/dt obtained with AGVC allows attenuating the common mode currents compared to that of the SGVC (Figure 10). The variation of the di/dt caused by the variation of the drain current (current from 2 A to 6 A), causes an increase in $I_{cm}$ from 20 ns for a tint of 40 ns and a current of 6 A (Figure 10b) compared for the same tint but for a current of 2 A (Figure 10a). These analyses confirm the conclusions concerning the need to set up a closed-loop control in order to keep the di/dt constant, allowing to have a

constant $I_{cm}$ current. Regarding the oscillation frequency, the AGVC has no impact. This is the reason why the two peaks observed in the frequency domain with the two controls (AGVC and SGVC) occur at the same frequency (175 MHz and 600 MHz). A reduction of 20 dBµA is obtained with the AGVC for a tint of 120 ns.

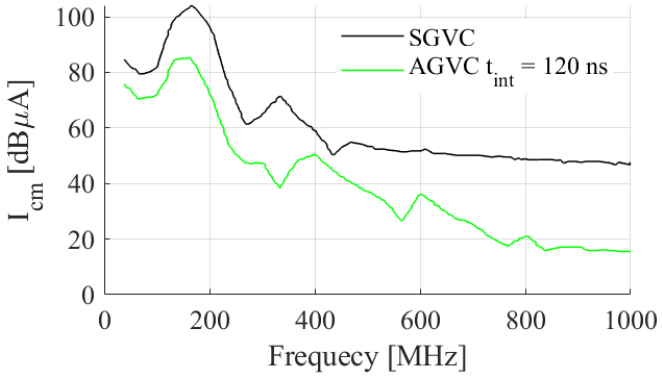



**Figure 11.** Common mode current ($I_{cm}$) during turn-on in a frequency domain for load current of 6 A, Rg = 3 Ω, $V_{grint}$ = 4 V, and Vdc = 50 V.

## 5. Closed-Loop Active Gate Voltage Control

In the AGVC, di/dt and dv/dt vary with the operating point of the transistor and the power converter parameters. To overcome these issues, a closed-loop AGVC can be applied.

### *5.1. Closed-Loop AGVC with Common Source Parasitic Inductance during Turn-On*

The closed-loop control uses the configuration-1 of the AGVC structure in Figure 3. The voltage $V_{Ls}$ created by the drain current during turn-on is used to control the driver 2 (Drv2) (Figure 12). At the beginning of the turn-on (t = [0 $t_1$]), the drain current $I_d$ is zero as $V_{gs}$ is less than $V_{th}$, and the voltage at the terminal of $L_s$ ($V_{Ls}$) is zero. Since the signal related to $L_s$ is connected to the inverse input of driver-2. The control voltage of the GaN transistor is the output voltage of the driver-1 (the output of the driver-2 being in the high-impedance state for $V_{Ls}$ is 0).

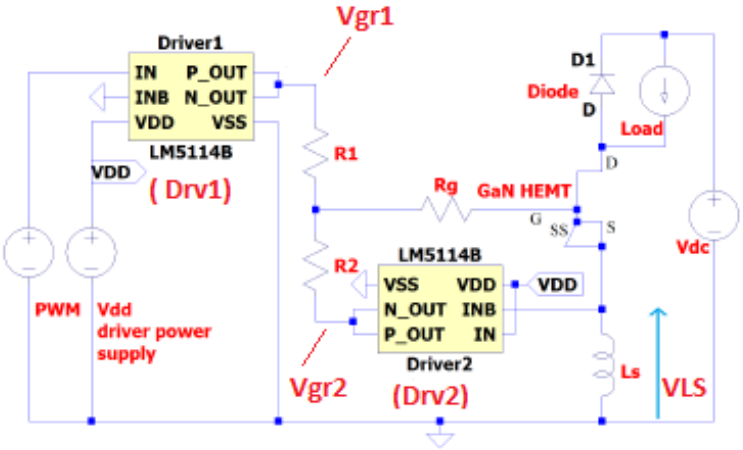



**Figure 12.** Schematic diagram of the proposed closed-loop AGVC using a common source parasitic inductance ($L_s$).

The output voltage of the driver-1 ($V_{gr1}$) will increase until reaching the threshold voltage of the GaN ($V_{th}$) at $t_1$, which causes a positive variation of the drain current and, thereby, the positive variation of $V_{Ls}$ ($V_{Ls}$ > 0 V) (Figure 13). Depending on the peak value ($V_{Lsmax}$ and its duration ($t_{VLs}$), four cases are possible, but only one has an effect on di/dt.

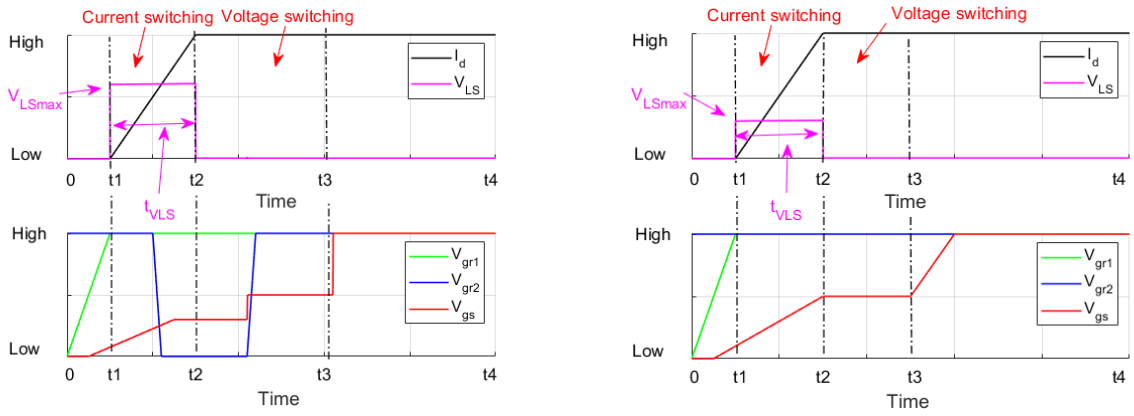



**Figure 13.** Simulated signals of the proposed circuit: (**a**) case 1, (**b**) case 2.

When the maximum value ($V_{Lsmax}$ of $V_{Ls}$ is larger than the minimum input voltage of the driver-2 (2.5 V) with a sufficient duration of the $t_{VLs}$, the output of the driver-2 ($V_{gr2}$) reaches the low state that will allow controlling the GaN device with an intermediate gate voltage ($V_{grint}$). This will slow down the switching speed of the current (Figure 13a). The other three cases are where the peak value (either or both $V_{Lsmax}$ of parasitic inductance and its duration $t_{VLs}$) is insufficient to create a low state at the output of the driver-2. In these three cases, there will be no reduction of $I_d$ (Figure 13b). It is a type of "binary" AGVC as, according to the load current, the di/dt is controlled (as in the first case) or not (other cases).

### 5.1.1. Simulation Results

The circuit in Figure 12 is simulated for a parasitic inductance of 1 nH ($L_s$ = 1 nH) and a drain current of 28 A (Figure 12). The proposed closed-loop control circuit does not slow down the switching speed of the current because the $V_{Lsmax}$ obtained during the di/dt is lower than the minimum activation voltage of the LM5114 driver (Figure 14). However, by increasing the value of $L_s$ to 2 nH for the same drain current ($I_d$ = 28 A), a sufficient input voltage is applied to the input of driver-2 (Figure 15b) that enables the LM5114 (driver-2) that allows us to slow down di/dt (Figure 15b). The significant delay time (20 ns Figure 15b) of LM5114 drivers compared to the switching time of the GaN transistor makes this closed-loop control have more effect on the dv/dt than the di/dt (Figure 15b).

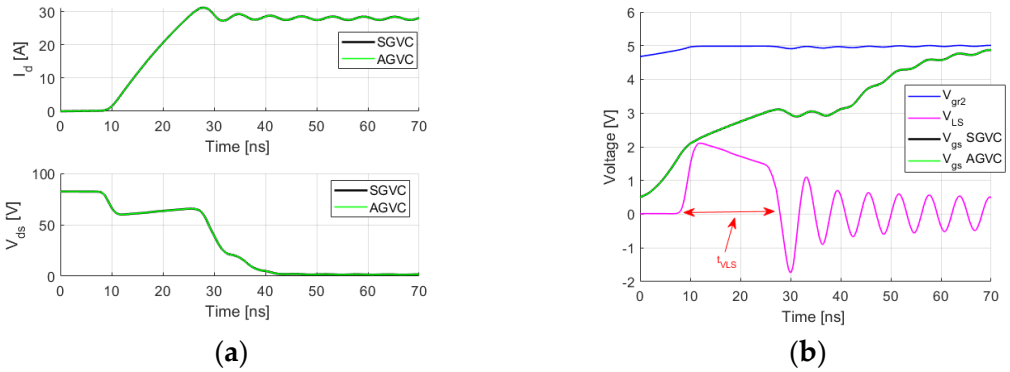



**Figure 14.** Simulated waveform of the main voltage and current using the proposed closed-loop active gate voltage circuit (AGVC) and standard gate voltage control (SGVC) ($I_d$ = 28 A, $L_s$ = 1 nH), (**a**) $V_{ds}$ and $I_d$, (**b**) $V_{Ls}$, $V_{gr2}$, $V_{gs}$ of AGVC, and $V_{gs}$ of SGVC.

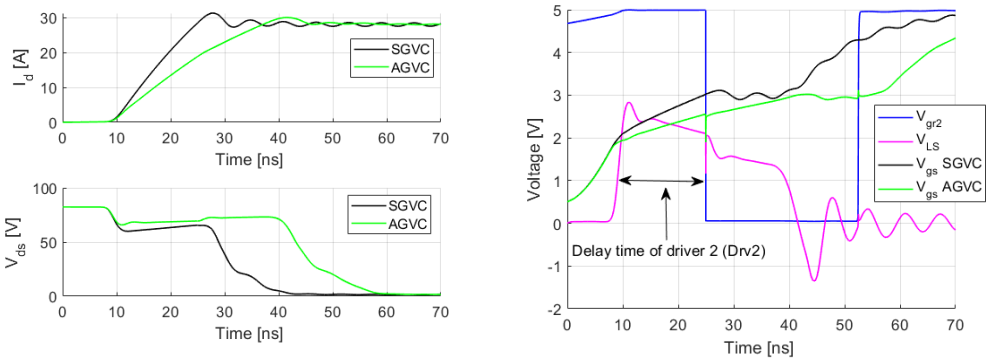



**Figure 15.** Simulated waveform of the main voltage and current using the proposed closed-loop active gate voltage circuit (AGVC) and standard gate voltage control ($I_d$ = 28 A, $L_s$ = 2 nH), (**a**) $V_{ds}$ and $I_d$, (**b**) $V_{Ls}$, $V_{gr2}$, $V_{gs}$ of AGVC and $V_{gs}$ of SGVC.

#### 5.1.2. Experimental Results

A circuit with 2 nH of $L_s$ as illustrated in Figure 12 was experimentally analyzed and the results are presented in Figure 16. For a load current between 5 and 20 A, the experimental circuit cannot slow down the current switching speed like the predictions of the simulation evaluation. The voltage across Ls ($V_{Lmax}$) is larger than the minimum activation voltage of the LM5114 driver (2.5 V). A fair assumption has been made on the driver operation, which the inactivation of the driver is due to a small application time, $t_{VLs}$, of $V_{Lmax}$. Therefore, the application of such a circuit requires a driver capable of reacting to an input signal shorter than or equal to 15 ns.

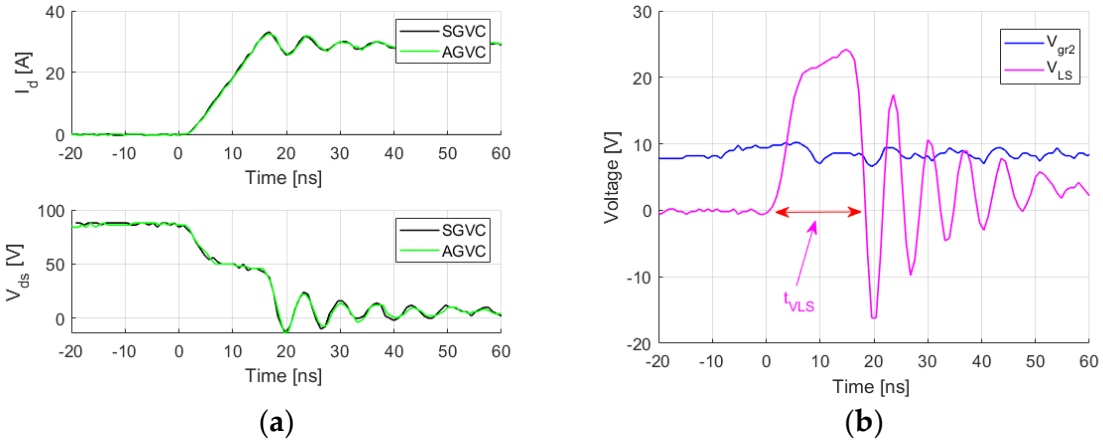



**Figure 16.** Experimental waveform of the main voltage and current using the proposed closed-loop active gate voltage circuit (AGVC) and standard gate voltage control (SGVC) ($I_d$ = 28 A, $L_s$ = 2 nH), (**a**) $V_{ds}$ and $I_d$, (**b**) $V_{Ls}$, $V_{gr2}$, $V_{gs}$ of AGVC and $V_{gs}$ of SGVC.

### *5.2. Closed-Loop AGVC with a Derivative Circuit during Turn-Off*

In this approach, the drain voltage $V_{ds}$ can be used to tune the parameter $t_{int}$ of the circuit (Figures 17 and 18), which comprise a resistor (R1), two diodes (D1, D2), and a capacitor (C1). At the beginning of the turn-off phase of the GaN transistor, a zero voltage can be applied to the cathode terminal of D2 and to the anode terminal of D1 while keeping the control signal $V_{gderiv}$ low. The increase in the drain voltage ($V_{ds}$) ensures the forward biasing of diodes D1 and D2 and produces a high-level control signal $V_{gderiv}$. At the end of the turn-off transient, the control signal $V_{gderiv}$ turns back to a low level (Figures 18 and 19).

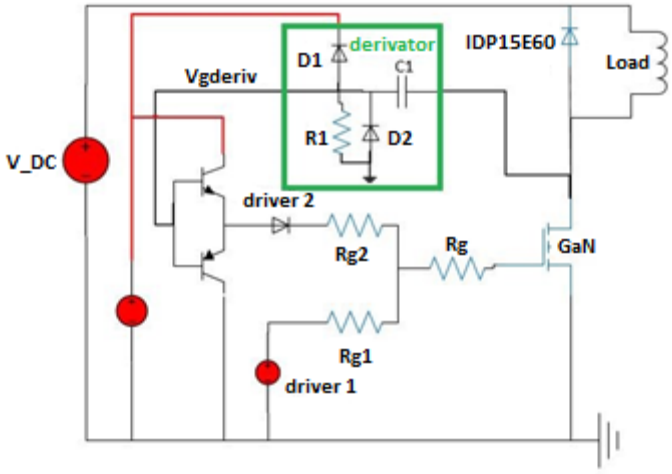



**Figure 17.** Schematic diagram of the proposed AGVC closed-loop during turn-off.

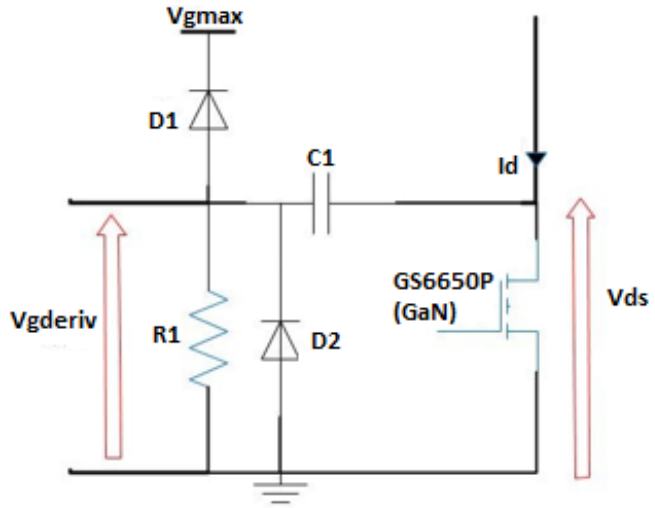



**Figure 18.** Schematic diagram of a derivative circuit.

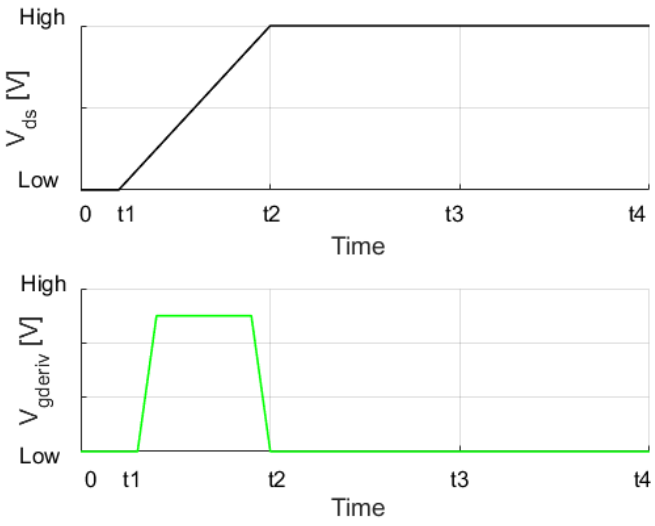



**Figure 19.** Simulated control signal of the driver ($V_{gderiv}$) during GaN transistor turn-off.

An experimental prototype of the circuit in Figure 17 was implemented. At the initial turn-off of the GaN transistor (see graphs during time 0 to 10 ns in Figure 20), the $V_{gs}$

signals are identical for both gate voltage controls (i.e., standard gate voltage control and AGVC closed-loop control for the turn-off). The drain voltage ($V_{ds}$) is lower than the voltage supply of the derivative circuit of the driver ($V_{grmax}$) during initial turn-off. Hence, the $V_{gderiv}$ signal is in a low state. After 15 ns, the voltage $V_{ds}$ is higher than the voltage $V_{grmax.}$ Therefore, the $V_{gderiv}$ signal increases (Figure 21). The proposed circuit applies an intermediate gate-source voltage starting from 15 ns. The ratio of the voltage transient speed of AGVC to SGVC is 0.97 as seen in Table 3.

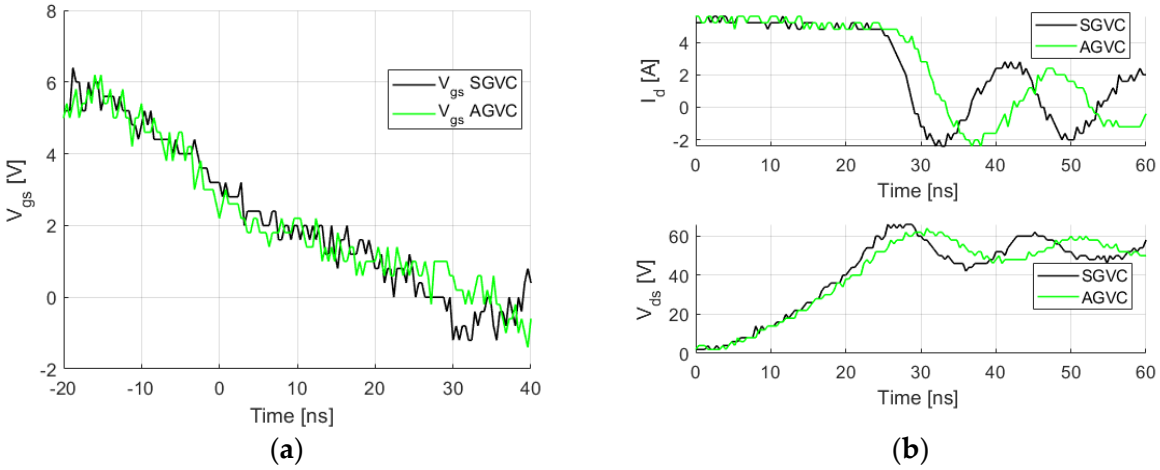



**Figure 20.** Experimental waveforms of the AGVC closed-loop voltage control compared to the standard gate voltage control ($I_d$ = 5 A, $V_{\_DC}$ = 50 V), (**a**) $V_{gs}$, (**b**) $V_{ds}$ and $I_d$.

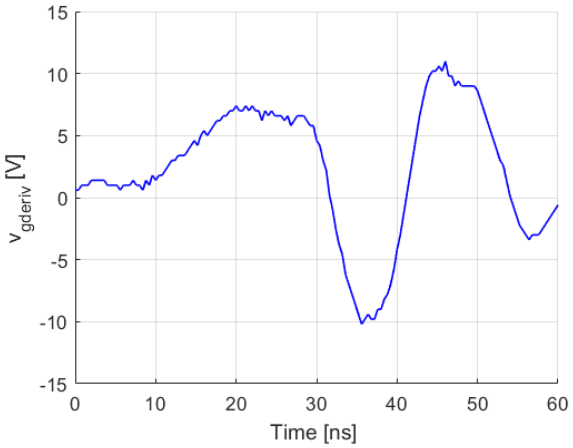



**Figure 21.** Input signal of $V_{gr2}$.

**Table 3.** Performances of closed loop of AGVC and standard gate control circuits during the turn-off.

| | AGCV di/dt [A/ns] | SGCV di/dt [A/ns] | AGCV dv/dt [V/ns] | SGCV dv/dt [V/ns] | di/dt (AGVC/SGVC) | dv/dt (AGVC/SGVC) |
|---|---|---|---|---|---|---|
| $V_{\_DC}$ = 100 V $I_d$ = 5 A | 0.61 | 0.66 | 4.4 | 5 | 0.92 | 0.88 |
| $V_{\_DC}$ = 100 V $I_d$ = 10 A | 1.31 | 1.56 | 5.34 | 5.6 | 0.8 | 0.95 |
| $V_{\_DC}$ = 50 V $I_d$ = 10 A | 1.56 | 1.6 | 3.5 | 3.62 | 0.98 | 0.97 |

As seen in the results, the speed of the current transients has not reduced significantly. Therefore, the losses are not in the case of the open-loop control. The switching waveform

of the drain current depends on several parameters. The first parameter is the response time of the driver that causes a significant delay in the output voltage of the driver ($V_{gr}$). The di/dt is reduced with an increase in $V_{gr}$. The closed-loop control system is more efficient when the supply voltage is above 100 V for a similar load current (i.e., 10 A as seen in Table 3). This technique has less impact on the current at high voltages when the switching time is large enough to compensate the response times of the driver. The second parameters are the resonance of the capacitance, resistance, and parasitic inductance of the circuit. To address this issue, a flip-flop is necessary to capture only one high-state event in the control signal $V_{gderiv}$.

## 6. Conclusions

Initially, the feasibility of controlling di/dt and dv/dt across GaN transistors in the open-loop gate control was studied with an experimental analysis. Despite its high switching speed, an application of the open-loop AGVC technique can be used to reduce the switching speed by 90% compared to a passive technique, resulting in a 50% reduction in the switching losses. Although the open-loop AGVC can be used to obtain fewer switching losses compared to the standard gate voltage control, it has many issues, such as the inability to control switching transient time of the power device less than 10 ns, and the difficulty of imposing similar transition patterns when the operating point vary. Furthermore, the variation of the experimental conditions (i.e., temperature, voltage, and current) affects the reduction rate in transient time. In order to solve these problems, a less complex AGVC-based closed-loop strategy was proposed. It was possible to manage the switching transients on the variation of the experimental conditions. However, due to the long response times (>10 ns) of the Si-based discrete components in the control circuit, it only solved these problems partially. However, by implementing a GaN-based monolithic circuit, the delays in the control loop can be eliminated.

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