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ABOVE 2 A/mm DRAIN CURRENT DENSITY OF GaN HEMTS GROWN ON SAPPHIRE

F. Medjdoub¹, J.-F. Carlin², M. Gonschorek², E. Feltin², M.A. Py², N. Grandjean², and E. Kohn¹, *Member IEEE*

¹University of Ulm, Albert Einstein Allee 45, 89081 Ulm, Germany,

Email: farid.medjdoub@uni-ulm.de

²Institute of Quantum Electronics and Photonics, Ecole Polytechnique Fédérale de Lausanne (EPFL),
CH 1015 Lausanne, Switzerland

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We report on the investigation of an InAlN/GaN HEMT structure, delivering higher sheet carrier density than the commonly used AlGaIn/GaN system. We achieved in a reproducible way more than 2 A/mm maximum drain current density for a gate length of 0.25 μm with unpassivated undoped devices realized on sapphire substrates. Small signal measurements yield a $F_T = 31$ GHz and $F_{\text{MAX}} = 52$ GHz, which illustrates the capability of these structures to operate at high frequencies. Moreover, the pulsed analysis indicates a more stable surface in the case of AlInN than that of AlGaIn, attributed to the lattice matched growth of this barrier with 17 % In content on GaN, avoiding strain piezo polarization in the material.

1. Introduction

GaN is a universal material for a variety of electronic and optoelectronic applications such as light emitters, transistors, and sensors. Due to its wide band gap it is particularly interesting for high-frequency and high-power Field-Effect Transistors devices. However, many difficulties arise from the lattice mismatch and polar surface of the commonly used AlGaIn/GaN heterojunction. Even if several improvements have been made in the growth and design of this material system in recent years the commercialization remains still difficult. Recently, the AlInN/GaN heterojunctions were proposed as alternative for power FETs [1].

In this paper we discuss results obtained from a GaN-based High Electron Mobility Transistor (HEMT) with an AlInN barrier. Applying Vegard's law for alloys of InN, AlN and GaN as indicated in Fig. 1, InAlN layers containing 17% Indium can be grown lattice matched on GaN and therefore have no piezoelectric stress component. This rather novel configuration promises high current densities up to 3 A/mm, the 2DEG being only induced by the difference in spontaneous polarization. Moreover, it offers a higher band offset between the GaN channel and the InAlN barrier as compared to AlGaIn. However, the materials system is difficult to grow due to the distinctly different growth conditions required for GaN and InAlN and the difficulty to incorporate In and Al in the same lattice without clustering. However, these problems have been widely overcome in first promising investigations [2,3].

Figure 1: Spontaneous polarization over the lattice constant of InN, AlN, GaN. Lattice matched AlInN is obtained for AlInN with 17% Indium.

2. Growth and processing

Major issues for the growth of AlInN are the different requirements for the growth parameters to achieve good crystalline quality for binaries contained in the ternary alloy, namely InN and AlN. AlN tends to grow polycrystalline for growth temperatures below 1000 °C [4,5]. On the other hand, InN can only be grown at low temperatures and high ammonia partial pressures, whereas high ammonia partial pressures have a strong effect on the AlN growth rate. Here, the studied structures (see Fig. 2) were grown by an AIXTRON MOCVD system on 2 inch diameter (0001) sapphire substrates [6]. They consist of 2 μm thick GaN buffer, 1 nm thick AlN spacer layer and 13 nm thick AlInN barrier layer with 81% Al composition. The thin optimized AlN interlayer is used to reduce alloy disorder scattering and thus to improve the transport characteristics. Room temperature Hall effect measurements yielded a 2DEG sheet charge of $2.6 \times 10^{13} \text{ cm}^{-2}$ with a record electron mobility of $1170 \text{ cm}^2/\text{Vs}$ and a sheet resistivity of $211 \Omega/\square$ [7].

Figure 2: Schematic cross section of the AlInN/GaN HEMT devices

Capacitance-Voltage profiling indicates a 2 DEG carrier density 14 nm below the surface at the AlInN/GaN interface (see Fig. 3), resulting in a sheet charge density in agreement with Hall measurements.

Figure 3: Capacitance-Voltage profiling. Formation of a 2 DEG is indicated at 14 nm below the surface.

FETs have been realized as follows: The devices are mesa isolated by Ar plasma etching. Then, Ti/Al/Ni/Au ohmic contact stacks are alloyed at 890°C in nitrogen atmosphere to provide contact resistances of 0.7 Ω .mm, as measured by linear TLM. The submicron gates ($L_g = 0.25 \mu\text{m}$) are defined with electron beam lithography. Ni/Au is deposited to produce the gate Schottky contacts. The HEMT devices are not yet passivated.

3. Experimental results

The output characteristics of a 0.25 μm gate length device with 25 μm gate width are shown in Fig. 4. The maximum drain current density at +2 V V_{GS} exceeds 2 A/mm in a reproducible way (2.3 A/mm for the presented device), which is to our knowledge beyond the highest drain current density of any AlGaIn/GaN HEMT structure, especially when fabricated on sapphire. It reflects the high sheet carrier density in this novel heterostructure. The transconductance peaks at 265 mS/mm (see Fig. 5) with 10 V applied to the drain and -5 V to the gate. The breakdown voltage at pinch-off is estimated to about 40 V for a device with a drain source spacing of 2.5 μm and is thought to be linked to residual buffer layer leakage.

Figure 4: DC output characteristics of an $\text{Al}_{0.81}\text{In}_{0.19}\text{N}/\text{GaN}$ HEMT $0.25 \times 25 \mu\text{m}^2$. V_{GS} swept from -10 V to 2 V by step of 2V

Figure 5: Transfer characteristics of an $\text{Al}_{0.81}\text{In}_{0.19}\text{N}/\text{GaN}$ HEMT $0.25 \times 25 \mu\text{m}^2$ at $V_{\text{DS}} = 10\text{V}$.

Pulse experiments were performed in a routine as used to assess the stability of AlGaIn/GaN devices (described with more details in [8]) with 500 ns pulses (see Fig. 6). All quiescent bias points (V_{DS0} , V_{GS0}) are chosen in order to simultaneously eliminate the thermal effect (cold polarization) and to reveal the gate and drain lag effects: ($V_{\text{DS0}} = 0\text{ V}$, $V_{\text{GS0}} = 0\text{ V}$), ($V_{\text{DS0}} = 0\text{ V}$, $V_{\text{GS0}} = \text{pinch-off voltage}$) and ($V_{\text{DS0}} = 10\text{ V}$, $V_{\text{GS0}} = \text{pinch-off voltage}$). The first quiescent bias point is used as the reference to compare with the other bias conditions. A drop of 13 % (gate lag) and 38 % (drain lag) regarding the maximum drain current density is observed at $V_{\text{DS}} = 10\text{ V}$. Compared to typical unpassivated AlGaIn/GaN structures on sapphire, those changes are much lower, which indicate a more stable surface in the case of AlInN.

Figure 6: Pulsed $I_{\text{D}}-V_{\text{DS}}$ characteristics of an $\text{Al}_{0.81}\text{In}_{0.19}\text{N}/\text{GaN}$ HEMT $0.25 \times 50 \mu\text{m}^2$ with three different quiescent bias points. V_{GS} swept from -9 to 1 V by step of -2 V.

The S-parameters of $0.25 \times 50 \mu\text{m}^2$ HEMTs were measured between 0.5 and 40 GHz. We achieved cut-off and maximum oscillation frequencies $F_{\text{T}} = 31\text{ GHz}$ and $F_{\text{max}} = 52\text{ GHz}$ (shown in figure 7) extrapolated from the current gain H_{21} and the maximum available gain (MAG) at $V_{\text{GS}} = -6.5\text{V}$ and $V_{\text{DS}} = 10\text{V}$ respectively. These results show the capability of this structure to operate at high frequency. It reflects the high material quality already obtained and the maturity of the processing technology. We observed a good $F_{\text{MAX}} / F_{\text{T}}$ ratio, which is may be directly correlated to the device power performances.

Figure 7: Current gain cut-off frequency ($|H_{21}|$) and maximum oscillation frequency (extrapolated from the Maximum Available Gain) for a $0.25 \times 50 \mu\text{m}^2$ $\text{Al}_{0.81}\text{In}_{0.19}\text{N}/\text{GaN}$ HEMT

4. Conclusion

We have investigated the potential of AlInN/GaN structures for high power applications. We obtained more than 2 A/mm open channel current which corresponds to the highest maximum drain current density delivered by any GaN FET. We have also revealed the capabilities of these structures to operate at high frequencies. Pulsed measurements reveal a more stable surface in the case of AlInN than that of AlGaIn. However, the breakdown voltage of these devices is still limited mainly because of a relatively low GaN buffer resistivity. The improvement of the GaN buffer resistivity associated with the utilization of a field plate technology should strongly improve the three-terminal breakdown voltage of these structures. Power measurements will be carried out on these devices.

6. Acknowledgement

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