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Nowadays, millimeter scale power sources are key devices for providing autonomy to smart, connected and miniaturized sensors. However, until now, planar solid state microbatteries do not yet exhibit a sufficient surface energy density. In that context, architectured 3D (3 dimensional) microbatteries appear therefore to be a good solution to improve the material mass loading while keeping small the footprint area. Beside the design itself of the 3D microbaterry, one important technological barrier to address is the conformal deposition of thin films (lithiated or not) on 3D structures. For that purpose, Atomic Layer Deposition (ALD) technology is a powerful technique that enable conformal coatings of thin film on complex substrate. In this paper, an original, robust and highly efficient 3D scaffold is proposed to significantly improve the geometrical surface of miniaturized 3D microbattery. Four functional layers composing the 3D lithium ion microbattery stacking has been

successfully deposited on simple and double microtubes 3D templates. Advanced characterization tools are used to highlight the interface between each layer (in depth synchrotron X-Ray nanotomography and HAADF (High Angle Annular Dark Field) Transmission electron microscope analyses). For the first time, using ALD, anatase TiO_2 negative electrode is coated on 3D tubes with Li_3PO_4 lithium phosphate as electrolyte, opening the way to all solid-state 3D microbatteries. Li_3PO_4 low temperature form exhibits a notably high ionic conductivity (# 6.2 x 10^{-7} $S.cm^{-1}$) and an electrochemical stability window close to 4.2V. The specific area resistance has been found to be the lowest reported so far (# 3.8 $\Omega.cm^2$). The deposited Li_3PO_4 layer is pinhole free and 100 % conformal on original, high aspect ratio (> 50) and highly robust 3D silicon microtubes. The surface capacity is significantly increased by the proposed topology (high Area Enlargement Factor (AEF) – "thick" 3D layer), from 3.5 $\mu Ah/cm^2$ for a planar layer up to 0.37 mAh/cm^2 for a 3D thin film (105 times higher). Clearly, this work paves the way towards high performance all-solid-state 3D on chip Li-ion microbatteries.

1. Introduction

Internet of Thing have recently emerged as an application for miniaturized and smart electronic devices capable of collecting, analyzing and transmitting data: wireless sensors or body area networks are the main declination of such concepts. The downscaling of these devices should also include the miniaturization of the embedded power sources to supply energy. Although a single energy harvesting device may be sufficient in some cases, energy storage is a crucial bottleneck for the spread of these products. While the surface of such smart miniaturized sensors is significantly reduced, the energy and power densities of planar solid state microbattery are no more sufficient to reach the requested self-powering ability.

For applications requiring a high energy density while maintaining a good power density, three-dimensional (3D) lithium-ion microbatteries (MB) have been proposed as an attractive solution[1],[2,3],[4],[5] in a similar way to the 3D electrostatic nanocapacitors[6],[7] developed by Rubloff *et al.*. Indeed, 3D architectures allow to enhance the mass loading of active materials while maintaining a small footprint area, which is the relevant parameter for microsystems[8,9], more energy-to-surface dependent than energy-to-weight **(figure 1)**.

Since the pioneer work of E. Peled in 1995, only 3D MB with liquid electrolyte have been published [1,5,9–11] and an all-solid-state 3D MB prototype is still not available. Despite interesting performance, the liquid based 3D MB do not fulfill the requirements to be integrated in miniaturized electronic devices owing to the flammability, the solvent evaporation and the potential leakage of this type of electrolyte.

In order to perform the fabrication of all-solid 3D MB prototype at the wafer level, a substantial hindrance should be overcome: the deposition of a thin film solid state electrolyte on 3D structured substrates. Besides exhibiting lithium ions conduction, the electrolyte layer should be pinhole free, highly conformal and exhibits an insulating behavior to maintain electrical isolation between the two electrodes. Therefore, “conventional techniques” such as radio frequency sputtering or chemical vapor deposition are not suitable because they would generate pinholes, cracks or inhomogeneous coverage of 3D scaffold, leading to short-circuits that would be responsible for the failure of the 3D MB. On the contrary, Atomic Layer Deposition (ALD) is a powerful technology to deposit such thin, pinhole-free and conformal layers on complex substrate. Moreover, nowadays, ALD is available from industrial point of view to deposit thin films on large surfaces (especially in the photovoltaic industry where solar panels with a surface close to 2 m^2 are produced[12]), demonstrating a potential technology transfer compatible with CMOS microelectronic facilities. ALD is a gas phase deposition process based on self-limiting reactions between a volatile precursor and active sites on the surface, enabling a control of the thickness at the atomic level. Moreover, it is

recognized for producing pinhole-free films, even for very low thickness. ALD has already been used in half cell prototype of 3D MB[13–15], with unlithiated transition metal oxide (V_2O_5, TiO_2,…) deposited on complex 3D structures. Tested in liquid electrolyte versus lithium metal electrode, such 3D ALD based electrodes clearly demonstrate the potentialities of this technology in the field of 3D electrochemical energy storage at the microscale. Moreover, since 2009, interest in ALD of lithium-containing film[16,17] is growing: thin film electrolytes ($Li_{0.32}La_{0.3}TiO_z$, Li_2O/Al_2O_3, Li_2O/Ta_2O_5, LiAlSiO, Li_3PO_4, LIPON (lithium phosphorous oxynitride))[18–23] on one side, and electrodes[24–26] ($LiMn_2O_4$, $LiCoO_2$, $LiFePO_4$) on the other side, have been developed, but independently, i.e. no coating of the one on the other.

To fabricate efficient Electrochemical Energy Storage (EES) microdevices, various 3D nanostructures such as anodized aluminum membrane (AAM), silicon nanowires (SiNW) or multiwall carbon nanotubes (MW-CNT) have been used as attractive scaffold by most of the investigators[14,27–29]. Unfortunately, the high flexibility of nanowires or nanotubes severely hinder a potential transfer of the technology to pilot lines production and these 3D templates could be viewed as model scaffold for a one-layer demonstration. Moreover, either the low spacing between two nanostructures (SiNW, MW-CNT) or the small diameter of nanopores (AAM) limit the thickness of the different layers to be coated. For instance, if on one hand, AAM is one of the most efficient and robust 3D template for Metal – Insulator – Metal electrostatic nanocapacitor, [6,30] where the thickness of each layer doesn't exceed 15 nm, on the other hand, this is not true in the present case where the surface capacity of the electrodes is proportional to the layer thickness. For instance, in AAM devices with a significant area enlargement factor (x 50), the deposited layer thickness should have been more than 100 nm to compete the planar devices. Unfortunately, the quite small diameter (roughly 250 nm) of AAM's nanopores, would not allow to deposit the at-least six layers (one insulator, two current collectors, two electrodes separated by a solid electrolyte) requested to build a 3D MB.

In order to fabricate high performance on-chip 3D MB at the wafer level, we should combine the technological realization of robust 3D scaffold with a high AEF and the conformal deposition of the 6 layers (thickness between 30 to 150 nm, depending on the functionality of the layer). We believe that instead of fragile nanostructures, "large" microstructures have to be selected, both for their robustness and from a structure spacing point of view. To the best of our knowledge, only P. Notten *et al.*[31] have investigated the chemical deposition of solid electrolyte (Li_3PO_4) on 3D robust silicon microstructures instead of nanostructures. Nevertheless, the low aspect ratio (1:1) of the proposed scaffold as well as the selected deposition technique (CVD) lead to a poor conformal (22 %) deposit on inefficient 3D template from specific area point of view. Despite a poor conformal behavior, some 3D MB prototype has been proposed by sputtering deposition means[32].

In this paper, the development of robust and efficient 3D scaffolds, combined with the potency of atomic layer deposition of 4 functional layers has been achieved. The robustness is ensured by the process itself (etching of the silicon wafer) while the efficiency is linked to the optimization of the pattern-design leading to high (>50) AEF (we present both optimized patterns of single microtubes, as well as a new design of double microtubes). Insulating thin film, current collector, negative electrode and solid electrolyte have been conformally deposited onto 3D silicon template, at the wafer level. It is important to note that technological fabrication process of such 3D devices is fully compatible with the existing microfabrication facilities of the microelectronic industry.

Beside "classical" structure and microstructure characterization, the quality of the interfaces has also been studied by HAADF Transmission Electron Microscopy and synchrotron X-Ray nanotomography analyses to check interdiffusion between the stacked layers. Finally, the electrochemical behavior of the electrolyte has also been fully characterized and confronted to literature.

In a first part, original and robust 3D silicon scaffold have been fabricated with Si-compatible microelectronic facilities. Lithography and etching tools have been used to fabricate 3D mechanically robust and high aspect ratio (AR 80:1) silicon single microtubes (SMT, concept already published[15] with AEF close to 30 but improved in this paper leading to an AEF value of 50) and double microtubes (DMT, innovative design presented here) on 3 inches silicon wafer. The geometrical parameters of the microtubes (diameters, spacing, etched depth) have been fine tuned to reach a high AEF (# 50) while keeping large enough the spacing between two microstructures, as well as the inner diameter of the tubes, to allow the deposition of several functional layers. When such high specific area scaffold is combined with step conformal deposition facilities allowing to produce thin layers (at least 100 nm thick), high performance electrochemical energy storage microdevices could be fabricated at the wafer level.

In a second part, the successful ALD of pinhole-free solid electrolyte Li_3PO_4 on 3D scaffold is presented. After optimization, the as-deposited solid electrolyte reaches the highest ionic conductivity obtained for an ALD lithium containing solid thin film electrolyte (6.2 x 10^{-7} S/cm) leading to the lowest area specific resistance never reached (3.8 $\Omega.cm^2$). Moreover, a large electrochemical window stability (4.2 V) has been demonstrated. The conformality of the Li_3PO_4 thin film on our high aspect ratio 3D microstructures is measured to be as close as possible to 100 %.

Finally, in a third part, four functional layers composing on chip 3D MB are successfully developed: Al_2O_3 (insulating layer), platinum Pt (current collector), TiO_2 (negative electrode) and Li_3PO_4 (solid electrolyte) thin films are deposited on 3D silicon scaffold. Three types of 3D silicon-etched scaffold, namely micropillars, single and double microtubes. X-ray nanotomography and Transmission Electron Microscope analyses have been performed to check the interfaces between the layers and to picture at a 3D level, the coating of the different layers. The performances of the anatase TiO_2 negative electrodes

deposited on 3D silicon single and double microtubes are measured when combined with the Li_3PO_4 solid electrolyte (< 60 nm thick). To demonstrate the outstanding performance of the proposed high AEF scaffold topologies, a "thick" (155 nm) TiO_2 layer has also been synthesized leading to a noteworthy surface capacity of 0.37 mAh/cm^2. To the best of our knowledge, this is the first time that the surface capacity of anatase TiO_2 thin films deposited on 3D robust and efficient template is evaluated in solid electrolyte. This work paves the way to the fabrication of 3D Li-ion all-solid state microbattery at the wafer-level with significantly improved performance and the successive deposition of highly conformal layers.

2. Design of the 3D Li-ion all solid state microbattery

A "classical" solid state planar lithium microbattery[33] (MB) developed at the wafer level **(figure 1A)** exhibits an energy density of roughly 0.5 mWh/cm^2. Typically, this 2D MB is composed by the already described 6 layers and the thickness of the electrode materials, linked to the energy density performances, varies between 1000 nm up to 4000 nm. To simplify the explanation, let consider an average thickness of 3000 nm. To reach the same energy density with a 3D concentric MB than with a planar one **(figure 1A)**, the area enlargement factor (AEF) of the 3D scaffold have to be at least 30 (*i.e.* the ratio between 3000 nm and 100 nm) if, of course, same materials are considered for both 2D and 3D MB prototypes. Moreover, since a significant increase of the energy performances is expected, this AEF should reach a higher value (typically, more than 50). As already discussed, nanostructured 3D template is known to be really interesting from the AEF point of view but suffer from either a lack of space to achieve the conformal deposition of 6 layers (AAM – small pore diameter) or from a high flexibility: these drawbacks severely hinders the technological transfer toward pilot line production (SiNW, CNT). Then, going to microstructured vertically aligned 3D scaffold is an attractive solution from robustness point

of view. Moreover, the geometrical parameters could be fine-tuned to allow the deposition of the six layers having a significant thickness while keeping high the AEF, at the same level of magnitude than the 3D nanostructures scaffold.

In such way, the spacing **(figure 1B)** between two microstructures is kept close to 1 µm to have both a dense 3D scaffold and to allow the deposition of the six layers. Moreover, if hollow microstructures are fabricated (ex: microtubes), the inner diameter should have been set to at least 1 µm for the same reasons. The most effective mean to increase the surface capacity in such 3D devices is to increase the quantity of active materials. In that case, since the material deposition is achieved on the edge of each microstructure, the lateral surface (base perimeter x etched depth) should be maximized (**figure 1B**). Regarding the limitation of the etching tools (AR max = 80: 1) and the minimum lateral dimension set to 1 µm (spacing, inner diameter), the maximum theoretical etched depth achievable is 80 µm. Moreover, to guarantee a sufficient robustness of the 3D scaffold (i.e. non-flexible), we have set the outer diameter of the microstructures to 5 µm. This leads to a structure pitch close to 6 µm (sum of the outer diameter and the spacing parameters – **figure 1B**). As the depth of the microstructures is limited firstly by the robustness and secondly by the maximum AR of the etching tools, an attractive solution consists in the fabrication of microtubes **(figure 1B)** where the lateral area accessible to increase the mass loading could be doubled. It is clear that the lateral area available with the microtubes[15] technology is higher than the one for micropillars **(figure 1B)** having similar outer diameter. If two tubes are fabricated instead of one, this remark is further enhanced. In this paper, silicon based single and double microtubes scaffold are fabricated **(figure 1B)**. The technological limits of the SMT (single microtube) have been reached considering the geometrical parameters imposed to fulfill robustness. In such a way, we succeeded to achieve an AEF of 53 with the fabrication of 78 µm depth SMT. A novel, original, as robust and more efficient topology is also proposed in this paper: the double microtubes as described in **figure 1B and 1C**. Silicon double microtubes (DMT) array

(58 µm depth – **figure 1C**) have been successfully fabricated and, regarding the dimensions of the 3D scaffold, the corresponding AEF is close to 45 approaching the AEF of the SMT but, for the moment, with a lower etched depth. This is in the same order of magnitude than the AAM scaffold proposed by Rubloff *et al* for electrostatic nanocapacitor[28] but the SMT **(figure 1D)** and DMT templates allow to deposit thicker layer due to higher spacing and inner diameter. As demonstrated recently[15], the etched depth inside the tube is half the outside depth (**figure 1B**). Silicon Micropillars (MP) and microwalls (MW) were also fabricated either for morphological analyses (Scanning and Transmission electron microscopy and 3D X-ray nanotomography analyses). A complete description of theses 3D scaffold is reported in the **table 1**.

Once the 3D scaffolds are designed and fabricated, the next step is to build concentric 3D MB by achieving the step-conformal materials deposition on the substrate. To reach this goal and as already discussed, ALD technology has been selected for the whole stacks **(figure 1A)**. The temperature deposition of all the layers does not exceed 300 °C meaning that the thermal budget of the 3D MB fabrication is around 300 °C. For on chip 3D MB developed at the wafer level, an insulating layer is firstly required to isolate each microbattery. Indeed, as the footprint area of each 3D MB is roughly a few square millimeters, many samples are fabricated on a 3 inches (at the lab scale) or 8 inches (in pilot production line) silicon wafer and all these MB need to be isolated the one from the other. Al_2O_3 (100 nm thick) is selected regarding its insulator behavior as well as its ability to be easily deposited by ALD[13]. Moreover, regarding the thickness of this layer, the scalloping effect owing to the deep reactive ion etching process of the silicon microstructures is significantly reduced by smoothing the surface by decreasing the roughness and so limiting the defects or outliers of the 3D template[27,28]. A current collector, in our case, platinum (30 nm) is then deposited on the alumina thin film. Then, TiO_2 (anatase polymorph) is used as negative electrode. We have chosen this electrode material because it has already been developed previously within the

scientific community of 3D MB[14,15,34] and has been shown to be efficient. Moreover, we have already worked with such TiO_2 3D electrode but uncoated with solid electrolyte. Within the frame of this study **(figure 1A)**, we finally covered the 3D SMT and DMT $Al_2O_3/Pt/TiO_2$ stacking by a low thickness, conformal and pinhole free Li_3PO_4 solid electrolyte.

3. Next step towards all solid state 3D microdevices: step conformal deposition of 4 functional layers on 3D silicon microtubes scaffold

Atomic Layer Deposition of the solid electrolyte has been successfully optimized in the framework of this paper. Structural, chemical and SEM analyses have confirmed that a step-conformal β-Li_3PO_4 layer could be deposited on 3D scaffold (see supporting information). Five samples with different configurations have been fabricated to demonstrate the potentialities of the proposed technology. ~~To have a reference, the first sample was not coated with Li_3PO_4 solid electrolyte. On the other samples, 4 functional layers have been deposited by ALD (insulating layer: Al_2O_3, current collector: Pt, negative electrode: TiO_2 and solid electrolyte: Li_3PO_4).~~ The overall parameters of the five samples are summarized in **table 1**. The planar S_{2D1} sample, is the reference's one (without solid electrolyte) for the electrochemical study. The S_{2D2} sample is similar to S_{2D1} but with an additional Li_3PO_4 layer on the top. The surface charge and discharge capacities of planar TiO_2 thin film are measured with this S_{2D2} sample. The 3D micropillars sample (MP sample) is used for the synchrotron X-ray nanotomography analysis. Silicon single and double microtubes samples (SMT and DMT samples) are fabricated following the technological process described in experimental setup. Two high AEF values close to 50 are obtained with such 3D microtubes scaffolds. The SMT sample is coated with a TiO_2 thin film (thickness up to 155 nm) while the DMT sample, exhibiting a lower etched depth than the SMT scaffold (see **table 1**), is decorated with a

thinner TiO_2 layer (55 nm). Except the S_{2D1} sample, all the samples are coated by the Li_3PO_4 solid electrolyte with thicknesses varying between 20 and 40 nm.

First of all, structural and microstructural analyses of the 3D samples were undertaken. The **figure 2** show transmission electron microscope analysis (TEM) of the DMT sample. A longitudinal cross section of the DMT was prepared by focused ion beam techniques and clearly shows the conformal deposition of several layers outside and inside the double microtube scaffold (**figure 2 A**). The observed thicknesses of the 4 layers are in good agreement with the targeted requests. When zooming on the top left corner of the DMT (**figure 2B, 2C and 2D**), the 4 layers deposited on the silicon template are clearly highlighted (Z contrast analysis).

Energy Dispersive X-ray spectroscopy (EDX) chemical analyses **(figure 2 E to J)** within the TEM are also given to i) study the elementary composition of each layer and ii) check the interfaces where interdiffusion phenomena between the layers could occur. From this chemical mapping analysis (silicon element – red color (**figure 2F**), aluminum element – orange color (**figure 2G**), platinum element (**figure 2H**) – blue color, titanium element – green color (**figure 2I**)), three layers have been totally identified with no interdiffusion at the interface. When focusing on the outside interface of the DMT scaffold (**figure 2J**), a thin Li_3PO_4 layer between the TiO_2 and the SiO_2 protective layer is observed. The lithium element is not sensed by EDX but the phosphorous one is perceived. Structural analyses (**figure 2K and figure SI.6**) performed in the TEM have confirmed the anatase polymorph of TiO_2 while the β-form of Li_3PO_4 is identified as the last layer of the stacking. A similar study has been performed on the SMT sample (TEM analysis proposed on **figure SI.5)** and the conformal deposition of the 4 layers is also demonstrated for the SMT 3D scaffold. In summary, no interdiffusion is observed again confirming the pertinence approach of the proposed study with the ALD technology.

To complete the TEM morphological and chemical mapping analyses, Transmission X-ray Microscope (TXM) is used to study the MP sample by X-ray Micro-tomography. The obtained results are reported in **figure 3**. 3D analysis (TXM image) of a silicon micropillar coated with the four functional layers deposited by ALD is proposed on **figure 3**. The corresponding 4 layers stacked on the 3D isolated microstructure (Al_2O_3, Pt, TiO_2 and Li_3PO_4 thin films) can be distinguished by relative contrast and are consistent with the thickness measured by TEM on a sample exhibiting a concentric topology **(figure 3A and B)**. The TXM tomography reconstruction (**figure 3C and D**) of a single micropillar shows regular stripes at the surface, perfectly illustrating the scalloping effect produced by the etching process.

4. Further insights on the Al_2O_3/Pt/TiO_2/Li_3PO_4 stacked layers all-deposited by ALD on 3D scaffold

Several complementary measurements are required to finalize the study. Firstly, the electrochemical window stability of the solid electrolyte should be evaluated. To reach this goal, two additional samples (S_6 and S_7) have been studied by (CV) cyclic voltammetry (0.1 mV/s) in the window stability of a liquid electrolyte (1M LiTFSI in EC/DEC (1/1)) in between 0.5 V and 4.7 V vs Li/Li^+. The S_6 sample is only a platinum layer (40 nm thick) deposited by ALD on a planar silicon wafer and the CV is performed against a lithium metal foil acting as the reference and the counter electrodes. The S_7 sample is similar to the first one but an additional Li_3PO_4 layer (60 nm thick) is deposited on the top of the platinum layer. The lowest limit of the CV has been set to 0.5 V vs Li/Li^+ in order not to induce a Li-Pt alloy while the liquid electrolyte is known to decompose above 4.7 V vs Li/Li^+. As depicted on **figure 4A**, the Li_3PO_4 solid electrolyte clearly demonstrates a large electrochemical window stability (4.2 V) in the same order of magnitude that the one measured[35] by Kamawura *et al*.

From this measurement, it is clear that the Li_3PO_4 is a lithium ion conductor and the ionic conductivity of such thin films has thus been evaluated.

The **figure 4B and 4C** reports the electrochemical impedance spectroscopy (EIS) measurements of 5 planar samples (from LPO_1 up to LPO_5 – see **table 2**) with various temperature of the ALD reactor and different layer thicknesses, focusing only on the Li_3PO_4 study. The methodology used to perform the measurement of the ionic conductivity of such solid electrolyte is based on the Bates' study[36] on LIPON thin films. According to the shape of the impedance spectra exhibiting a semicircle behavior, the equivalent circuit used to fit the plots is composed of a resistance in parallel with a capacitor and in series with an additional resistance as shown in inset. The ionic conductivity has been evaluated after fitting the Nyquist plot with the equivalent circuit model to find the resistance of the Li_3PO_4 bulk layer (**figure 4B and 4C**). An alternative method is proposed in this paper to measure the ionic conductivity of the Li_3PO_4 layers – without a fitting step – by plotting the ionic conductivity issued from the admittance measurement as a function of the frequency. In this approach, the plateau at low frequency is directly linked to the ionic conductivity of the solid electrolyte. The two different methods of ionic conductivity measurement were applied in this paper and lead, fortunately, to the same conclusion.

The R_2 resistance represents the bulk resistance of the solid electrolyte while the R_1 remains the resistance of the platinum blocking electrode. The diameter of the semicircle (**figure 4B and 4C**) corresponds to the area specific resistance (ASR) contribution and thus to the ionic conductivity of the solid electrolyte. Instead of a perfect capacitor, a constant phase element (CPE) is used to approximate the capacity of the dielectric thin film. As shown on **figure 4B and 4C**, the impedance plots of the 5 tested LPO samples do not exhibit a tail at low frequency as proposed[20] by X. Sun *et al*. The semicircular shape is the typical behavior of a solid electrolyte in between two blocking electrodes with no diffusion of the lithium through the Pt layer. The **figure 4B** reports the Nyquist plots of the Li_3PO_4 as a function of

the reactor's temperature with a thickness kept around 50 nm (# 1000 ALD cycles), while on **figure 4C**, the Nyquist plots of Li_3PO_4 deposited at 300 °C with varying thickness are proposed. The measured ionic conductivity of the five samples using the fitting method (**figure 4D**) is reported on **table 2** and a comparison with the non-fitting method is proposed for the 3 last deposited samples.

Ionic conductivities of LPO_1 (250 °C) and LPO_2 (325 °C), measured at room temperature (RT), have been evaluated respectively to 1.44 x 10^{-7} S/cm and 2.31 x 10^{-7} S/cm, while, at 300 °C, it is found to 4.33 x 10^{-7} S/cm. These value are i) of the same order of magnitude than the LIPON solid electrolyte deposited by ALD recently[18,19], ii) one order of magnitude higher than the value obtained[31] by Notten *et al* in 2014 with Li_3PO_4 deposited by CVD and finally iii) of the same order than the value published by Kamawura *et al*[35] where the Li_3PO_4 thin film is deposited by Pulsed Laser Deposition (4.0 x 10^{-7} S.cm^{-1} at RT). With such performance, the area specific resistive contribution (ASR) of the LPO_3 sample (60 nm, 4.33 x 10^{-7} S/cm ⇨ 13.85 Ω.cm^2) is more than two times better than the one obtained by a LIPON[37] thin film deposited by RF sputtering (1 µm, 3 x 10^{-6} S/cm ⇨ 33 Ω.cm^2), a non-conformal deposition method. As no short-circuit between the two blocking electrodes has been highlighted during the EIS measurements, the thickness of the solid electrolyte has progressively been decreased to improve the ASR. The LPO_4 sample (30 nm thick) exhibits an outstanding ionic conductivity (6.2 x 10^{-7} S/cm) leading to an ASR close to 4.85 Ω.cm^2. Despite a lower ionic conductivity (2.6 x 10^{-7} S/cm), the LPO_5 sample (10 nm thick) reach the impressive value of 3.84 Ω.cm^2 with a pinhole free layer. This value has never been reached for a solid electrolyte deposited by ALD (see **table 2** and **table 3** for comparison purpose). The low obtained ASR for this Li_3PO_4 solid electrolyte is i) 150% lower than the previous value (6 Ω.cm^2) published by B. Dunn[38] *et al* in 2014 and ii) 500% lower than the ones recently reported in 2015 for LIPON solid electrolyte deposited by ALD[18,19]. The ionic

conductivities of the LPO_3, LPO_4 and LPO_5 samples calculated with the two proposed methods (with and without fit) are the same, clearly validating the measurements.

We have thus demonstrated that nitrogen-free Li_3PO_4 is a suitable candidate as solid electrolyte for 3D Li-ion microbattery (pinhole free layer (10 nm thick), 4.2 V electrochemical window, ionic conductivity close to 5 x 10^{-7} S/cm, ASR = 3.84 Ω.cm^2). The conformality of the Li_3PO_4 thin film, already demonstrated on **figure 2**, is also confirmed when only the Li_3PO_4 layer is considered on 3D scaffold (~~100 % conformity~~), as shown on **figure SI-4**.

~~To finalize the study, the electrochemical behavior of a 3D electrode coated with this solid electrolyte should be evaluated. As a matter of fact, the areal capacity of the 3D electrode has to be measured. For this purpose, the anatase TiO_2 negative electrode is conformally deposited on 3D silicon single and double microtubes topologies (see **figure 2 and 3**). Then, these samples are decorated with the Li_3PO_4 thin film. To the best of the authors' knowledge, this is the first time that the areal capacity is measured together with a solid electrolyte layer. This study provides new insights in the development of all-solid-state 3D Li-ion microbattery.~~

The last part of this electrochemical study is focused on the cyclability as well as the charge and discharge surface capacities of the S_{2D2}, SMT and DMT samples (**figures 2 and 3**). The aim of these analyses is to demonstrate i) the improvement of the material mass loading by an efficient and robust scaffold specially designed for electrochemical energy storage devices at the microscale and ii) the ionic conduction of the lithium ion through the Li_3PO_4 thin films, from a lithium foil to the TiO_2 negative electrode. As lithium metal could not be deposited by ALD, the samples and particularly the Li_3PO_4 layer were evaluated against a liquid electrolyte (1M LiTFSI EC/DEC (1/1)). A lithium foil acting as the counter and reference electrodes is placed in the electrolyte tank. ~~The **figure 4** reports the electrochemical analyses of the proposed samples.~~ The cyclic voltammetry of the S_{2D1} planar sample (without

the Li_3PO_4 solid electrolyte) is depicted in **figure 4E**. The classical behavior of a TiO_2 anatase thin film is observed with two redox peaks occurring respectively at 1.7 V and 2.1 V vs Li/Li^+ as already published[39]. Galvanostatic plots of the S_{2D2} sample (with the Li_3PO_4 coating) have been performed (not shown in this paper) at C/10 between 1 V and 3.5 V vs Li/Li^+. As expected, the plateaus occur at the same potential than the S_{2D1} clearly demonstrating the ionic conduction of the lithium ion, from the lithium foil, through the Li_3PO_4 solid electrolyte and to the TiO_2 thin film. The surface capacity (3.5 $\mu Ah/cm^2$) of this sample has been extracted from this galvanostatic plot taking into account both the thickness and the dimension of the test area. This surface capacity hereafter our reference capacity of planar TiO_2 thin film (55 nm thick) will be compared during the following measurements to the areal capacity of the 3D samples. Similar measurements have been investigated on 3D SMT and DMT samples (**figure 4F, G and H**). The surface charge and the discharge capacities of the DMT sample are given in **figure 4F:** when the C Rate is increased from C/20 up to 2C, the charge capacity is reduced from 0.14 mAh/cm^2 down to 50 $\mu Ah/cm^2$ and the plateau progressively shifts to lower potential, until it disappears. Despite a moderate thickness (55 nm), an interesting surface capacity is obtained, thanks to the efficiency of 3D scaffold (high AEF). Cyclability of the DMT sample is given **figure 4G** where more than 70 cycles at different C rate are reported. From these measurements, the benefit from the 3D scaffold to improve the material mass loading on a limited footprint area is clearly shown. To the best of the authors' knowledge, this is the first time that such 3D effect is demonstrated in solid electrolyte environment. To prove the pertinence of our approach when designing the 3D scaffold (i.e. that performances should increase with increasing amount of active material), a TiO_2 layer exhibiting a higher thickness (155 nm) has been deposited by ALD on the 3D SMT template. As already discussed, such thickness could only be deposited on scaffold where geometrical dimensions (structure diameters, spacing) have been carefully optimized while this goal could not be reached with most of proposed concept[27,29]. An outstanding surface

capacity (**figure 4H**) of 0.37 mAh.cm^2 at C/16 is reached when combining high AEF scaffold (53) and "thick" layer (at the scale of the ALD world!). Several cycles have been essential to stabilize the surface capacities of the thin film electrodes coated with the Li_3PO_4 solid electrolyte (**figure 4H)**. When the C rate is increased, the surface capacities progressively decrease from 0.37 mAh/cm^2 at C/16 down to 80 µAh/cm^2 at 2C (**figure 4I**). At C/11, the surface capacity stabilizes around 0.3 mAh/cm^2. The 3D SMT electrode has been cycled during 75 cycles.

A benchmark of the different proposed concept is reported on **figure 5**. Two different areas are pointed out on the graph reporting the surface capacity of TiO_2 thin films as a function of the layer thickness and the AEF. The first set (red rectangle) of results[14,29,34] is obtained with TiO_2 thin films deposited on 3D nanostructures (Ni nanowires, Tobacco Mosaic Virus nanoscaffold and Al nanorod template) without solid electrolyte additional layer. Blue rectangle corresponds to "our" TiO_2 thin films (S_{2D2}, DMT and SMT samples) coated with a solid electrolyte. DMT scaffold coated with 55 nm demonstrate an areal capacity higher than 100 µAh/cm^2 depending the used C rate (C/20 up to C/10). As shown on **figure 1 and 2**, the diameter as well as the spacing between two DMT would allow to deposit higher thickness. This remark is also acceptable for the SMT scaffold. A step-conformal TiO_2 thin film of 155 nm coated on the 3D SMT scaffold (AEF = 53) reaches a surface capacity of 0.37 mAh/cm^2 more than two times higher than the areal capacity (170 µAh/cm^2) measured by S. George *et al* when using Nickel nanowires and thin TiO_2 layer (17 nm). In this reference[14], there is not enough space between two nanostructures to allow the deposition of high thickness layer and it would be really difficult to be competitive against 2D microbattery with such concept, since the electrode thicknesses are limited by the spacing parameter (< 20 nm per layer). Just for comparison, a sputtered $LiCoO_2$ thin film acting as a positive electrode exhibits a normalized discharge capacity close to 50 µAh/cm^2/µm meaning that 3 µm thick thin film provides 150 µAh/cm^2. Our proposed technology allows to reach an outstanding discharge capacity of 370

µAh/cm^2 with a 155 nm TiO_2 layer, clearly demonstrating the benefits of 3D SMT and DMT robust scaffold against nanostructured based templates: this value is roughly 100 times higher than the surface capacity (3.5 µAh/cm^2) of our planar reference TiO_2 thin film (55 nm).

Conclusion

We have demonstrated in the framework of this study an attractive design of 3D based electrochemical energy storage devices at the micrometer scale. Robust, efficient and easy scalable 3D topologies are proposed to significantly improve the surface capacities of on-chip 3D Li-ion microbattery embedded as micropower sources for smart and connected microsensors. In such way, single and double silicon microtubes scaffold are fabricated to reach an area enhancement factor of 50 ± 5 i.e. of the same order of fragile nanostructured templates for 3D based devices. Nevertheless, in our design, the spacing between two robust microstructures as well as the inner diameter of each tube (1 µm), allowing to deposit thicker layers than the one deposited on highly flexible nanostructured templates. Four functional layers (# 100 nm thick) of the 3D microbattery have been deposited by ALD on the proposed scaffold. An insulating layer, a current collector, a negative electrode and the solid electrolyte have been step-conformally deposited on the 3D microtubes pattern. Chemical mapping analysis achieved by TEM combined with synchrotron X-Ray nanotomography have confirmed the conformal shape of the deposited layers as well as the good quality of each interface leading to non interdiffusion in between the thin layers. The proposed Li_3PO_4 pinhole free 3D solid electrolyte (electrochemical window stability > 4.2 V) has reached a good conformality ~~close to 100 %~~ on high aspect ratio structures and one of the best area surface resistance contribution (3.84 Ω.cm^2) obtained for such layer combining a high ionic

conductivity (6.2 x 10^{-7} S/cm) and a low thickness layer (10 nm). To clearly demonstrate the potential of the proposed solution (SMT and DMT topologies coated with ALD of functional layers), the surface capacity of TiO_2 based negative electrode is evaluated when combined with this Li_3PO_4 solid electrolyte. To the best of the authors' knowledge, this is the first time that an outstanding surface capacity close to 0.37 mAh/cm^2 (at least 220% higher than the best value obtained with a TiO_2 electrode deposited on 3D nanostructured scaffold and tested in liquid electrolyte) is reached, even more true when considering this value measured with a solid electrolyte.

Experimental Section

Film preparation: Al_2O_3, Pt and TiO_2 layers were deposited from a Beneq TFS 200 ALD reactor. Li_3PO_4 thin films were grown in a Picosun R200 ALD reactor under an argon pressure around 2 mbar. Argon was used as the carrier and purging gas. Lithium tert—butoxide (LiO^tBu) and trimethyl phosphate (TMPO) precursors were used respectively as lithium and phosphate sources. The LiO^tBu precursor war purchased from Strem Chemicals (claimed purity 98%) while TMPO precursor was purchased from Sigma-Aldrich (claimed purity 99%). The adapted sublimation temperature was 185°C and 85°C respectively. Most films were deposited with a total of 500 cycles except the ones for electrochemical tests (1000 cycles) in order to optimize the precursors' consumption. LiO^tBu and TMPO were pulsed into the chamber alternatively with different pulse time duration separated by 6 s argon purge. For LiO^tBu pulse lengths of 0.5, 0.6, 0.8, 1, 1.2, 1.5 and 4 s were used while pulse times of 0.6, 1, 2, 4, 6 and 8 s were used for TMPO. Aside from electrochemical measurements which were carried out on Li_3PO_4 films on Pt coated silicon (100) substrates, all characterizations were conducted on Li_3PO_4 films deposited on silicon (100) substrates.

3D silicon microstructures have been fabricated by following a double step technological process. Lithography of resists (acting as the etching mask) and Deep Reactive Ion Etching (Oxford Plasma pro 100 Estrelas dry etching equipment) processes are combined to perform the fabrication of such 3D scaffold.

Sample morphological and structural characterization: Film thicknesses were accurately determined from X-ray reflectivity (XRR) fits on planar substrate. For 3D films, thicknesses have been evaluated by SEM (Zeiss Ultra 55 Scanning Electron Microscope) at the top, along the edge and at the bottom of the 3D microstructures to determine the full conformality of the ALD-processed Li_3PO_4 solid electrolyte. Crystallinity of the whole films was examined in grazing incidence X-ray diffraction (GIXRD) with a Rigaku SMARTLAB multi-purpose six-axis diffractometer (9 kW rotating anode) using CuKα- radiation (λ=1.5418 Å). The local-structure was also confirmed by microRaman spectroscopy through the use of a Horiba Jobin Yvon LabRam HR UV Raman spectrometer with a 473nm-laser source. Micropillars were separated from the Si wafer and were mounted on copper grids to allow X-Ray nanotomography analyses. Simple and double microtubes were also mounted on a copper grid to achieve the TEM analyses. High-resolution TEM, EDX-STEM and HAADF-STEM experiments were acquired using a JEOL-ARM200F 200 kV equipped of Cs image corrector and Cold-FEG. TEM images have been processed using FIJI and Digital Micrograph softwares. SAED pattern was calculated using the MactempasX-2 software.

The TXM images have been acquired on the beamline 32-ID of the APS synchrotron at Argonne National Laboratory. Data set acquired at 8 keV with 3 s exposure time / projection. X-ray objective lens = Fresnel zone plate (FZP) with 60 nm outermost zone width. The numerical aperture of the FZP was matched by the condenser. The condenser was a beam shaping condenser, i.e. a grating with 1.32 mm of diameter and 60 nm spacing for the outermost grating. ~710 projections acquired along 177o instead of the usual 180o. We had

missing angles because of the substrate blocking the view. Pixel is ~20 nm large but the true spatial resolution is 60 nm (you can see 60 nm features with at least 2 pixels). Reconstruction made with Tomopy (Gürsoy, Doga, et al. "TomoPy: a framework for the analysis of synchrotron tomographic data." Journal of synchrotron radiation 21.5 (2014): 1188-1193) using the algorithm from the ASTRA toolbox (Pelt, D. M., & Batenburg, K. J. (2015). Accurately approximating algebraic tomographic reconstruction by filtered back projection. In Proceedings of the 13th International Meeting on Fully Three-Dimensional Image Reconstruction in Radiology and Nuclear Medicine). Note that of course, the geometrical dimensions as well as the thickness of the 4 layers are compatible with the resolution of the nanotomography equipment (# 10 nm).

Lithium and Phosphorus contents within the Li_3PO_4 thin films were determined using an inductively coupled plasma atomic emission spectrometer (ICP-AES) by dissolving beforehand the films in (2/3 HNO_3 + 1/3 HCl) solution at 125°C. Small quantities of these solutions were analyzed.

Planar and 3D electrochemical testing: Electrochemical impedance spectroscopy (EIS) measurements were conducted with a Biologic VMP3 equipment over a frequency range from 10 Hz up to 500 KHz on Pt / Li_3PO_4 / Pt sandwich structures deposited on Si (100) substrates. The considered geometric area of the blocking electrodes was 0.18 cm^2 as defined by the intersection between the over and under layers of the Pt ribbons **(figure 5)**. Cyclic voltammetry (CV) and Galvanostatic Charge and Discharge Plots were investigated on the VMP3 potentiostat/galvanostat equipment using a homemade Teflon like flat cell with Li metal used as the counter and reference electrode. The electrolyte (1 mL), comprising 1 M Li(TFSI), where TFSI is the anion bis(t(trifluoromethanesulfonyl)imide), dissolved in ethylene carbonate (EC) and diethylene carbonate (DEC) in a 1:1 ratio, was poured into the flat-cell cavity. The tested area (circular shape) of the sample was limited to 0.785 cm^2. The

flat cells under test were placed in a glove box with controlled atmosphere (O_2 and H_2O quantities: less than 1 ppm).

Supporting Information
Supporting Information is available from the Wiley Online Library or from the author.

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Figures

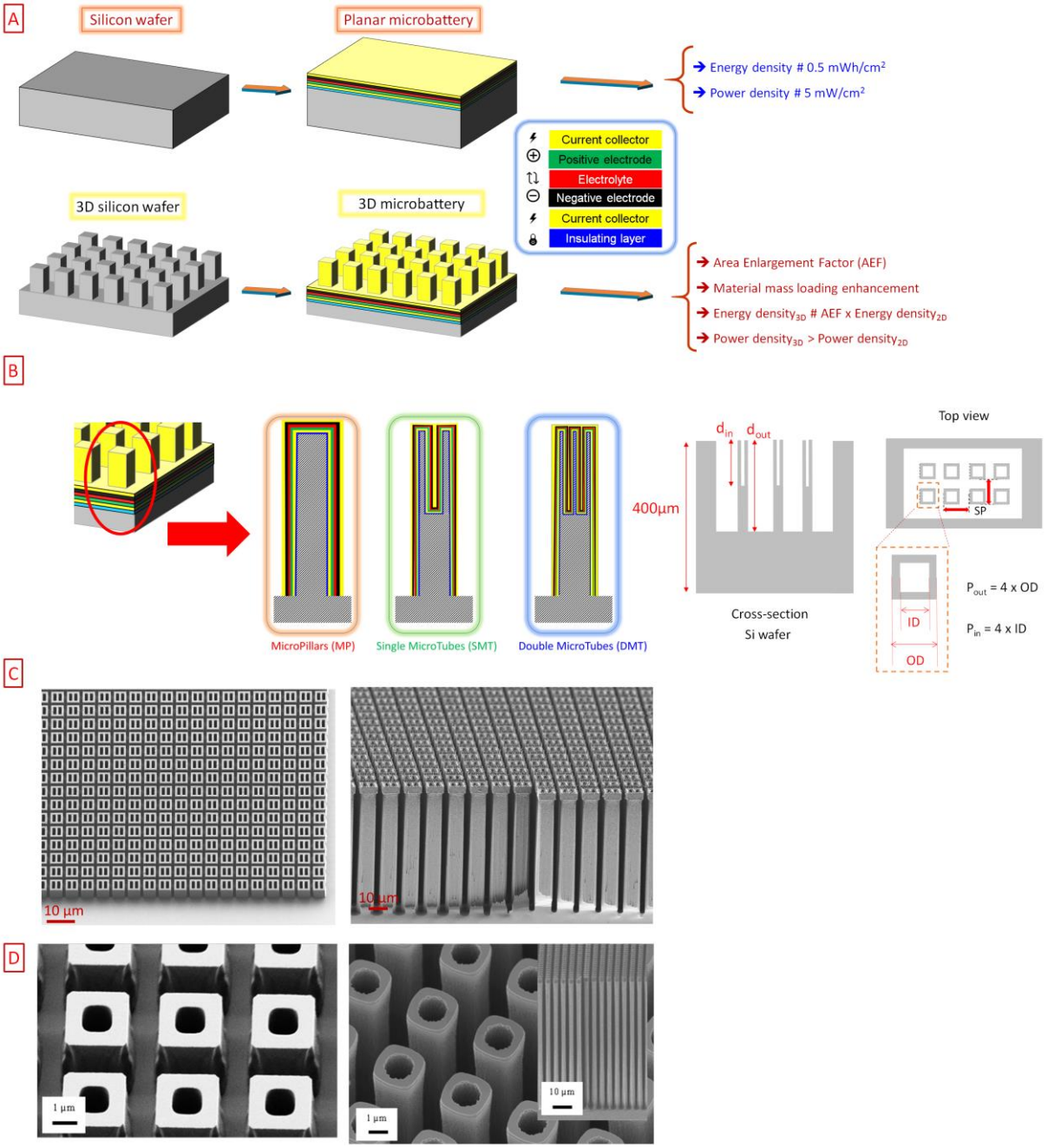

Figure 1 – **A.** Schematic of 2D and 3D microbatteries fabricated on silicon wafer. The concept of the proposed 3D lithium ion microbattery is developed at the wafer level: vertically aligned 3D microstructures are decorated by a six layers' stacking deposited by ALD (inset). A 3D scaffold is used to significantly improve the specific area, to enhance the material mass loading while keeping small the footprint area. In such way, the specific energy of 3D microbattery is significantly increased as compared to planar counterpart. The power density is improved as the layer thickness in 3D microbattery is lower than in 2D one. **B.** Description of the proposed 3D scaffold: micropillars, simple microtubes and double microtubes (MP, SMT and DMT) are successfully

fabricated on 3 inches silicon wafer. **C and D**. SEM micrographs of the fabricated DMT (SMT respectively): photoresist mask (left) and 3D silicon scaffold (right) after the deep reactive ion etching of the wafer selectively to the mask.

Table 1 – Parameters of the tested samples (planar and 3D topologies) for nanotomography and electrochemical analyses

Name	Φ_{out}-Φ_{in} (µm)	Spacing (µm)	Structure pitch (µm)	Etched depth (µm)	% of inner depth	Calculated AEF	Al_2O_3 Thickness (nm)	Pt Thickness (nm)	TiO_2 Thickness (nm)	Li_3PO_4 Thickness (nm)
S_{2D1}	-	-	-	-	-	1	120	40	55	-
S_{2D2}	-	-	-	-	-	1	120	40	55	40
MP	3	1	4	24	-		120	40	77	40
SMT	5 - 1	1	6	78	60	53	120	40	155	20
DMT	5 - 1	1	6	58	53	45	120	40	55	20

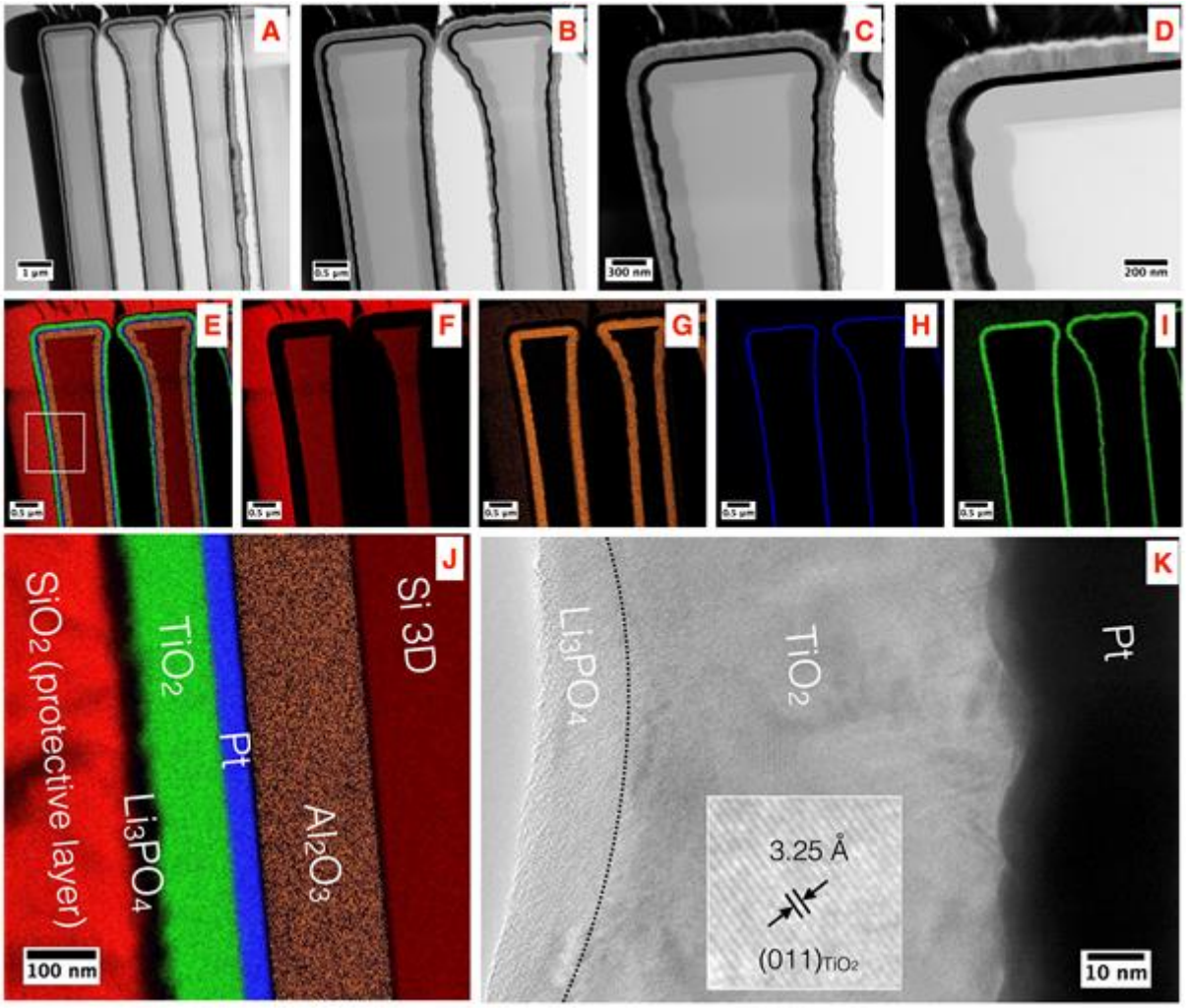

Figure 2 - (A-D) TEM images at different magnifications of a thin layer (milled by FIB) of the 3D double microtubes coated with the following $Al_2O_3/Pt/TiO_2/Li_3PO_4$ stacking layers. **(E-I)** EDX-STEM mapping of coated double microtubes exhibiting the localization of Si (red), Al (orange), Pt (blue) and Ti (green) elements. **(J)** Layer interfaces EDX-STEM elemental map of the stacked layers consisted of Si-3D/Al_2O_3/Pt/TiO_2/Li_3PO_4/SiO_2-protective. Li_3PO_4 layer, which cannot be detected using EDX probing, is clearly observed in between TiO_2 and SiO_2 layers. **(K)** High resolution TEM image showing Li_3PO_4 external layer, highly crystalline TiO_2 layer (inset exhibits lattice fringes corresponding to (011) of anatase TiO_2) and Pt layer.

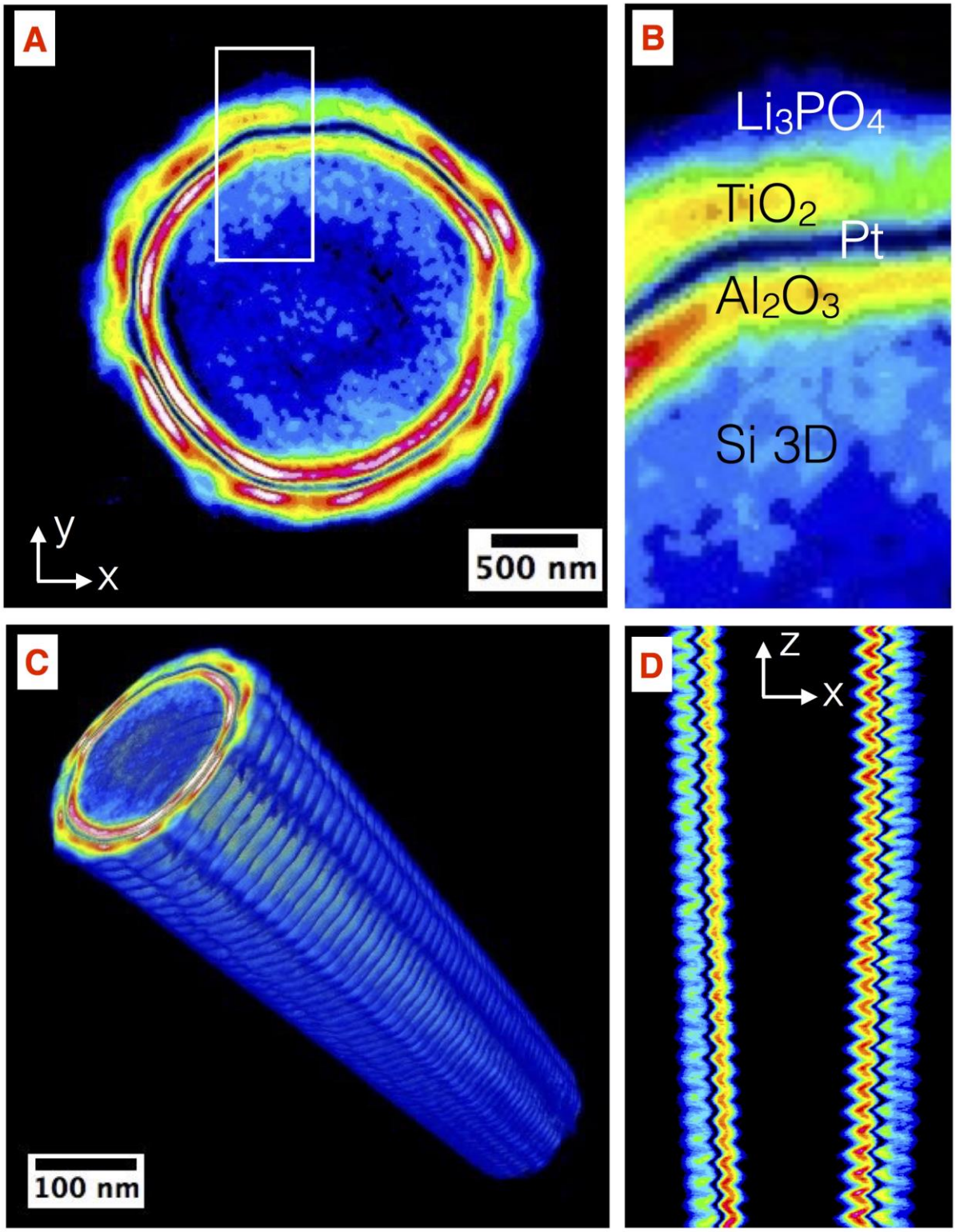

Figure 3 - (A) Top-view (TXM image) of a silicon micropillar coated with the four functional layers deposited by ALD. **(B)** The region in the white rectangles exhibits the 4 layers stacked on the 3D isolated microstructure in which etched silicon 3D micropillar, Al_2O_3, Pt, TiO_2 and Li_3PO_4 thin films can be distinguished by relative contrast and are consistent with the thickness measured by TEM on a microbattery exhibiting a concentric topology. **(C)** TXM tomography reconstruction of a single micropillar showing regular stripes at the surface

owing to the scalloping effect produced by the etching process. **(D)** Image (longitudinal projection) revealing stripe structure obtained from cross section of the micropillar following the xz plan.

Table 2 – Parameters and obtained results of the 5 tested LPO samples. The solid electrolyte deposited by ALD is in sandwich between two Pt blocking electrode. In this table, the surface resistance contribution as well as the ionic conductivities reached by the proposed electrolyte are summarized.

Name - T°C	Thickness (nm)	Surface (cm^2)	$R_{2\text{-fit}}$ (Ω)	Surface Resistance (Ω.cm^2)	$\sigma_{ionic\text{-fit}}$ (S/cm)	$\sigma_{ionic\text{-no fit}}$ (S/cm)
LPO_1 - 250	42	0.18	161.5	**29.07**	**1.44×10^{-7}**	
LPO_2 - 325	60	0.18	144	**25.92**	**2.31×10^{-7}**	
LPO_3 - 300	60	0.18	76.93	**13.85**	**4.33×10^{-7}**	**2.20×10^{-7}**
LPO_4 - 300	30	0.18	26.97	**4.85**	**6.18×10^{-7}**	**3.20×10^{-7}**
LPO_5 - 300	10	0.18	21.34	**3.84**	**2.60×10^{-7}**	**1.20×10^{-7}**

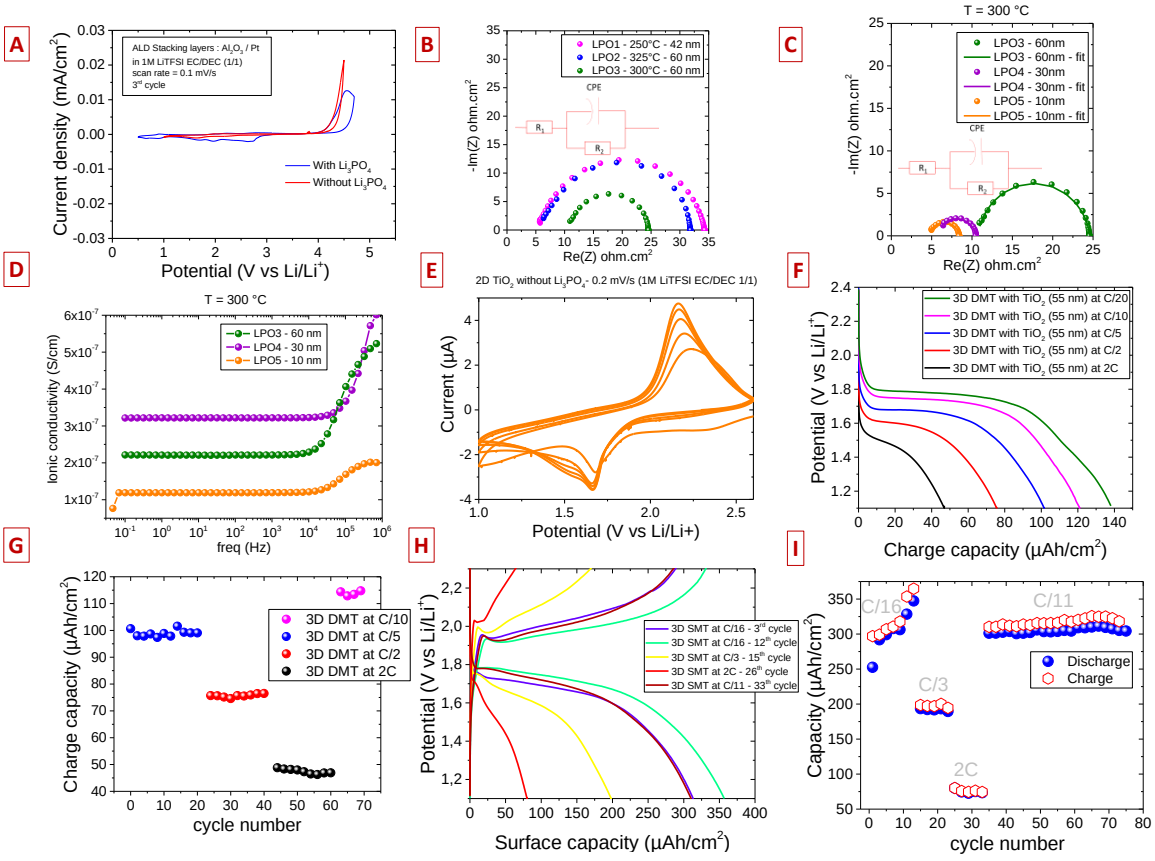

Figure 4 - A. Electrochemical window stability of the Li_3PO_4 solid electrolyte measured by cyclic voltammetry (0.1 mV/s) in liquid electrolyte between 0.5 and 4.7 V vs Li/Li^+: from this measurement, the Li_3PO_4 thin film (60 nm) is found to be stable at least over 4.2 V electrochemical window (S_6 and S_7 samples). The upper limit has

been set close to the decomposition of the 1M LiTFSI - EC/DEC (1/1) liquid electrolyte while the lower limit has been set above the lithium – platinum alloy. **B.** Electrochemical Impedance Spectroscopy curves of the Li_3PO_4 thin films regarding the operating temperature of the ALD reactor and the layer thickness. The Li_3PO_4 thin film is in sandwich between two blocking electrodes (Pt) and the methodology used to perform the measurement is similar to the Bates' study[36]. Evolution of the impedance plots as a function of the operating temperature (LPO_1 up to LPO_3 samples) of the ALD reactor: the equivalent circuit used to fit the semi-circles is reported in inset. **C.** Impedance plots of the Li_3PO_4 solid electrolyte deposited at 300 °C with different thicknesses (LPO_3 up to LPO_5 samples). **D.** Evolution of the ionic conductivity vs the frequency for the LPO_3, LPO_4 and LPO_5 samples. This method allows to obtain the ionic conductivity of the tested layers without performing a fit of the measurements. **E.** Cyclic voltammetry (CV) of planar TiO_2 based electrode (S_{2D1}) cycled in liquid electrolyte (1 M LiTFSi EC/DEC (1/1)) without the Li_3PO_4 solid electrolyte. The redox peaks at 1.7 and 2.1 V vs Li/Li^+ are attributed to the anatase polymorph. **F.** Evolution of the TiO_2 potential as a function charge surface capacity for the DMT sample at different C rate (from C/20 up to 2C). The TiO_2 thickness is constant in both cases (55 nm) and, from these measurements, the significant interest of the 3D fabricated scaffold is clearly highlighted. **G.** Surface capacity ($\mu Ah/cm^2$) of the DMT sample as a function of the number of cycles and at different C rate. **H.** Evolution of the charge and discharge surface capacities of the SMT sample as a function of the C rate (AEF = 53 and TiO_2 thickness = 155 nm). **I.** Charge and discharge capacities vs number of cycles at different C rate (respectively at C/16, C/3, 2C and C/11). The mass loading of the TiO_2 thin film is significantly improved by the 3D simple or double tubes scaffold and the Li_3PO_4 solid electrolyte deposited both on planar and 3D samples allows the conduction of the lithium ions from the liquid electrolyte to the TiO_2 layer. No dissolution of the Li_3PO_4 layer has been found after the electrochemical characterization.

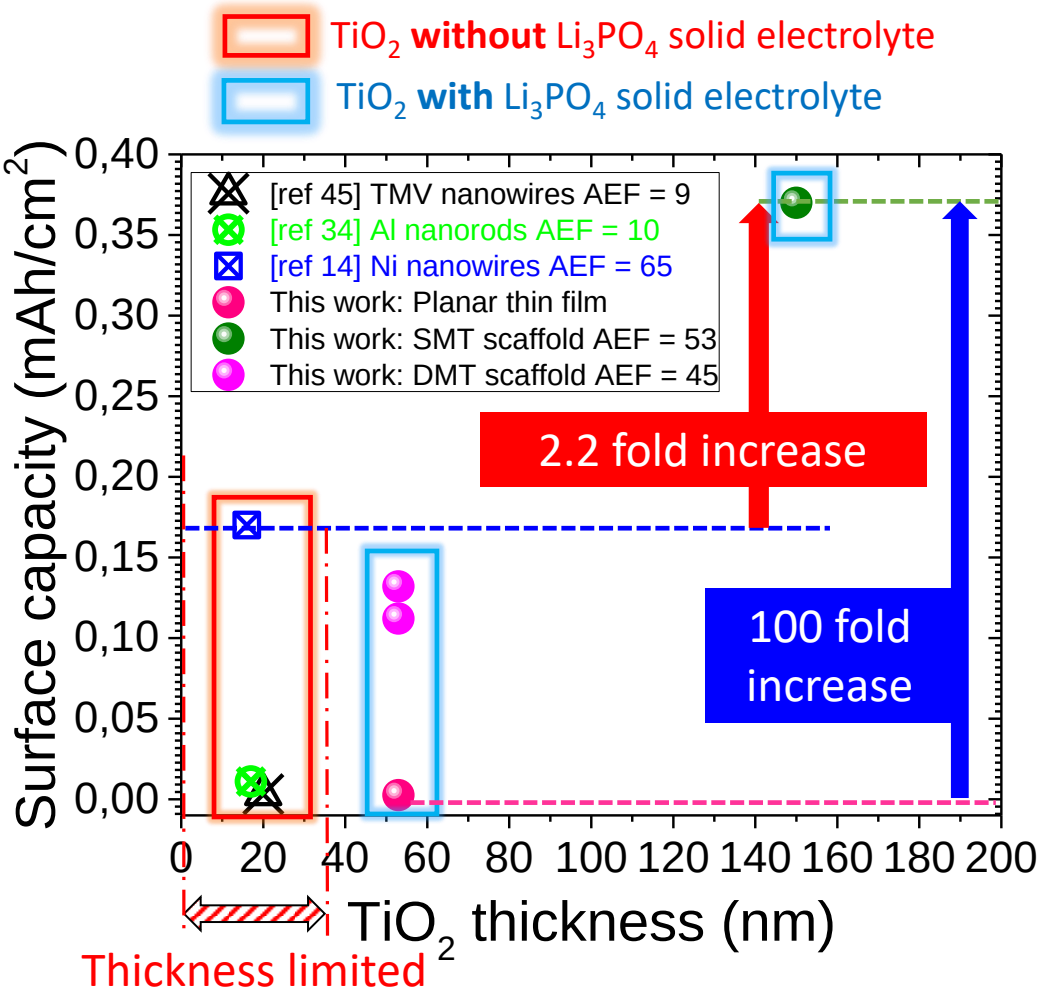

Figure 5 - Benchmarking of the proposed technology. Surface capacity of the 3D electrodes regarding the state of the art. To the best of the authors' knowledge, the 3D scaffolds tested in this letter and coated with TiO_2 – Li_3PO_4 thin films are the only electrode reaching this surface capacity (0.37 mAh/cm^2 at C/16) in a solid state configuration. The surface capacity is more than 2 times higher than the best published 3D capacity and 100 times higher than our planar TiO_2 thin film electrode.

Atomic layer Deposition of 4 functional pinhole free and thin layers has been performed on highly robust and efficient 3D silicon microtubes scaffold exhibiting an area enhancement factor value close to 55. In depth study of the interfaces between each layer is proposed by combining Transmission Electron Microscope and synchrotron X-Ray nanotomography analyses. A complete study of the Li_3PO_4 solid electrolyte developed by ALD is proposed in this paper. Pinhole free, thin and dense Li_3PO_4 layer exhibits the highest ionic conductivity (6.2 x 10^{-7} S/cm) and the lowest area specific resistance (3.8 Ω.cm^2) reported for an ALD solid electrolyte. The electrochemical window is found greater than 4.2 V and an excellent conformality of the thin films deposition is proposed. The areal capacity of TiO_2 electrode move from 3.5 µAh/cm^2 for planar thin film up to 0.37 mAh/cm^2 for thin layer deposited on 3D template and coated with a step conformal solid electrolyte Li_3PO_4.

Keyword: Atomic Layer Depostion, solid electrolyte, 3D microbattery, double microtube, high areal capacity

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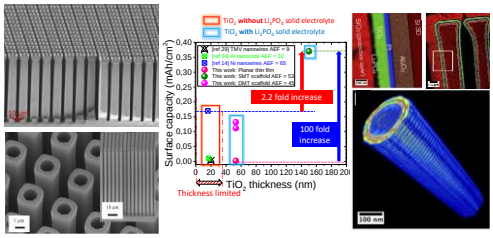
Atomic Layer Deposition of functional layers for on chip 3D Li-ion all solid state microbattery



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