Investigation of the UTB-InAs-MOSFETs structure

Sofiane Ammi, Abdelkader Aissat, Nicolas Wichmann, S. Bollaert

Investigation of the UTB-InAs-MOSFETs Structure

Sofiane Ammi[1], Abdelkader Aissat[1,2], Nicolas Wichmann[2], Sylvain Bollaert[2]
[1] Faculty of Technology University Blida.1.09000, Blida, Algeria
[2]Electronic microelectronic and nanotechnology institute (IEMN), UMR CNRS 8520, University of Sciences and Technologies de Lille 1. Poincare Avenue´, PB 60069, *59652* Villeneuve d'Ascq, France
email: sakre23@yahoo.fr

Abstract

An Ultra-Thin-Body (UTB) InP/InAs/InGaAs MOSFETs is investigated. Computer Aided Design(CAD) tools are used to extract the electrical properties of this structure.Our simulation work gives us the possibility to extract the output characteristics, transfer characteristics and RF performances. With the small-signal equivalent circuit models, intrinsic elements are calculated from the Y- parameters matrix using AC analysis. To further improve the accuracy of the simulation, the effect of doping in the channel and source-drain regions, the Indium content in different layers are discussed and optimized. The results arevalidated withdevice characteristics of the fabricated 150 nm InP/InAs/InGaAs MOSFET. A high drain current of 665 mA/mm and extrinsic peak transconductance of 440 mS/mm are obtained at V_{ds}=0.7V. A current gain cutoff frequency f_T of 41.69 GHz and a simultaneous maximum oscillation frequency f_{max} of 94 GHz are estimated at V_{ds}=0.7V and V_{gs}=0.2V.

Keywords: III-V Semiconductor, UTB-InAs-MOSFET, electrical characteristics, simulation, TCAD tools.

1. Introduction

The spectacular microelectronics revolution has been occurred by the nearly ideal properties of silicon dioxide and its interface with silicon. Continually thinner gate oxides have been a critical feature of the overall scaling of transistor dimensions for three decades, enabling continued speed improvement even as operating voltages decrease. This era of scaling in thickness of a silicon dioxide insulator will soon come to an end, as gate tunneling current, reduced reliability, and diminishing returns in speed make further reductions impossible or unrewarding [1].

The other limitation of MOSFET scaling is excess off-state leakage. High off-state leakage current can occur from a largesubthreshold leakage due to worse electrostatics, or from the tunneling leakage caused by large electric field in the oxides and the channels [2]. Several new technologies have been proposed to conquer these limitations such as high-k dielectrics [3], metal gate electrodes [4], stressors [5], and new transistor architectures based on silicon-on-insulator (SOI), such as Fin FETs [6], Junctionless transistors [7] or gate-all-around FETs [8]. Reducing these leakage currents in nanoscale MOSFETs is of great importance for continuous device scaling, particularly for low standby power logic applications and the battery-driven mobile electronics. Recently, new channel materials such as III-V compound semiconductors have drawn great attention because of their superior transport properties [9]. III-V InGaAs/InAs materials are considered as promising candidates for replacing Si-based MOSFETs for future very-large-scale integration logic applications. III-V InGaAs/InAs

materials have smaller electron effective mass (m^* ~ 0.041 for $In_{0.53}Ga_{0.47}As$ and m^*~ 0.026 for InAs) than Si channels (m^*~ 0.19) [10,11]. Smaller electron effective mass providesexcellent transport properties, as evidenced by high electron mobility ($\mu \sim 1/m^*$) and high injection velocity ($v_{inj} \sim \sqrt{1/m^*}$). In InGaAs or InAs, the electron mobility is more than 10 times higher than in silicon, which could deliver higher I_{on} at lower supply voltages [12], they are also known to have low contact resistance [13].Today much of the development of semiconductor devices and processes is done by computer modeling. The approach is called TCAD (Technology-Computer Aided Design). Uses of TCAD tools reduce the development cost and shorten the development time.

In this paper, we have used TCAD software for modeling and simulating the electrical performance of an Ultra-thin body InAs MOSFET structure. The simulation is based on solving the Poisson equation and carrier continuity equations based on the conventional drift-diffusion transport model with Fermi-Dirac statistics, Shockley-Read-Hall (SRH) recombination model and electric field-dependent mobility model [14]. The results are presented as current-voltage curves, RF performances and a table of the extracted intrinsic elements. Simulated output characteristics and transfer characteristics of the InP/InAs/InGaAs MOSFET have been compared to experimental data of the fabricated 150 nm InP/InAs/InGaAs MOSFET.

2. Theoretical Model

Equations (1) to (11) summarize the necessary equations for the constitution of our code. The simulation begins with the resolution of Poisson equation given by:

$$\nabla^2 V = -\frac{\rho}{\varepsilon} \qquad (1)$$

Where ∇ is the divergence operator, V is the electrostatic potential, $\varepsilon$is the material-dependent permittivity and $\rho$is the charge density described by:

$$\rho = p - n + N_D^+ - N_A^- \qquad (2)$$

Where n and p are the electron and hole density, N_D^+ and N_A^- are, respectively, the ionized donor and the acceptor density concentration.

The continuity equations used are (3) and (4), where n and p are the electron and hole concentration, J_n and J_p are the electron and hole current densities, G and R are the generation and recombination rates for the carriers, and q is the elementary charge.

$$\frac{\partial n}{\partial t} = -\frac{\nabla \overrightarrow{J_n}}{q} + G_n - R_n \qquad (3)$$

$$\frac{\partial p}{\partial t} = -\frac{\nabla \overrightarrow{J_p}}{q} + G_p - R_p \qquad (4)$$

The continuity equations may be approximated by a drift-diffusion model [14], the current densities are expressed as:

$$\vec{J}_n = q.n.\mu_n.\vec{E} + q.D_n.\vec{\nabla}_n \quad (5)$$

$$\vec{J}_p = q.p.\mu_p.\vec{E} + q.D_p.\vec{\nabla}_p \quad (6)$$

D_n and D_p are the diffusion coefficients for electrons and holes, μ_n and μ_p are the carrier mobilities which depend on the parallel electric field $\overrightarrow{E}$, [14].

In this work, the drift-diffusion model is used with Fermi-Dirac statistics [15,16].The Shockley-Read-Hall(SRH) recombination is being used to simulate band gap transitions [17,18].

The small-signal equivalent circuit used for modeling the MOSFET and extraction of *S* and *Y* parameters is depicted in figure 1. The solid-line rectangle encloses the equivalent circuit of the intrinsic MOSFET device.

The current gain H_{21} of a transistor can be calculated from the *S* parameters using the following expression:

$$|H_{21}|^2 = \left|\frac{-2.S_{21}}{(1-S_{11}).(1+S_{22})+S_{12}.S_{21}}\right|^2 \quad (7)$$

The gain evolution of -20dB/decade determine the transition frequency, f_T, corresponding to $|H_{21}| = 1$ (0 dB).

The unilateral power gain is expressed as follows:

$$U = \frac{\left|\frac{S_{21}}{S_{12}} - 1\right|^2}{2.\left(k\left|\frac{S_{21}}{S_{12}}\right| - Re\left|\frac{S_{21}}{S_{12}}\right|\right)} \quad (8)$$

k is the stability factor given by:

$$k = \frac{1-|S_{22}|^2-|S_{11}|^2+|S_{11}S_{22}-S_{12}S_{21}|^2}{2.|S_{12}|.|S_{21}|} \quad (9)$$

When U=1 (0 dB), we can get the maximum oscillation frequency, f_{max}.

The corresponding *Y*-parameter matrix is [19]:

$$Y_{ij} = \begin{bmatrix} \frac{jC_{gs}\omega}{1+jR_iC_{gs}} + jC_{gd}\omega & -jC_{gd}\omega \\ \frac{G_m e^{-j\omega t}}{1+jR_iC_{gs}} - jC_{gd}\omega & G_d + jC_{ds}\omega + jC_{gd}\omega \end{bmatrix} \quad (10)$$

The intrinsic elements such as G_m, G_d, τ, R_i, C_{gs}, C_{gd} and C_{ds} are calculated from Y_{ij} using the formulas below:

$$\begin{cases} G_m = -\left|\frac{Y_{21}-Y_{12}}{Y_{11}+Y_{12}}\right| \frac{1}{Im\left(\frac{1}{Y_{11}+Y_{12}}\right)} \\ G_d = Re(Y_{22}) \\ \tau = -\frac{1}{\omega}\left(arg\left(\frac{Y_{21}-Y_{12}}{Y_{11}+Y_{12}}\right)+\frac{\pi}{2}\right) \\ R_i = Re\left(\frac{1}{Y_{11}+Y_{12}}\right) \\ C_{gs} = -\frac{1}{\omega Im\left(\frac{1}{Y_{11}+Y_{12}}\right)} \\ C_{gd} = -\frac{Im(Y_{12})}{\omega} \\ C_{ds} = \frac{Im(Y_{22}+Y_{12})}{\omega} \end{cases} \quad (11)$$

3. Results and Discussion

The schematic view of simulated UTB-InAs-MOSFET structure is shown in figure 2. From bottom to top the InP/InAs/InGaAs layers structure simulated consists of a semi-insulating InP substrate, a 300 nm unintentionally doped (U.I.D) $In_{0.52}Al_{0.48}As$ buffer layer, the channel was composed of a 3 nm U.I.D $In_{0.53}Ga_{0.47}As$/ 3 nm U.I.D InAs for highest mobility, a 3 nm U.I.D InP layer acting as an insulating layer (InP is a wide band gap semiconductor material) and the final high-*k* gate oxide Al_2O_3 layer is a 4 nm thickness.

The choice of indium concentration on the $In_xGa_{1-x}As$ structure can be shown in figure 3. We see that for a value of x = 0.53, the strain and ΔE_g at the InAs / InGaAs interface have a value of 3% and 0.38 eV respectively, if we want to improve it, we must have a lower ΔE_g which increases the leakage current [20]. In the case of $In_xGa_{1-x}As/In_yAl_{1-y}As$ interface, the lattice matched condition (x,y) assures the following equation y(x) =1.02.x-0.02, where (x=0.53, y=0.52) verify this equation.

The gate length of simulated structure is 150nm with U.I.D because we have seen that by doping the channel a current I_d increased slightly (figure 4-a) but there will be a deterioration of the subthreshold slope which increase the leakage current (figure 4-b). The source and drain access regions are heavily n-doped for $N_D = 10^{19}$ cm^{-3}, this value gives an optimal I_d current (figure 5). Ideally, the transistor that is most needed is equipped with a high drive current and low subthreshold voltage swing, which improve the switching speed of SOI MOSFET device. Using an oxide barrier or a wide band gap semiconductor barrier will potentially reduce the barrier leakage current [21]. This UTB structure is chosen to reduce leakage current and to maintain good control of the electron in the channel [22]. Epitaxial layers are grown by molecular beam epitaxy in which composition is similar to figure 2.This is a gate first self-aligned MOSFET architecture, in which gate electrode is used as a mask for ohmic contact definition. The Al_2O_3 gate oxide with a thickness of 4nm is deposited by atomic layer deposition (ALD). Ohmic contact is performed by nickel (Ni) salicide like process [23] to form Ni-epilayer alloy. Experimental measurement is performed using HP 4142B modular DC source/monitor unit at room temperature on 150 nm gate-length MOSFET [24]. Experimental data fitting can be done by adjusting transfer characteristic in the saturated region with altering the saturation velocity, threshold voltage with the work function, then the output characteristics by modifying the low field mobility and adding a resistance to each contact that correlate to the value measured on the real device (Table 1).

The drain current I_d is plotted against drain-source voltage V_{ds} in figure 6 with the gate voltage varying from -1 to 1V in a steps of 0.5V and a gate length of L_g = 150 nm. It can be seen that I_d reaches the value of

630 mA/mm at V_{ds}=0.7V and V_{gs}=1 V. The characteristics I_d-V_{gs} (black solid points) and corresponding transconductance (blue solid points), G_m, of UTB-InAs MOSFET are shown in figure 7 with L_g=150 nm at constant V_{ds} = 0.7 V. The current drain I_d and $G_{m(max)}$ reach to 665 mA/mm and 440 mS/mm, respectively. Figure 8 shows a comparison of the I_d-V_d characteristics of a 150nm gate length UTB-InAs-MOSFET structure between simulation results (solid stars) and experimental data (solid circles) [24].We calculate the correlation coefficient; we find a value of 0.96, a value that is close to 1 which means that there is a good agreement between the experimental results and our simulation. In figure 9 (the left y axis), we compare the I_d-V_{gs} characteristics at V_{ds}=0.7 V and L_g=150 nm. The results are compared between real device measurement (lines dotted) and device simulation (solid star lines) and the correlation coefficient is equal to 0.99. The transconductance, G_m is also shown in the same figure 9 on the right y axis. The plots show agreement with measured data. S-parameter simulations were performed up to 50 GHz. Figure 10 represents the current gain $|H_{21}|^2$ as a function of frequency at V_{ds}=0.7 V, V_{gs}=0.2 V and L_g= 150 nm. The cutoff frequency, f_T, of the simulated device is estimated by extrapolating the low-frequency current gain to unity at −20 dB/decade. As shown in figure 10, the cutoff frequency is found to be f_T=41.69 GHz. Figure 11 represents the variation of unilateral power gain, U_g, with respect to frequency at V_{ds}=0.7 V, V_{gs}=0.2 V and L_g= 150 nm. The maximum frequency of oscillations, f_{max}, of simulated UTB-InAs-MOSFET structure was estimated to be f_{max}= 94 GHz. Using small signal equivalent circuit model (figure 1) and equations (10,11), the intrinsic elements such as G_m, G_d, τ, R_i, C_{gs}, C_{gd} and C_{ds} can be extracted and are summarized in Table 2. We note that maximum of G_m with DC simulation (G_m=420 mS/mm) has approximately the same value as the one obtained by AC simulation (G_m=414 mS/mm).

4. Conclusion

In this paper, a 150 nm gate UTB-InAs MOSFET has been investigated. To analyze the DC performance of this structure, numerical simulation was carried out using TCAD tools. We developed a code to resolve the Poisson and carrier continuity equations based on the conventional drift-diffusion model of charge transport with Fermi-Dirac statistics, Shockley-Read-Hall (SRH) recombination and electric field-dependent mobility models. Our work gives us also the possibility to simulate the dynamic performances and to extract intrinsic elements with the small-signal equivalent circuit models. The doping in a channel and source-drain regions, the indium content in different layers are discussed and optimized. The results are validated with device characteristics of the fabricated 150 nm InP/InAs/InGaAs MOSFET. Drain current of 665 mA/mm, transconductance of 440 mS/mm are obtained at V_{ds}=0.7V and cutoff frequency of 41.69 GHz, maximum oscillation frequency of 94 GHz are estimated at V_{ds}=0.7V and V_{gs}=0.2V.

References

[2] M. Koh, W. Mizubayashi, K. Iwamoto, H. Murakani, T. Ono, M. Tsuno, T. mihara, K. Shibahara, S. Miyazaki and M. Hirose, “Limit of gate oxide thickness scaling in MOSFETs due to apparent threshold voltage fluctuation induced by tunnel leakage current,” IEEE Tans Electron Device, vol. 48, (2001) 259-264.

[3] J. P. de Souza, E. Kiewra, Y. Sun, A. Callegari, D. K. Sadana, G. Shahidi, D. J. Webb, J. Fompeyrine, R. Germann, C. Rossel and C. Marchiori,“Inversion mode n-channel GaAs field effect transistor with high-k/metal gate,” *J. Appl. Phys. Lett.*, vol. 92, (2008) 153508.1-2.

[4] R. Chau, S. Datta, M. Doczy, B. Doyle, J. Kavalieros, and M. Metz, “High-*k*/metal gate stack and its MOSFET characteristics,” *IEEE Electron Device Lett.*, vol. 25, (2004) 408-410.

[5] Y. Song, H. Zhou, Q. Xu, J. Luo, H. Yin, J. Yan, and H. Zhong, “Mobility enhancement technology for scaling of CMOS devices: overview and status,” *Journal of Electronic Materials*, vol. 40, (2011), pp. 1584-1612.

[6] G. P. Lansbergen, R. Rahman, C. J. Wellard, I. Woo, J. Caro, N. Collaert, S. Biesemans, G. Klimeck, L. C. L. Hollenberg and S. Rogge, “Gate-induced quantum-confinement transition of a single dopant atom in a silicon Fin FET,” *Nature Physics*, vol. 4, (2008) 656-661.

[7] A. Dehzangi, A. M. Abdullah, F. Larki, S. D. Hutagalung, E. B. Saion, M. N. Hamidon, J. Hassan and Y. Gharayebi, “Electrical property comparison and charge transmission in p-type double gate and single gate junction less accumulation transistor fabricated by AFM nanolithography,” *Nanoscale Research Letters*, vol. 7, (2012), 1-9.

[8] B. Yang, K. D. Buddharaju, S. H. G. Teo, N. Singh, G. Q. Lo and D. L. Kwong, “Vertical silicon-nanowire formation and gate-all-around MOSFET,” *IEEE Electron Device Lett.*, vol. 29, (2008) 791-794.

[9]Y. Liu, H. Pal, M. Lundstrom, D. H. Kim, J. A. Del Alamo, and D. A. Antoniadis, "Device Physics and Performance Potential of III-V Field-Effect Transistors," *In: S. Oktyabrsky, P. D. Ye, editors. Fundamentals of III–V Semiconductor MOSFETs, New York: Springer*, (2010) 31-50.

[10] C. Wetzel, R. Winkler, M. Drechsler, B. K. Meyer, U. Rossler, J. Scriba, J. P. Kotthaus, V. Harle and F. Scholz,“Electron effective mass and nonparabolicity in $Ga_{0.47}In_{0.53}As$/InP quantum wells,” *Physical Review B*, vol. 53, (1996) 1038-1041.

[11] I. Vurgaftman, J. R. Meyer and L. R Ram-Mohan, “Band parameters for III–V compound semiconductors and their alloys,” *J. Appl. Phys.*, vol. 89, (2001) 5815-5875.

[12] T. Krishnamohan, D. Kim, K. C. Saraswat, "Properties and Trade-Offs of Compound Semiconductor MOSFETs," *In: Oktyabrsky S, Ye PD, editors. Fundamentals of III–V Semiconductor MOSFETs, New York: Springer*, (2010) 7-27.

[13] S. H. Kim, M. Yokoyama, R. Nakane, O. Ichikawa, T. Osada, M. Hata, M. Takenaka and S. Takagi, "high-Performance InAs-On-Insulator n-MOSFET with Ni-InGaAs S/D Realized by Contact Resistance Reduction Technology," *IEEE Transactions On Electron Devices*, vol. 60, (2013) 3342-3350.

[14] R. E. Bank, D. J. Rose and W. Fichtner, "Numerical Methods for Semiconductor Device Simulation," *IEEE Transactions on Electron Devices*, vol. 30, (1983)1031-1041.

[15] S. Selberherr, "Analysis and Simulation of Semiconductor Devices," *Springer-Verlag Wien, New York*, 1984.

[16] R. Kim, M. S. Lundstrom, "Notes on Fermi-Dirac Integrals 3rd Edition," *Network for Computational Nanotechnology*,Purdue University, 2008.

[17] W. Shockley, W. T. Read, "Statistics of the Recombination of Holes and Electrons," *Phys. Rev.*, vol. 87,(1952) 835-842.

[18] R. N. Hall, "Electron Hole Recombination in Germanium," *Phys. Rev.*, vol. 87, (1952)387.

[19] G. Dambrine, A. Cappy, F. Héliodore and E. Playez, "A new method for determining the FET small signal equivalent circuit," *IEEE Trans. Microwave Theory Tech.*, vol. 36, (1988) 1151-1159.

[20] A. Aissat, S. Nacer, F. Ykhlef , J.P. Vilcot, "Modeling of $Ga_{1-x}In_xAs_{1-y-z}N_ySb_z$/GaAs quantum well properties for near-infrared lasers," Materials Science in Semiconductor Processing vol. 16, (2013) 1936–1942

[21] J. Millán, P. Godignon and A. P. Tomás, "Wide Band Gap Semiconductor Devices for Power Electronics," *ATKAFF*, vol. 53, (2012) 107-116.

[22] J. G. Fossum, V. P. Trivedi, "Fundamentals of Ultra-Thin-Body MOSFETs and FinFETs,"*1st edition Cambridge University Press*, (2013) pp103-136.

[23] X. Zhang, H. Guo, X. Gong, Q. Zhou, Y. R. Lin, H. Y. Lin, C.H. Ko, C. H. Wann and Y.C. Yeo,"$In_{0.7}Ga_{0.3}As$ Channel n-MOSFET with Self-Aligned Ni–InGaAs Source and Drain," *Electrochemical and Solid-State Letters*, vol. 14, (2011) H60-H62.

[24] M. Ridaoui, M. Pastorek, A. B. D. Fadjie, N. Wichmann, A. Jaouad, H. Maher and S. Bollaert, "Ultra-Thin-Body InAs-MOSFETs with elevated Source/Drain contacts,"*Compound Semiconductor Week, Toyama, Japan*, IEEE Xplore, 2016.

Figures Caption

Figure 1. Conventional small-signal MOSFET model.

Figure 2. Schematic cross-sectional view of ultra-thin body InAs MOSFET.

Figure 3. Evolution of the strain and ΔE_g versus Indium fraction for InAs / $In_xGa_{1-x}As$.

Figure 4. (a) Evolution of drain current versus the channel area doping at V_{ds}=0.7V and V_{gs}=0.5V.

(b) Evolution of drain current below the threshold versus gate-source voltage at different channel area doping.

Figure 5. Evolution of drain current versus the Source-Drain region doping at V_{ds}=0.7V and V_{gs}=0.5V.

Figure 6. Drain current (I_d) variation versus drain voltage-source (V_{ds}) at different gate-source voltage (V_{gs}) and L_g =150 nm.

Figure 7. Variation of drain current (black solid points) and transconductance (blue solid points) with respect to gate-source voltage at constant V_{ds} = 0.7 V and L_g =150 nm.

Figure8. Comparison of the I_d-V_d characteristics of real device measurement (solid circles) and device simulation (solid stars) at different gate voltage and L_g=150 nm.

Figure 9. Comparison of experimental (dotted lines) and simulation data (solid star lines) of I_d-V_{gs} and corresponding transconductance characteristics with respect to V_{gs} at V_{ds}=0.7V and L_g =150 nm.

Figure 10. Variation of current gain $|H_{21}|^2$ versus frequency atV_{ds}=0.7 V, V_{gs}=0.2 V and L_g=150 nm.

Figure 11. Variation of unilateral power gain U_g versus frequency at V_{ds}=0.7 V, V_{gs}=0.2 V and L_g=150 nm.

Table 1. The physical parameters used in the simulation

Table 2. The intrinsic small-signal circuit components extracted from simulation at V_{ds}=0.7 V and L_g=150 nm.

Figure1:

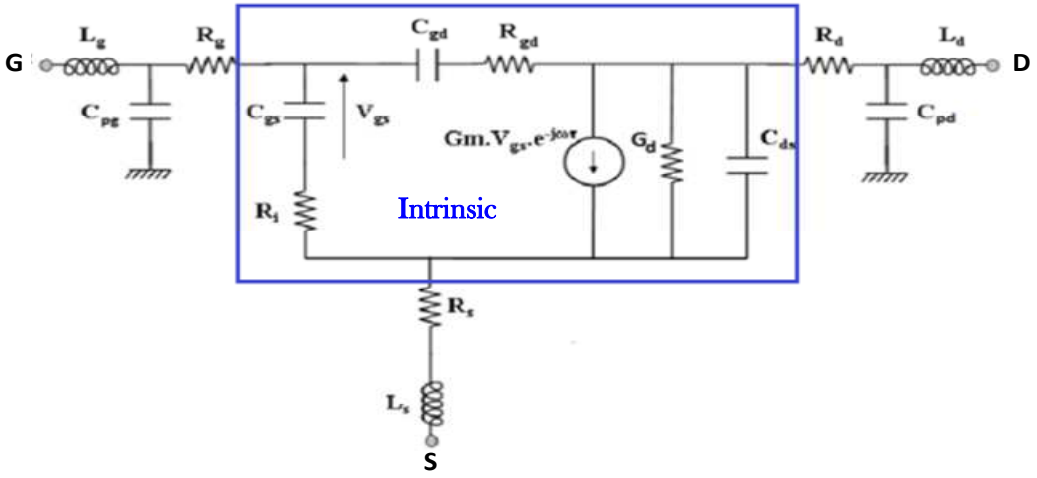

Figure 2:

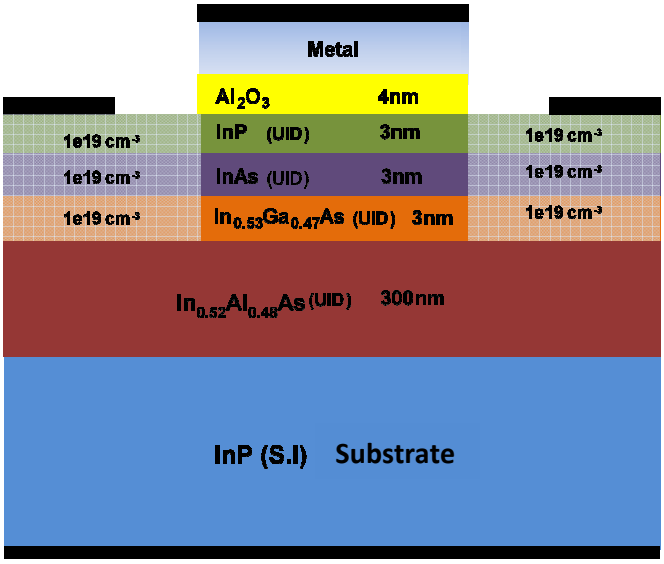

Figure 3:

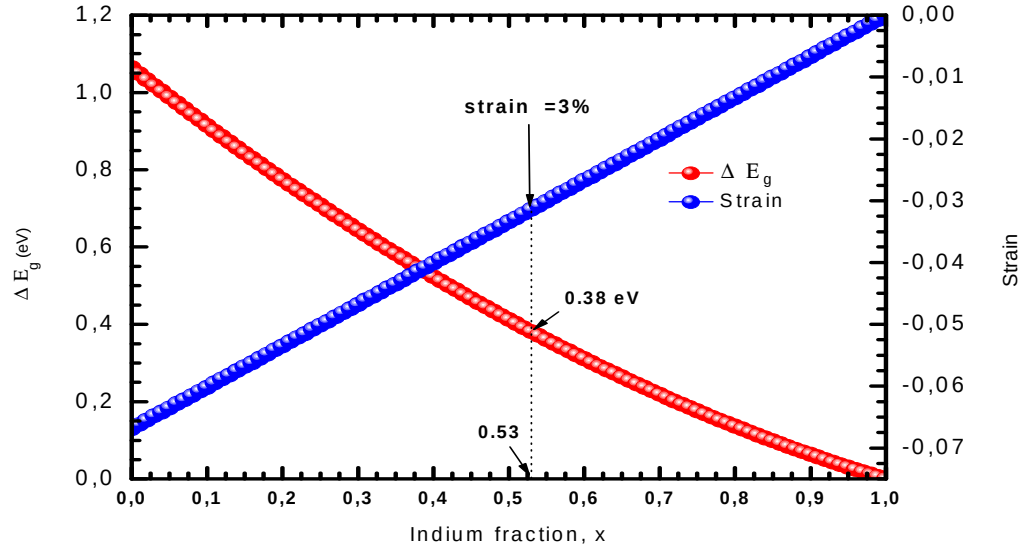

Figure 4 (a,b):

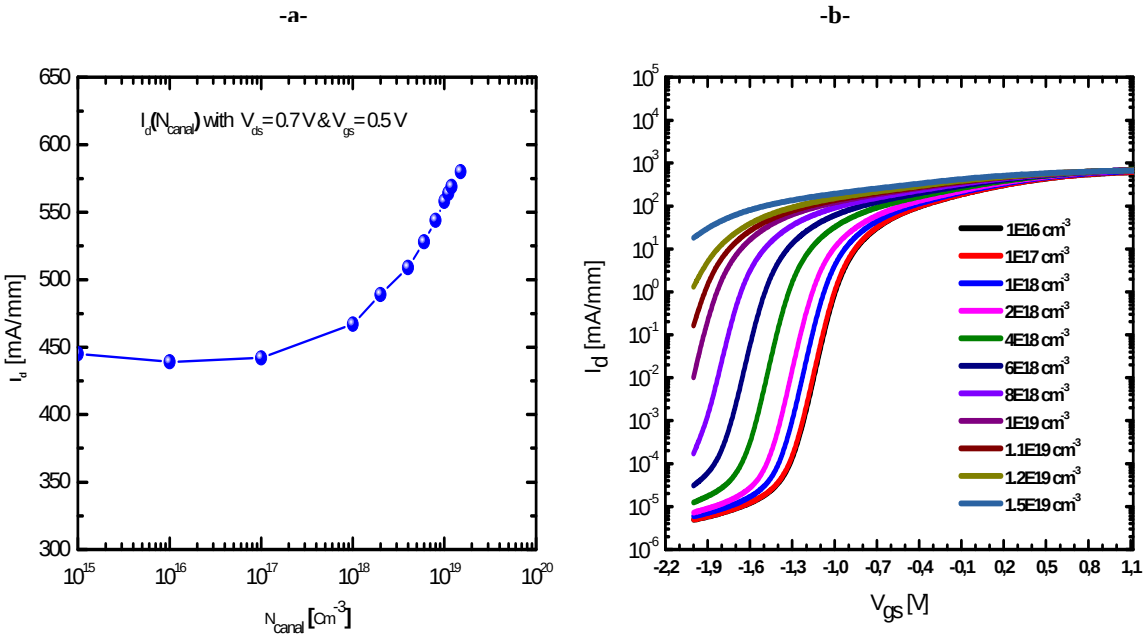

Figure 5:

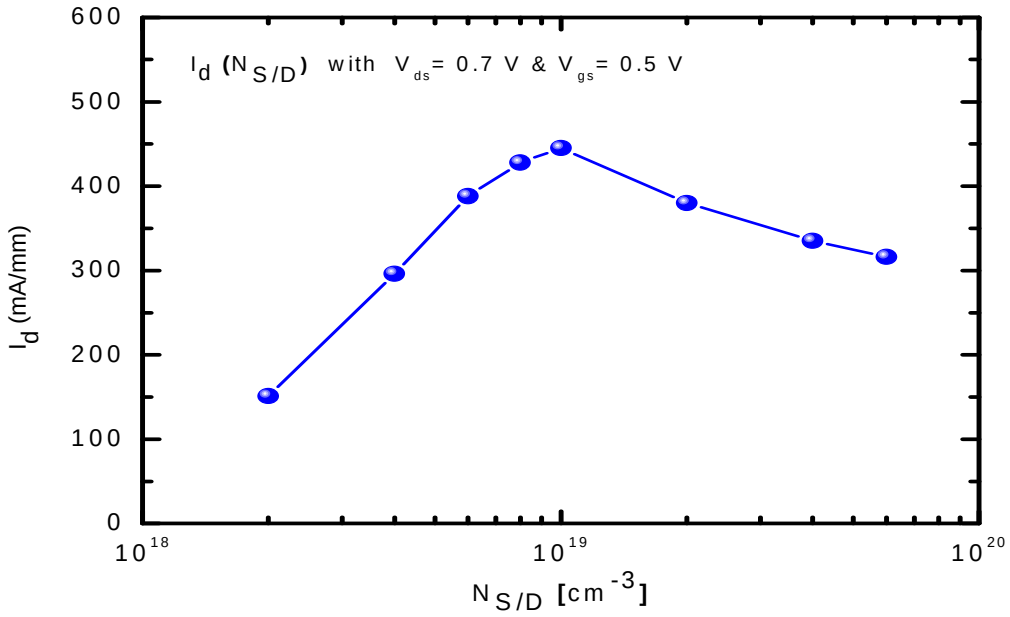
I_d ($N_{S/D}$) with V_{ds}= 0.7 V & V_{gs}= 0.5 V
600
500
400
300
200
100
0
I_d (mA/mm)
10^{18}
10^{19}
10^{20}
$N_{S/D}$ [cm^{-3}]

Figure 6:

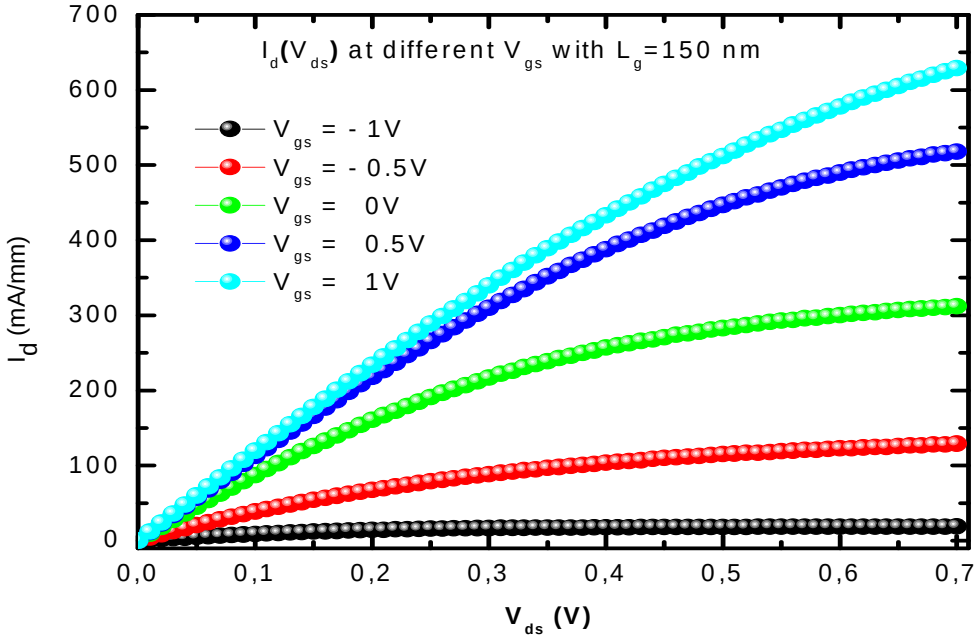

Figure 7:

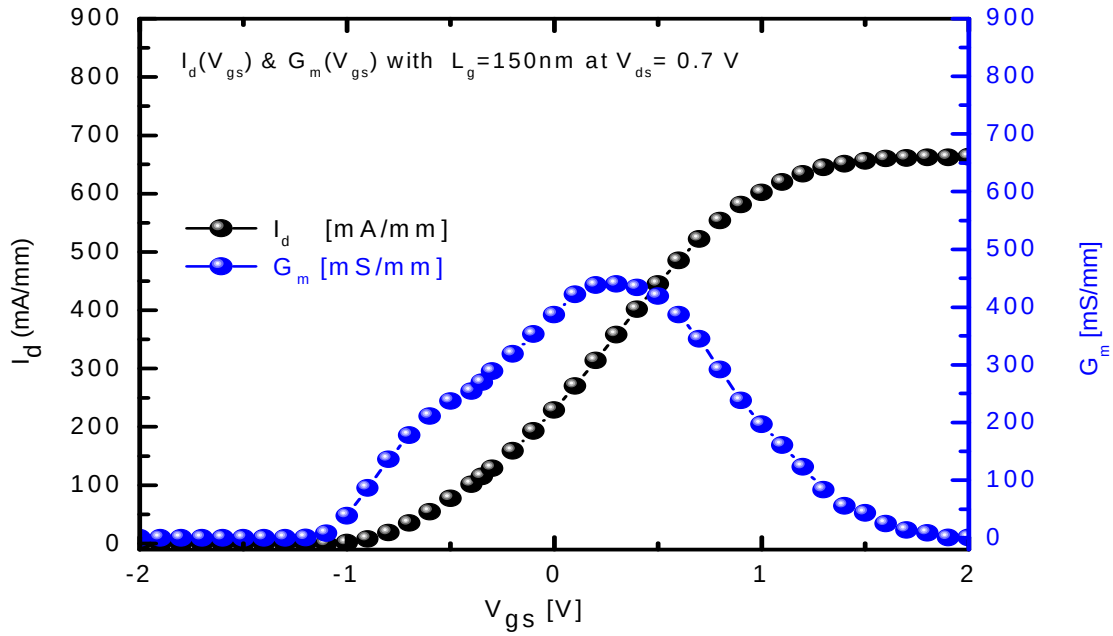

Figure 8:

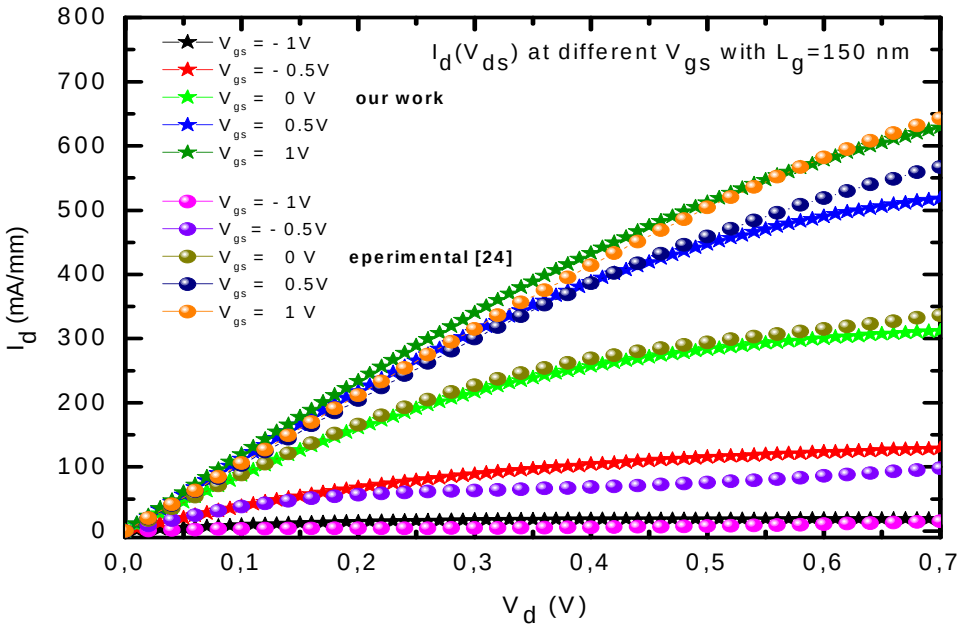

Figure 9:

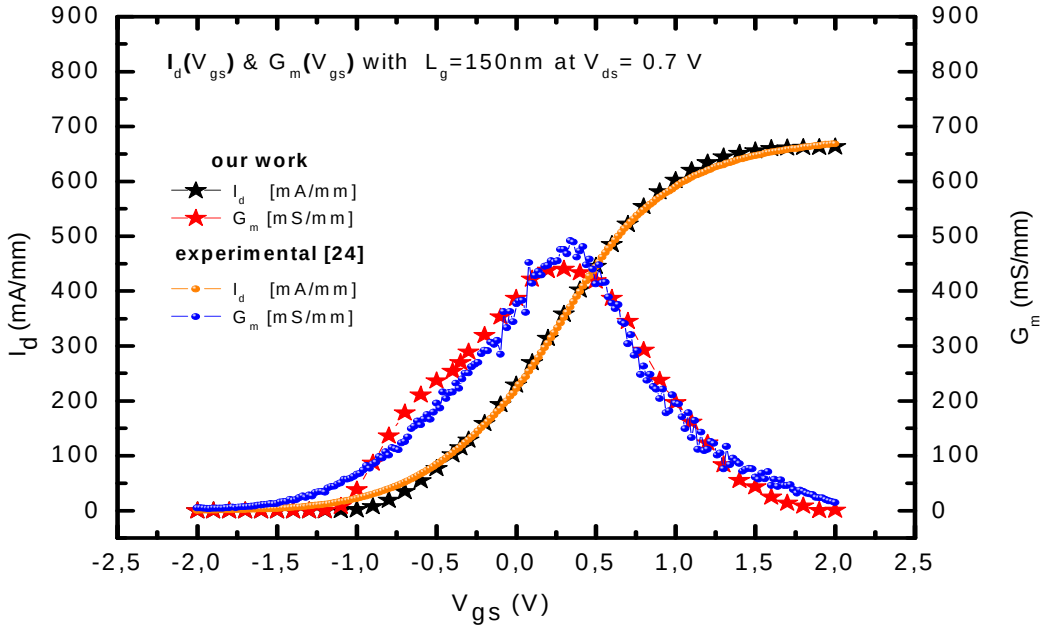

Figure 10:

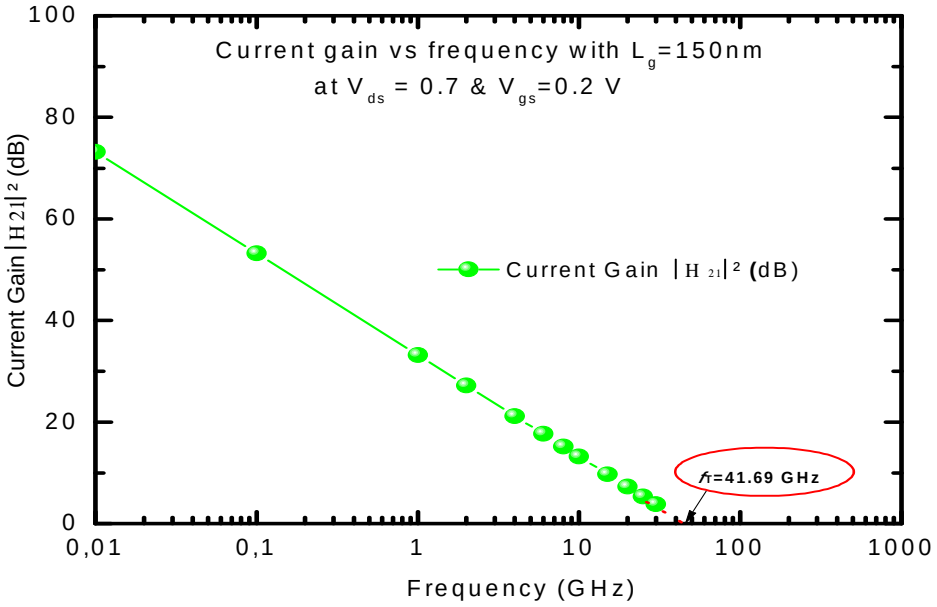

Figure 11:

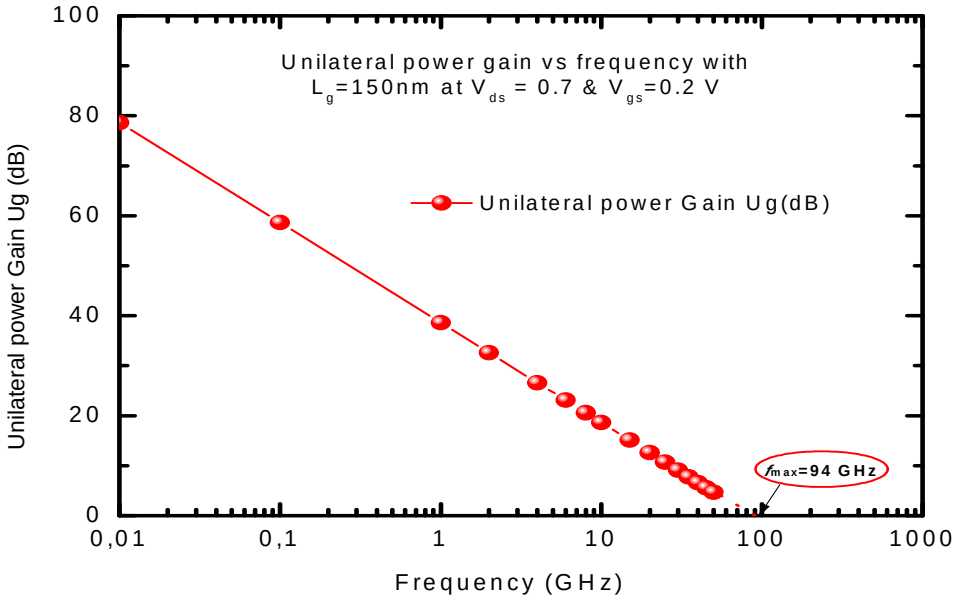

Table 1 **:**

Parameter	**Value**		
	InP	**InAs**	**$In_{0.53}Ga_{0.47}As$**
Affinity (e.V)	4.38	4.9	4.51
Electron Mobility ($cm^2/V.s$)	450	33000	13000
Electron Saturation Velocity ($x10^7$) (cm/s)	0.65	0.8	0.22
Source-Drain Resistance Access ($\Omega.\mu m$)	200		
Effectif Gate Work Function (eV)	3.94		

Table 2:

Intrinsic elements	Notation	Unity	Values
Transconductance	G_m	mS/mm	414
Conductance	G_d	mS/mm	130
Input resistance	R_i	Ohm.mm	0.592
Gate-Drain resistance	R_{gd}	Ohm.mm	1.30
Gate-Source capacitance	C_{gs}	fF/mm	1200
Gate-Drain capacitance	C_{gd}	fF/mm	229
Drain-Source capacitance	C_{ds}	fF/mm	51