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Microcrystalline Silicon Tunnel Junction for Monolithic Tandem Solar Cells using Silicon Heterojunction Technology

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Abstract—In this study, we developed a microcrystalline silicon tunnel junction to be used as a tunnel recombination junction between a large-gap top-cell and a silicon heterojunction bottom-cell, in a monolithic tandem integration. This junction is composed of a p-type layer on the top of an n-type layer, deposited by plasma-enhanced chemical vapor deposition at low temperature (200°C). Microcrystalline phase percentage was controlled with Raman spectroscopy and ellipsometry measurements. The total stack has a thickness of 40 nm and an average conductivity around 10 S/cm. Minority carrier lifetime measurements showed an improvement of the field effect and the passivation with the addition of this junction on top of silicon heterojunction solar cells. Moreover, implementation of microcrystalline layer on top of reference rear emitter silicon heterojunction solar cells improved the fill factor and did not induce parasitic absorption above 700 nm. Simple test structures were fabricated in order to characterize the tunnel junction and optimize it. Then, we carried out dark temperature-dependent I-V measurements on those test structures and observed peaks and valleys, characteristic of the junction tunnel behavior. The developed tunnel junction shows low contact resistivity and activation energies these are promising results for the complete integration on the tandem device.

Index Terms—Microcrystalline Silicon, Silicon Heterojunction, Tandem Solar Cells, Tunnel Recombination Junction

I. INTRODUCTION

Silicon based single-junction solar cells record efficiencies [1] are getting closer to their practical limit highlighted by K. Yoshikawa *et al.* [2]. In this context, tandem and multi-junction solar cells are a great solution to reach more than 30% efficiency. With their high power conversion efficiencies over 25%, silicon heterojunction solar cells (SHJ) are very promising candidates as bottom-cell for monolithic tandem solar cells [1]. In fact, the key of the SHJ technology is the very high open-circuit voltage (V_{oc}) achieved by amorphous silicon passivation, over 740mV [3]. Their fabrication process has demonstrated to be cost effective (e.g. Panasonic, Hevel, Enel Green Power, REC...) and their architecture permits a rear or a front emitter and high bifaciality ratio [4]. Moreover, as a bottom-cell in monolithic tandems, SHJ cells only absorb in the infrared range, so the parasitic absorption in the near UV range of amorphous silicon layers (a-Si:H) do not generate short-circuit current losses. Such tandem solar cells with SHJ bottom-cell demonstrated efficiency of 20% with GaAsP top-

cell [5] and efficiencies up to 29.15% with perovskite based top-cell [6].

To obtain a good monolithic tandem, the junction between the two sub-cells is a key feature. This junction, usually named tunnel recombination junction (TRJ) should be thin, transparent and conductive to allow the charge carriers to recombine. In multijunction solar cells, tunnel junctions interconnect the sub-cells and prevent the formation of parasitic p-n junctions [7]. In the case of monolithic perovskite/silicon tandem solar cells, Mailoa *et al.* [8] first demonstrated the feasibility of this kind of silicon tunnel junction, in 2015, using hydrogenated amorphous silicon partially crystallized by an annealing at 680°C. Then, in 2019, two groups proposed a (n+)poly-Si/(p+)poly-Si tunnel junction for high-temperature passivated contact bottom-cells [9], [10]. In parallel, for the same type of bottom-cells, Nogay *et al.* made a tunnel junction using a silicon carbide layer [11]. With a SHJ bottom cell, tunnel junction layers should not degrade a-Si:H layers' interfaces, which are sensitive to high temperature. In this context, nano- or microcrystalline silicon that could be processed at low-temperature seems to be a good choice. It also presents some advantages comparing to others recombination junctions, as transparent conductive oxides (TCOs), often used in tandem with a perovskite-based top-cell. In fact, nano- or microcrystalline silicon layers are more transparent in the infrared range and have optical indexes more adapted [12]. Moreover, this type of junction already performed well in several multijunction solar cells [13]–[16] and have all the required qualities. For example, Sahli *et al.* demonstrated a perovskite/silicon tandem solar cell with a nanocrystalline silicon tunnel junction at low temperature (<200°C) in both standard and rear emitter configurations [13], [17]. The same kind of junction was also used by Tomasi *et al.* in back-contacted silicon SHJ and performed well [18].

In this work, we choose to develop a tunnel junction in microcrystalline silicon deposited by plasma-enhanced chemical vapor deposition (PECVD) at low temperature (200°C) to preserve the SHJ bottom-cell. Furthermore, the PECVD process of microcrystalline silicon takes place in the same tool than amorphous silicon layers of SHJ cells so the bottom-cell and the TRJ can be produced on the same line.

This study focuses on the characterization and the validation of this tunnel junction, without building an entire tandem. Contrary to the previous presented work, the idea here is not

to show a functional tandem solar cell but to propose a SHJ bottom-cell with a front-side TRJ, adapted for a tandem integration with a large-gap top-cell. In the same way that J. Yang *et al.* did for standard silicon-based solar cells [19] and Luderer *et al.* did for a TOPCon bottom-cell [10]. Therefore, we investigated the tunnel junction in three parties: the characterization of the microcrystalline silicon layers, its implementation on the top of an SHJ solar cell and the validation of a sufficient tunneling behavior and a low resistance junction.

II. MATERIALS AND METHODS

Microcrystalline silicon layers were deposited by plasma-enhanced chemical vapor deposition (PECVD) at 200°C. The deposition power was 1100 Watt and the pressure was 9 Torr. To obtain a 20 nm thickness, deposition times were 110 and 80 seconds, for (n+)μc-Si:H and (p+)μc-Si:H layers, respectively. Moreover, we used a H₂/SiH₄ ratio at 400 and dopants/SiH₄ ratios at 1 and 1.2 for (n+)μc-Si:H and (p+)μc-Si:H, respectively.

Symmetrical test samples and SHJ cells are fabricated with industrial processes on n-type Cz commercial wafers, 180 μm, with a resistivity between 0.5 Ω.cm and 1.5 Ω.cm, M2 size. Wafers are received as-cut and are then cleaned and textured with classical chemical treatments (KOH solution and O₃ based clean), for detailed information see [20], [21].

Amorphous silicon layers and ITO are deposited respectively by PECVD and PVD in Meyer Burger tools. The metallization is done by physical vapor deposition (PVD) for test samples and screen-printing 5 busbars bifacial design for SHJ cells.

Sheet resistance (R_{sheet}) was measured by 4-wire sensing on 20 nm layers deposited on glass. Spectroscopic ellipsometry measurements were performed with a Horiba Jobin Yvon UVISSEL ellipsometer under an incident angle of 70°. Raman spectroscopy was carried out using a 325 nm laser for the layer's surface ($\delta_p \approx 8$ nm) and a 442 nm laser to look more deeply ($\delta_p \approx 50$ nm). Minority carrier lifetime and implied parameters were measured by photoconductance decay on a WCT-120 Sinton instrument using the transient mode, shown results are the average of ten measurements for each sample. Light I-V measurements of total cell area were performed

under AM1.5G standard conditions using solar simulator. Dark I-V were done with probes on circular electrodes under vacuum. External quantum efficiencies were measured with a 150W Xe lamp spectrally filtered.

III. RESULTS AND DISCUSSION

Material characterization

In order to characterize the developed μc-Si:H layers, we performed electrical and optical measurements. We extracted conductivities from sheet resistances (Table I) and they are more than four orders of magnitude higher than doped amorphous silicon used in SHJ cells. To validate the crystallinity of the layers and determine their thickness, we did spectroscopic ellipsometry measurements on glass and on silicon substrates. Measured pseudodielectric functions ($\epsilon = \epsilon_r + i(\epsilon_i)$) and their fitting curves are shown in Fig.1. We used a model assuming a mixture of μc-Si:H, a-Si:H and void and extracted layers' thicknesses (Table I) and percentage of microcrystalline phase (Fig.2). Microcrystalline phase should be controlled not to impact the tandem's V_{oc} [22], [23]. The hump around 4 eV in ϵ_i curve is characteristic of the silicon microcrystallites [24] and confirmed the microcrystalline phase of the developed layers. Moreover, we performed Raman spectroscopy measurements to confirm the percentage of microcrystalline phase obtained by ellipsometry. Raman spectrums were decorrelated in three peaks: 480 cm⁻¹ for the amorphous phase, 520 cm⁻¹ for crystalline silicon and 507 cm⁻¹ for the mix-phase. The microcrystalline phase fraction,

TABLE I
 R_{SHEET} , CONDUCTIVITY AND THICKNESS OF MICROCRYSTALLINE SILICON LAYERS

	Average R_{sheet} (kΩ)	Average Conductivity (S/cm)	Best measured Conductivity (S/cm)	Average Thickness (nm)
(n+) μc-Si:H	25	20	33	21
(p+) μc-Si:H	250	1	2	19
(n+) μc-Si:H/ (p+) μc-Si:H	22	10	13	40

R_{sheet} and conductivity measured by 4-wire sensing. Thickness extracted by spectroscopic ellipsometry.

Fig.2 Percentage of microcrystalline phase extracted by spectroscopic ellipsometry and Raman spectroscopy.

Fig. 1 Plot of the pseudodielectric function (dotted lines) measured by spectroscopic ellipsometry and corresponding fitting curves (lines). A) microcrystalline silicon n-type layer on glass; B) microcrystalline n-p junction on glass ; C) n-type microcrystalline layer on silicon substrate/(i) a-Si:H/(n) a-Si:H ; D) n-p microcrystalline junction on silicon substrate/(i) a-Si:H/(n) a-Si:H. The region characteristic of silicon microcrystallites is circled with dotted line for glass substrates and the characteristic peak is shown in comparison with amorphous peak for silicon substrates.

$X_{\mu c-Si}$, was calculated using the following equation (adapted from [25]) :

$$X_{\mu c-Si} = \frac{I_{520} + I_{507}}{I_{520} + I_{507} + \sigma I_{480}}$$

where σ is the ratio of the integrated Raman cross-section for amorphous to microcrystalline silicon ($\sigma \approx 1$, [25]). I_{520} , I_{507} and I_{480} are the integrated intensities of the previous cited Raman peaks. Fig.2 demonstrate that the percentages of microcrystalline phase extracted by Raman spectroscopy and ellipsometry are consistent. In fact, the small differences observed between the two techniques are mainly explained by the fact that ellipsometry affected the entire layer, no matter its thickness, contrary to Raman spectroscopy. Due to the wavelength of the lasers used for Raman spectroscopy, the results obtained with the 325 nm laser (penetration depth: $\delta p \approx 8$ nm) are more related to the surface of the layers. This also explain why the microcrystalline phase percentage measured by Raman spectroscopy is almost the same for the p-type layer and the n+/p+ stack, because only the front p+ layer is measured. However, for the samples measured with the 442

nm laser ($\delta p \approx 50$ nm), obtained results represent the entire stack. This explains why the microcrystalline phase fraction is a bit lower than with ellipsometry for samples on a-Si:H (structures presented Fig.1 (c) and (d)), because the amorphous layers (between 10 and 15 nm) are included. In fact, in the model used to fit ellipsometric data, the amorphous layers are included in one pure amorphous layer and not in the mixed layer referring to microcrystalline silicon. Table I shows that we achieved a forty nanometers PN junction. Microcrystalline silicon layers have very good conductivities, around 10 S/cm and a controlled microcrystalline phase percentage.

▪ Microcrystalline silicon on the top of SHJ solar cells

Minority carrier lifetime measurements were performed after the PECVD process. Fig. 3 and Table II illustrate the improvement of passivation for symmetric structure (a) (Fig.4) with the addition of the microcrystalline silicon layers (structures (b) and (c)). In fact, the lifetime is more than doubled with the tunnel junction. This improvement is induced by the high level of hydrogen during the deposition, which will

Fig.3 Minority carrier lifetime vs Minority carrier density (Δn) of the studied structures, presented in Fig.4, measured by the Sinton Instruments tools. Symmetric structures are presented on the left sub-figure and rear emitter heterojunction structures on the right sub-figure.

passivate silicon dangling bonds. Moreover, the high conductivity of microcrystalline silicon layers compare to amorphous layers will increase the field effect. For rear emitter heterojunction samples, structure (d), the addition of microcrystalline silicon (structures (e) and (f)) is a bit beneficial and do not degrade the passivation. With the $\mu\text{c-Si:H}$ layers on top of the cells (structure (f)), the gain in iFF cannot be as high as in structure (c) because of the limitation induced by the rear emitter (p-type a-Si:H layer). Furthermore, we observed an implied V_{oc} improvement. As expected by using a PECVD process at low temperature, the deposition of $\mu\text{c-Si:H}$ layers do not degrade SHJ solar cells. Contrariwise, adding the microcrystalline tunnel junction tends to improve them by a better chemical passivation and increased field effect.

TABLE II
MINORITY CARRIER LIFETIME AT $1.0\text{E}+15 \Delta n$ AND CORRESPONDING iFF AND iV_{oc}

Structures	iV_{oc} (mV)	Lifetime at $1.0\text{E}+15 \Delta n$ (μs)	iFF (%)
(a)	/	1790	81.2
(b)	/	3720	83.9
(c)	/	4240	84.4
(d)	732	1630	84.3
(e)	735	1940	84.6
(f)	735	1880	84.5

Measured by the Sinton Instruments tools.

To validate this conclusion, we made two batches of 10 SHJ solar cells, one classical rear-emitter (REF batch) and one with the n-type microcrystalline silicon layer on the top of the

Fig.5 Schema of the solar cells corresponding to the two batches. REF: classical SHJ; MC N: SHJ with (n+) $\mu\text{c-Si:H}$ on the top.

TABLE III
MINORITY CARRIER LIFETIME AT $1.0\text{E}+15 \Delta n$ AND CORRESPONDING iFF AND iV_{oc}

	Average iV_{oc} (mV)	Average Lifetime at $1.0\text{E}+15 \Delta n$ (μs)	Average iFF (%)
REF	733	2600	84.1
MC N	734	2900	84.2

Measured by the Sinton Instruments tools.

amorphous one (MC N batch), Fig.5. The two batches endured exactly the same fabrication and characterization processes, except the microcrystalline silicon layer deposition for the MC N batch. Post-PECVD minority carrier lifetime measurements presented Table III show better implied parameters (iFF and iV_{oc}) and an increased lifetime for the batch MC N. This validates an improvement of the passivation with the addition of the microcrystalline layer ((n+) $\mu\text{c-Si:H}$). Thus, this results in better fill factors, more than 0.5% in average, for the MC N batch (Fig. 6). However, there is a non-negligible but expected

Fig.4 Test samples structures used for minority carrier lifetime measurements and dark I-V study.

Fig. 6 V_{oc} , J_{sc} , filled factors and efficiencies extracted from I-V measurements of total cell area, under AM1.5G standard conditions using solar simulator.

loss in current by the addition of the 20 nm (n+)μc-Si:H layer due to parasitic absorption in the visible range. In order to confirm this hypothesis, we made spectral response measurements (Fig. 7) and observed that the loss occurs between 300 and 700 nm. In this single-junction solar cell case, the current loss of 1.2 mA/cm² induces an average loss in efficiency of 0.5%. This will not be a problem in tandem application because the top-cell will fully absorb in the visible range. Furthermore, there is no significant difference between the two solar cells batches in term of V_{oc} . However, series

resistance are lower in structures with the (n+)μc-Si:H layer. This tends to prove that the contact (n+)μc-Si:H/ITO has a lower contact resistivity than the contact (n)μc-Si:H/ITO, as Nogay *et al.* already observed [26]. This study confirmed that adding microcrystalline silicon layers on the top of SHJ cells do not induce undesirable effect for tandem application.

▪ Tunnel junction behaviour

With the goal to validate the operation of the developed microcrystalline silicon tunnel junction, without building an entire monolithic tandem, we performed dark I-V measurements. We made a frontside circular plot of ITO/Ag deposited by masked PVD and a backside full surface ITO/Ag contact on structures (a), (b) and (c) (Fig.4). With this configuration, we observed the (n+)μc-Si:H/(p+)μc-Si:H tunnel junction as a tunnel diode associated in series with a resistance, forming by the others n-type layers. Fig. 8 shows the I-V curves measured at two temperatures, we observe peaks and valleys, characteristic of a tunnel diode. We noted a plateau region in the decrease from the peak current to the valley current minimum, this plateau is known as an indication of oscillation in the negative resistance region of the curve [27]. Moreover, peak currents are much higher than J_{sc} , which is required for a normal operation of the tunnel junction in multijunction solar cells, according to Yang *et al.* [19]. As expected, dark I-V curves demonstrate the tunnel effect in the developed (n+)μc-Si:H/(p+)μc-Si:H tunnel junction and validate its high recombination efficiency. In parallel, with the method presented by Luderer *et al.* [28], we extracted the

Fig. 7 External quantum efficiency of the best cells of each batch.

contact resistivity of the stack (n)c-Si/(i)a-Si:H/(n)a-Si:H/(n+)μc-Si:H/(p+)μc-Si:H/ITO/Ag (front-side of the structure (c), Fig.4) from ohmic ($R^2 > 0.994$) dark I-V curves, from -100 mV to 100 mV. We obtained values between 0.45 Ω.cm² and 0.55 Ω.cm² at 300K. Temperature-dependent contact resistivity values are in the same range and follow the same trend as the contact resistivity calculated by Nogay *et al.* [26] for the (p+)μc-Si:H/ITO/Ag stack. This demonstrates that the contact resistivity is dominated by the contact with the ITO layer and that the (n+)μc-Si:H/(p+)μc-Si:H junction presents a low contact resistivity. By plotting the contact resistivity in an Arrhenius plot –not shown here– between 250K and 350K we extracted low activations energies, from 75 meV to 150 meV, for both frontside stacks of the structures (b) and (c) (Fig.4). This demonstrates that the tunnel junction behavior is temperature-independent, as expected for a tunnel effect.

Fig. 8 I-V characteristic of structure (c) (Fig.4). Surface of circular front electrodes: 0.13 cm².

IV. CONCLUSIONS

To sum up, we have demonstrated a microcrystalline silicon tunnel junction easily integrated on the top of silicon heterojunction (SHJ) solar cells, for monolithic tandem applications. We controlled the microcrystalline phase percentage in order to maximize its recombination potential and obtained very good conductivities, around 10 S/cm for the entire junction. On top of that, we observed an increase of minority carrier lifetime which shows that the (n+)μc-Si:H/(p+)μc-Si:H layers improve the SHJ solar cells chemical passivation and field effect. Furthermore, those improvements induce a fill factor enhancement. Moreover, the current losses linked to the addition of microcrystalline silicon layers on top of SHJ cell will have no impact in tandem configuration. Finally, with a simple test structure and dark I-V measurements, we completed the tunnel junction characterization and validated its behavior as a low-resistive tunnel recombination junction.

Some supplementary studies are in progress to investigate more deeply the dark I-V measurements and reproduce this method to compare several n+/p+ TRJ for tandem solar cells.

The integration of this SHJ bottom-cell with the (n+)μc-Si:H/(p+)μc-Si:H tunnel junction and a perovskite based top-cell will be presented in future works.

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Anne-Sophie Ozanne received an Engineering degree from Polytech Nantes, specialised in materials and thin films technologies. She has over 20 years of experience on PECVD layers development. She started with an industrial PECVD equipment supplier as process engineer, and then joined the CEA-INES, France, in 2008, as an R&D specialist for PECVD layers development applied to heterojunction cells. Her scope of work goes from lab tool scale to industrial equipment's dedicated to production.

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