RF-DC Multiplier for RF Energy Harvester based on 32nm and TFET technologies

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Abstract—In this work, we are studying the effect of the technology scaling for different full-wave rectifier topologies using the Cross-Coupled Differential Drive (CCDD) strategy to implement a multiplier. For a conventional CCDD scaling from 90nm to 32nm, the PCE and VCE are maintained the same while a large degradation of the dynamic range and sensitivity are observed. This effect could be slightly limited by using a self-body bias CCDD topology. However, the use of TFET enables to avoid this degradation and provide a large VCE and output voltage for input voltage lower than 300mV. To extend this VCE for input voltage > 300mV, we use a CCDD topology increasing the loading drive capability. Interestingly, this resulted not only on increasing the output voltage for large V_{in} but also demonstrated larger PCE than expected for this topology.

Index Terms—TFET, 32nm, Multiplier, full wave rectifier, CCDD, PCE, VCE

I. INTRODUCTION

RECENTLY CMOS industry progresses have enabled the hetero-integration making possible System-on-Chip (SoC) where different technologies like analog, digital, or sensor modules are integrated on the same die. These SoC's fit perfectly into an important electronic market such as Internet-of-Thing (IoT) or more widely the connected object motivated by a new paradigm: Moore than More (MtM) paradigm [1]. However, the scaling of this kind of system is no more dependent on only one technology, but each integrated module in the system. For instance, the digital module will not scale at the same rate than the analog modules or the physical sensors. To make it simpler, the digital module scale easily from 180nm to 90nm node and no doubt for further node. What about the analog ones which are mainly used to conditionate the signal and supply the system of energy?

Among the analog modules, the Radio Frequency Energy Harvesting (RFEH) [2] device is an interesting system since it enables to supply the chip independently from any physically connected source. This one supplies a micropower dc signal from a rectified GHz AC signal, or a RF-DC converter connected to an antenna and matching impedance network [3]. In a previous study, we obtained that basic converter designed with ultra-scaled and 3D technologies like FinFET and TFET could improve the performance of over 32nm planar technology [4]. Additionally, we also found out that the choice

of a well-optimized topology could significantly influence the metric performance [5]. It is important to note that this last study was limited to conventional technology *e.g.* 180nm and 90nm technology nodes and most of the designed circuits were simple rectifiers.

In this present work, we are analyzing the effect of scaling node from planar (32nm) to non-planar technology (TFET) on Full Wave Rectifier Multiplier (FWRM) using based Cross Coupled Drive Differential (CCDD) topologies [6].

This study is divided as follows. First, we describe the different topologies, the 32nm iPDK and the TFET physics-based models for circuit simulations. Then the topologies are optimized using the same method of our previous work [5] and the simulations are carried out using the circuit TCAD simulator Synopsys. Finally, the results are compared with the 90nm technology reference [5] and the metric performance in each case is discussed. We conclude on the effect of the 32nm and TFET technology on the different studied topologies.

II. TECHNOLOGY, TOPOLOGY AND METHOD

The iPDK's used to run the simulations for planar technology include different nodes, namely 90 and 28/32nm. We also consider non-planar TFET technologies for the advanced nodes where the behavior is provided by the look-up table (LUT)[4]. These ones are built based on IV and CV characteristics obtained from a physics-based model applied to the TCAD-Sentaurus simulator. The considered TFET's are nanowire structures of Si(P++)/strained-Si/Si(N++) with 10-nm cross-section for a length of 30nm [6][7]. Note that the leakage current (I_{OFF}) and extrinsic parasitic capacitive component were calibrated according to the process described in [7].

Regarding the circuit topologies, we have considered a 2-stage FWR based on the CCDD technique (Fig. 1) to reduce the threshold voltage (V_{TH}) and hence the circuit power consumption. However, in this case, reverse current (OFF state) overwhelms the charging process resulting in power conversion efficiency (PCE) lower than expected. Dynamic control of the V_{TH} by using the self-body bias (SBB) technique [8] (Fig. 2) is employed to limit this performance reduction. It is worth noting that this topology is only applied to planar technology (90nm and 32nm) since the TFET do not count with body contact. We also consider a CCDD based topology where the input RF

signal has been level shifted (Fig. 3) to afford larger load driving capability [9]. In the following, this latter topology will be called CDB while the conventional CCDD will be called CDA. In all design, CL is the load capacitance and CF and Cr are the fly or pump capacitor. We will use mainly two important Figure-Of-Merit's (FOM). The PCE which measures the output power (P_{out}) w.r.t. the input power (P_{in}), defined by (1):

$$PCE = \frac{\int_{t_0}^{t_0+T} v_{out} i_{out} dt}{\int_{t_0}^{t_0+T} v_{in} i_{in} dt} \quad (1)$$

and the Voltage Conversion Efficiency (VCE), which is the output voltage (V_{out}) w.r.t. the input voltage (V_{in}) as below (2):

$$VCE = \frac{\int_{t_0}^{t_0+T} v_{out} dt}{\int_{t_0}^{t_0+T} v_{in} dt} \quad (2)$$

Note that the ripple factor was negligible since the CL was optimized on purpose. For all tests, the input value is pure sinusoidal signal set at $f = 950\text{MHz}$ varying from 0.1-0.9V, to match with UHD RFID [8] and biomedical application [10].

Fig. 1: Conventional Cross-Coupled Differential Drive called CDA here. This topology is used for 90nm, 32nm and TFET technology.

Fig. 2: Self-Body Bias topology (SBB). Only used with planar technology and more specifically for 32nm technology.

Fig. 3: CCDD topology improving the load driving capability called here CDB. This topology is used for 90nm, 32nm and TFET technology.

III. DESIGN OPTIMIZATION AND SIZING

The procedure to optimize and design the circuits is based on the capacitance and transistor sizing to maximize the PCE in the perspective to yield no power losses [5]. For each considered technology, the topology was optimized by fixing the load to $50\text{k}\Omega$ and the channel length of the transistors. For each topology, we apply also the next constrain: the width of all NMOS transistors must be identical for the same stage; the same for the PMOS transistors. The optimization procedure is

Fig. 4: Optimization of the CDA topology for 32nm and TFET techno. Load is fixed to $50\text{k}\Omega$ and $L_n = L_p = 30\text{nm}$.

Fig. 5: Optimization of the SBB topology for 32nm techno only. Load is fixed to $50\text{k}\Omega$ and $L_n = L_p = 30\text{nm}$.

Fig. 6: Optimization of the CDB topology for 32nm and TFET techno. Load is fixed to $50\text{k}\Omega$ and $L_n = L_p = 30\text{nm}$.

based on the sweep of each capacitor, namely CF then CL, for a given fix width transistor values until we reach

simultaneously the maximum PCE, VCE and the lowest ripple factor. Then, for the obtained capacitance value, the width of the transistor is swept until we reached the maximum VCE on one side and the PCE on the other side. This procedure enables to design symmetrical topologies with good control of the channel resistance. Note that the latter is primordial for the lowest technology node as the 32nm one. The results of this optimization technique are shown in Fig. 3 to 5 where the PCE and VCE are plotted as a function of the N/P-MOSFET widths, for the TFET and 32nm technologies. In the following, we consider only the solutions where the PCE and the VCE are maximized for the circuit sizing. Based on this, the transistors and capacitors sizing of the optimized CDB, SBB and CDB topologies are given in Table I, II and III, respectively. Note that the total width is obtained for each transistor, namely summing all the fingers (fin).

TABLE I
SIZING OF THE 2-STAGE CCDD CIRCUIT (CDA)

Nodes	90nm		32nm		TFET	
Stage	1	2	1	2	1	2
CF[pF]	1	1	10	10	10	20
CL[pF]	1	1	10	10	7	1
RL[kΩ]		50		50		50
Total Wn[μm]	1.2 (1fin)	3 (1fin)	10 (5fin)	10 (5fin)	2.1 (300NW)	2.1 (300NW)
Total Wp[μm]	1.2 (1fin)	3 (1fin)	35 (10fin)	49 (14fin)	2.1 (300NW)	2.1 (300NW)
Ln = Lp [nm]	100		30		30	

TABLE II
SIZING OF THE 2-STAGE SBB CIRCUIT

Nodes	90nm		32nm	
Stage	1	2	1	2
CF[pF]	1	10	10	10
CL[pF]	10	10	10	10
RL[kΩ]		50		50
Total Wn[μm]	0.5(1fin)	0.5(1fin)	12(10fin)	12 (10fin)
Total Wp[μm]	1.9(1fin)	1.9(1fin)	62(20fin)	62(20fin)
Ln = Lp [nm]	100		30	

TABLE III
SIZING OF THE CDB

Nodes	90nm	32nm	TFET
CF[pF]	10	1	10
Cr[pF]	1	1	5
CL[pF]	10	1	10
RL[kΩ]	50	50	50
Total Wn[μm]	0.8(1 fin)	2.6(2fin)	1.82(260fin)
Total Wp[μm]	1.6 (1fin)	20.8(16fin)	2.1(300fin)
Ln = Lp [nm]	100	30	30

IV. RESULTS AND DISCUSSION

The PCE and the VCE extracted from the TCAD simulation of the different circuit topologies implemented with different technologies are shown in Fig. 6 and 7, respectively. Note that the results are benchmarked with the circuit simulation using the 90nm technology reference [5]. The output voltage (V_{out}) is plotted as a function of the input voltage (V_{in}) in Fig. 9 and as a function of the input power (P_{in}) in Fig. 10. The performance parameters and FOM's extracted on the data in Fig. 6-10 are summarized in Table IV.

Fig.7: PCE as a function of the input power for the different design and technology.

Fig.8: PCE as a function of the input power for the different design and technology.

In the case of the conventional CDA for the considered technology the $PCE > 60\%$ is obtained. Though, the scaling from 90nm ($PCE_{peak} = 70\%$) to the 32nm technology produces a 5% lower PCE_{peak} while a slight improvement is obtained with the TFET technology ($PCE_{peak} = 71.5\%$). Note that this PCE peak is obtained at higher P_{in} for the 32nm (+2dBm) and for the TFET (+~1dBm) technology. Interestingly and compared to the 90nm reference, the dynamic range (DR) for $PCE > 60\%$ is twice lower with the 32nm ($DR = 4.8dB$) while it is clearly maintained (10dB) with the TFET technology. The performance degradation caused by the scaling to the 32nm technology is somewhat limited with the SSB topology where a slightly better PCE peak (70%) is obtained at lower P_{in} (-20.14dBm), among others. Regarding the CDB topology, the PCE_{peak} is much lower for the 32nm (25%) but consistent with the 90nm reference (36.1%) [9]. Thus, we can only observe a DR for $PCE > 20\%$ suggesting a significant harvested P_{in} consumption by the rectifier circuit with the CDB topology [3] consistent with the shift of the RF level by the dc from the 1-stage [9]. However, a great improvement is obtained with the TFET where the PCE peak (73%) and the DR (11dB) are in the range of the ones obtained with the CDA topology. The VCE (Fig. 8) reach however the highest maximum with the 32nm technology using the CDA topology where we get 165%, even larger than the reference. This result leads to an output voltage V_{out} of about 0.7V for $V_{in} = 0.4V$ (Fig. 9), namely at the PCE_{peak} , and a 1-V peak sensitivity of -12dBm (Fig. 10). Considering the DR ($PCE > 60\%$), this solution generates a V_{out} of 0.4 to 0.75V providing an output power ranging from 6.4 to 21.7μW. On the other side, TFET technology reaches a lower VCE peak and generates 0.62V output in the same condition but with less sensitivity (Table IV). In this case, considering the DR, the circuit generates an output ranging from 0.32 to 0.85V

providing an output power ranging from 3.3 to 33 μ W. Regarding the CDB topology, the 32nm technology reaches a similar VCE peak than for the CDA one but yielding only an output of 0.45V at the PCE_{peak} consistent with low PCE performance specific for this topology as explained earlier. On the contrary, the TFET technology applied to the CDB topology yields not only the highest VCE but also an output of 0.84V for $V_{in} = 0.4V$ (at PCE_{peak}) with an improved 1-V peak sensitivity of -15.5dBm (Fig. 9-10, Table IV). This solution supplies a V_{out} ranging from 0.65-1.23V with an output ranging from 12.4 to 44 μ W for a PCE>60% DR. As a matter of fact, the CDB topology is greatly improved when using the TFET technology.

The advantages of the TFET are low switching energy from a subthreshold slope below the 60mV/dec planar technology limit along with a V_{TH} in the range of 200mV and an extremely high output impedance [11-13]. Further, the used TFET's are unidirectional producing a reverse current extremely low [6][7]. All of These explain, in the case of the TFET technology, the very good PCE performance with both topologies (Table IV) and the highest V_{out} values for $V_{in} \approx V_{TH}$ and low P_{in} (Fig 9-10). Though, in the triode regime ($V_{in} > V_{TH}$), the TFET yields a low output current and therefore lowest output voltage for $V_{in} > 300mV$ (Fig. 9). However, this is true only for the CDA topology since in the case of the CDB the output voltage is the highest even for high input ($V_{in} > 300mV$).

To conclude, the rectifier circuit needs an active switching device that can work with a low power budget. Scaling MOSFET below 90nm technology node degrades output resistance, yield to too larger V_{TH} not to mention a less steep subthreshold slope. The only way to keep scaling the analog circuit like the FWR will be to switch to 3D technology as the TFET's. However, their specific characteristics come to a price of low output current that can be improved with a specific topology.

Fig. 9: Output voltage as a function of the input voltage.

Fig. 10: Output voltage as a function of the input power.

TABLE VI
PERFORMANCE METRIC RESULTS

Topology	CDA			CDB			SSB
techno	32nm	TFET	90nm	32nm	TFET	90nm	32nm
PCE peak (%)	67	71.5	70	25	73	36.1	70
VCE _{MAX} (%)	165	137	152	162	213	184	166
$V_{out}@PCE_{peak}$ [V]	0.7	0.62	0.57	0.45	0.84	0.67	0.58
$P_{in}@PCE_{peak}$ [dBm]	-18.4	-19.7	-20.42	-18	-16	-16.12	-20.14
DR (>60%)[dB]	4.8	10	9.5	NA	11	NA	5.8
Peak Sensitivity @1V[dBm]	-12	-14	-11.3	-6.7	-15.5	-10	-12

V. CONCLUSION

Conventional and based CCDD topologies have been considered to implement multiplier for RFEH and optimized for the 32nm planar and TFET nonplanar technology. The performance metric (PCE, VCE etc.) was extracted and compared. It results that scaling from 90nm (ref) to 32nm leads to similar performance at the cost of a twice lower dynamic range (PCE>60%). Interestingly, the intrinsic TFET characteristics, *i.e.* low V_{TH} , very good switching, and very high output resistance, enabled to correct this performance reduction for low V_{in} (0.2-0.4V) and relatively low power (-20 to -16dBm). We could improve the VCE with the TFET CDB circuit. We conclude that an analog circuit as a multiplier can be implemented with ultra-scaled technology only if 3D or non-planar technology is used. On the other side, this opens new opportunities since the 3D technology overcome physical limitations of the planar MOSFET such as the subthreshold slope here. We may also think about developing new topology to further optimize the circuit using such novel technology.

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