THz characterization and modeling of SiGe HBTs: review (invited)

Sebastien Fregonese, Marina Deng, Marco Cabbia, Chandan Yadav, Magali de Matos, Thomas Zimmer

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***Abstract*—This paper presents a state-of-art review of on-wafer S-parameter characterization of THz silicon transistors for compact modelling purpose. After, a brief review of calibration/de-embedding techniques, the paper focuses on the on-wafer calibration techniques and especially on the design and dimensions of lines built on advanced silicon technologies. Other information such as the pad geometry, the ground plane and the floorplan of the devices under test are also compared. The influence of RF probe geometry on the coupling with the substrate and adjacent structures is also considered to evaluate the accuracy of the measurement, especially using EM simulation methodology. Finally, the importance of measuring above 110 GHz is demonstrated for SiGe HBT parameter extraction. The validation of the compact model is confirmed thanks to an EM-spice co-simulation that integrates the whole calibration cum de-embedding procedure.**

***Index Terms*—THz characterization, mmW, S-parameters, on-wafer, HBT, BiCMOS, HICUM, compact modelling, de-embedding, TRL calibration.**

I. Introduction

THE recent review of THz silicon-based circuits presented by Wuppertal group [1] evidently shows an unprecedented panel of circuits operating in the lower end of the THz spectrum.

III-V technologies have been leading in the THz field for many years, but these technologies are difficult to use on a large scale for mass applications owing to issues like reliability, scaling, integration etc. In fact, mass applications require economical single-chip solutions that obviate the need for complex microelectronic assembly used to connect the III-V chips to the system. Therefore, Hillger *et al.* [1] pointed out that advanced CMOS and SiGe BiCMOS technologies could "fulfill this role, at least in the lower end of the THz spectrum". The arguments put forward by the authors are as follows [1]: the Si/SiGe technologies concurrently offers economies of scale, smallform-factors, and unprecedented integration capability at the highest industry standards. At the lower end of the THz spectrum, the potential mass applications are microsystems for sensing and active imaging components, but also future 6G wireless systems.

To enable engineers to design such Si-THz circuits, unique expertise and knowledge is required. In the development of complex THz circuits, advanced, precise and readable computer-aided-design (CAD) tools are an essential requirement. At THz range, a desirable feature in the CAD tools is to consist of both accurate electromagnetic EM tools and compact models. Moreover, in setting up these tools, have to be fed with accurate measurements in the THz range. In order to obtain accurate measurement data in THz range, techniques must be developed to verify and analyze the measurements with numerical simulation results. Characterization in the THz range is usually performed by small signal S-parameter measurements.

In this work, we present a review of S-parameter measurement and simulation methods for Si transistors over the last 15 years. Indeed, many research works have been performed on this topic, but only limited reviews of high frequency measurement above 110 GHz have been presented. In this field, Rumiantsev [2] elaborated a detailed review of probe technology; Derrier *et al.* presented a comprehensive analysis of calibration and de-embedding techniques for the on-wafer measurement below 110 GHz in 2012 [3]; Chevalier *et al.* published a review on THz HBT and compact modelling [4]. This paper complements the documents cited above by an analysis of the methodology of on-Silicon wafer measurements above 110 GHz.

After a comprehensive overview of the calibration and de-embedding techniques in part II of this paper, in part-III we focus on the design of test structures for the on-wafer calibration with special consideration of line geometry, ground-plane and floorplan. Part IV describes the importance of the measurement setup, especially the influence of the RF probes. Finally, part V presents a methodology for comparing measurements at very high frequencies, which is essential above 70 GHz for transistor compact modelling.

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II. Calibration and De-embedding Methods

The characterization of transistors requires precise calibration methods. Below 50 GHz, Short-Open-Load-Thru (SOLT) calibration on aluminum oxide substrate, followed by an open-short de-embedding, is an efficient method widely used in industry. Above 50 GHz, more precautions are required, especially with regard to the de-embedding method, and using sophisticated method such as pad-open/transistor-short/transistor-open method leads to more accurate result [3]. For the off-wafer calibration, methods such as LRRM are also used [5].

Above 70 GHz, the characterization of transistors on Si-wafers becomes more challenging [6]. Only very few demonstrations of transistor measurements at higher frequencies have been performed on silicon substrates [5], [7]–[10]. Voinigescu *et al.* [8] have demonstrated measurements up to 325 GHz of an advanced SiGe HBT (hetero-junction bipolar transistor) and have shown results of parameters S_{21} and H_{21} along with the maximum available gain MAG. In [8], the calibration has been carried out with impedance standard substrate (ISS) and the calibration methods used were LRRM (line-reflect-reflect-match) and TRL (Thru, Reflect, Line). In [9], Deng et al. have presented an exhaustive set of S-parameter measurements up to 325 GHz on HBTs from an advanced 55nm BiCMOS technology using calibration approach (LRRM on ISS) similar to [8]. Unfortunately, measurements in [8], [9] were not benchmarked with EM simulation. The report presented by Williams *et al.* in [5] clearly shows the limitations of off-wafer calibration methods by comparing them with the on-wafer TRL method. To compare the off-wafer calibration with the on-wafer TRL [5], the off-wafer calibration need to be followed by additional de-embedding methods such as open-short, pad-short-open or thru, line, short-open etc.

In [5], measurement results from a silicon-on-insulator (SOI) technology were presented where the characteristics of the line were characterized up to 500 GHz, while the transistor measurement was performed up to 110 GHz.

While previous studies were based on experimental demonstration, Fregonese et al. [11] took a different approach, using both experimental data and EM simulation to compare off-wafer SOLT and TRL calibration with on-wafer-calibration. The EM-based approach includes a model for the RF probes and models of the off-wafer and the on-wafer calibration kit and on-wafer devices-under-test (DUT). The study concludes that with increasing frequency the use of the off-wafer calibration methods lead to higher discrepancies in measurement with respect to the expected results. This discrepancy is more correlated to the fact that off-wafer calibration is performed in a different electrostatic environment between measurement and calibration than with the calibration method itself.

To sum-up the most important points:

i) SOLT and LRRM are widely used methods that can be employed from low frequencies up to 50 GHz or more, while TRL calibration at very low frequencies is less convenient due to the line size.

ii) The SOLT and LRRM methods require input parameters to be defined for each probe topology (note that LRRM does not require input parameter for the load). These parameters are often not well described at very high frequencies.

iii) Off-wafer calibration uses a reference plane that is defined at the probe tip in an EM environment which is altered during the measurement phase. This is a major drawback resulting in inaccuracies above 110 GHz.

iv) The on-wafer method has the same EM environment during both the calibration and measurement process.

v) The TRL method is an efficient method for on-wafer calibration and high frequency measurement because it uses a reference plane in an homogeneous medium (middle of a line) and requires only one set of lines with known lengths and a reflect on the wafer. Note that an impedance correction step using an on-wafer load is required.

Hence, recent studies agree that on-wafer TRL is the most accurate calibration method for high frequency measurement (>70 GHz), but this requires engineering efforts to develop an accurate on-wafer design kit. This calibration must be followed by an impedance correction procedure that can be tricky.

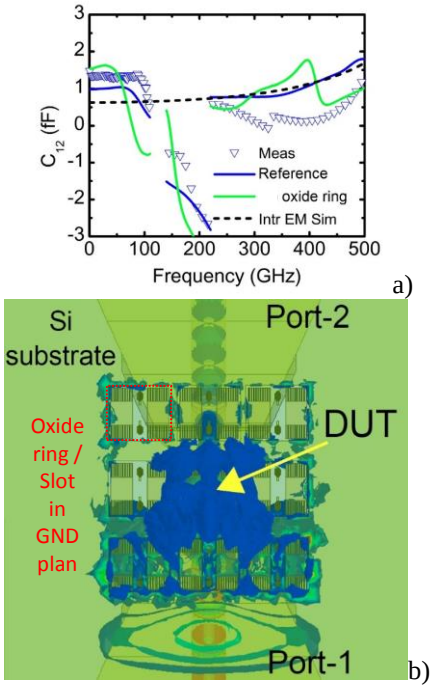

Fig. 1. Port 1 to port 2 capacitance with and without SiO_2 ring (a) and HFSS-simulated electric field contour (back view) for DUT transistor-open at 500 GHz with aligned neighbors and oxide ring (b).

III. Design of Test Structures

The validity of the TRL procedure and its accuracy is strongly dependent on the choice of the line topology, i. e. microstrip line (MLIN) or coplanar waveguide (CPW)), and on its geometry. Other than line, two other important aspects in on-wafer calibration kit design are the design of RF pad and the ground plane.

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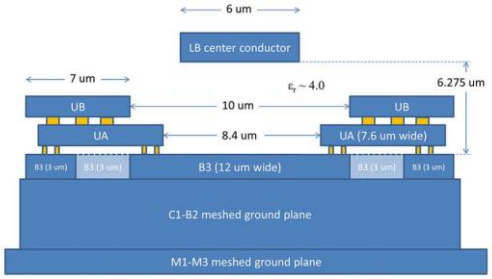
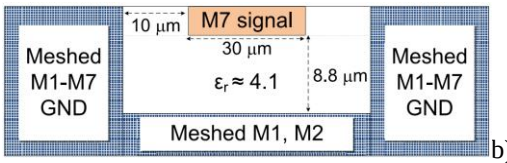
A. *Ground Plane:*

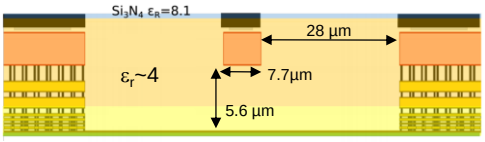
Williams et al. [12] recommend to use a continuous ground plane: "We further suppressed multimode propagation by using a continuous ground plane under the entire calibration kit to eliminate the possibility of slot modes between the grounds of adjacent calibration structures and other resonances." This point was the weakness of the layout presented in [13] and that was clearly identified using EM simulation. The impact of a non-continuous ground plane is shown in the Fig. 1. From Fig. 1a, the effect of the oxide ring is visible. The addition of the oxide ring disturbs the trends of the port capacitances generating a strong ripple on C_{12}, to a lesser extent on C_{11} and C_{22}. This is due to the fact that, when the dielectric ring is present (Fig. 1b), the E-field is heavily affected. The intensity of the field increases around the DUT and below the excitation probe and we can plainly see the field densifying around every adjacent structure. This reinforces our motivation in the use of the boundless ground plane.



a) from [14]



b) from [15]



c) This work

Fig. 2. Cross-sectional view of different lines used in on-wafer calibration kit: a) line fabricated in 45nm CMOS SOI process[14], b) CPWG line fabricated in a IHP Bipolar process[15], c) microstrip line fabricated in BiCMOS 55nm STMicroelectronics process. (copyright to be done)

B. *Conventional Lines:*

The design of lines for TRL calibration is still a non-standardized procedure as very different geometries are presented in the literature [10], [14], [15], while the corresponding frequency band and the technology are quite similar with respect to the back-end of the line (BEOL). An overview of different topologies is given in the table I and cross-sections of some lines are shown in Fig. 2. While [5], [14] uses a line comparable to a CPWG structure due to design rule constraints in a SOI CMOS technology, [15] uses CPWG lines with a larger width to minimize the losses within a BiCMOS technology. However, in [12], the authors explain that "the small cross section of the microstrip transmission lines helps to reduce radiation and multiple modes of propagation". In [12], the authors use a microstrip line of 22µm width on a BCB dielectric with very low dielectric losses, a process developed for THz application on III-V technologies.

In our approach a MLIN with a width of about 7 µm fabricated in a BiCMOS technology is used. This line represents a good trade-off between reduced losses and single mode propagation. Indeed, this line allows the suppression of high order modes at least up to 500 GHz as demonstrated in Fig. 3.

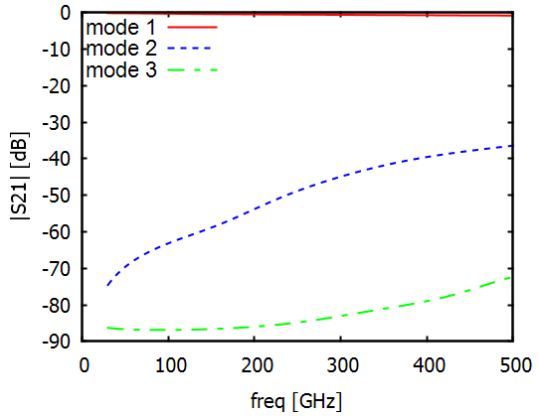


Fig. 3. Simulation of the first 3 modes of the micro-strip line from Fig. 2c (without pad) highlighting that only the first mode is propagated within the line (Length=583µm).

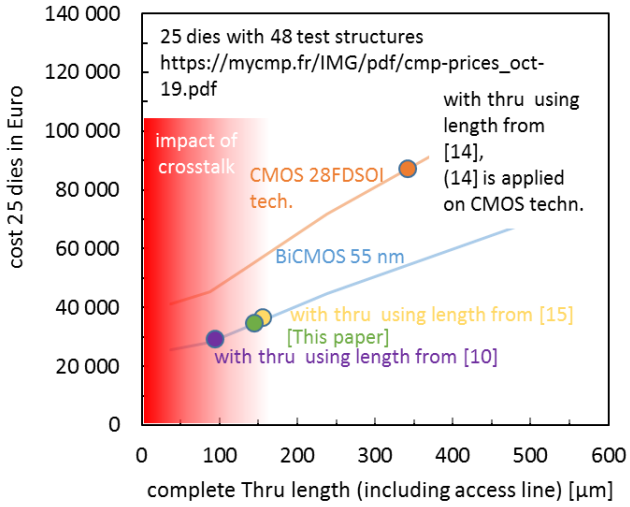


Fig. 4. Scenario of estimation of costs versus complete thru length based on the floorplan and on the cost of two advanced STMicroelectronics technologies the 28nm FDSOI CMOS technology and the BiCMOS 55nm technology. The figures highlight the importance in term of cost of the choice of the thru length and access.

A second important issue in the design of calibration kits is the length of the thru and the distance from pad to pad. The TRL calibration method is in fact an 8-term algorithm that does not correct for crosstalk. If this can be partially corrected by de-embedding, the easiest option to minimize the crosstalk influence is to increase the length between pads together with a reduction of parasitic propagation modes. Williams *et al.* uses upto 400µm in [12] together with microstrip line topology.

Also, Williams *et al.* [16] have proposed crosstalk correction using a 16-term error calibration model, but this is not widely

used because of its complexity in terms of need of various test structures and its implementation. Nevertheless a crosstalk correction is possible with a simplified approach described in [12] in which the authors mentioned that "having only three such standards, we employed the crosstalk corrections described in [16] and implemented in [17] under the additional assumption of symmetric probes and access lines". The same authors give also the following recommendation to limit probe to probe coupling in the case of the use of CPW lines but that from our point of view can be extended to the MLIN case: minimize probe pitch; keep the distance between crosstalk standards close to the device size.

If length extension is a simple option, this procedure is therefore costly, especially for advanced silicon technologies. Therefore, a tradeoff between cost and accuracies need to be found. To illustrate these remarks, we have calculated the cost of 25 dies with 48 test structures. The 48 is a usual number of test structures necessary for compact modelling purpose. The area required depends on the length of the thru (see Fig. 4). The study is done using two advanced technologies from STMicroelectronics, the 28nm FDSOI and the BiCMOS 55nm technologies. In the same figure, we have indicated the length of the thru chosen in the different on-wafer calibration kits from [14], [15] assuming that we have made a similar choice than these groups to choose the length of the thru. This Fig. 4 undoubtedly demonstrates the enormous cost difference that can be made with this choice: on the one hand a very expensive test structure, on the other hand potentially erroneous measurements.

	Comments	**Line topology**	**Thru length / Inter-probe distance [µm]**	**Line width / dielectric height / horizontal distance to GND [µm]**	**Pad size : length x width [µm²]**	**Distance between two adjacent structures– vector [x,y], [2]**	**Comments**
Williams2013 [12] NIST	InP / BCB Meas up to 1 THz	MLIN	400µm / NAN	22 / 8 µm	44 x 22	150µm	BCB dielectric is used up to 750 GHz (no high order modes) Gold pad (IIIV techno.)
Williams2014 [5][14]NIST	Silicon MOSFET Meas up to 110 GHz	CPWG (metal density constraint in PDK)	300µm / ~350 µm	6 / 6.275 / (see Fig. 2a) µm	40 x 30	undisclosed	Constraints in line design due to PDK Z_C =75 ohm corrected with off wafer load Gold platting of pads
Galatro[15] TU DELFT	Silicon BiCMOS Up to 325 GHz IHP	CPWG	100 µm / 150 µm	30 / 8.8 / 10 µm	50x30	undisclosed	
Galatro[7] TU DELFT	Silicon BiCMOS Up to 325 GHz	CPWG Inverted-CPW	100 µm / 150 µm	30/8/15 µm 5/1.07/10 µm	50x30	[160, 0] µm (structure are in line)	CPW and Innovative line topology
Fregonese IFX [10], [11] U. Bordeaux	BiCMOS Up to 500 GHz Infineon	MLIN	50 µm / 90 µm	4.9 / 3.9 /28 µm	38x38	[24, 0] µm (structure are in line)	Too dense floorplan => coupling to adjacent structure – Probable crosstalk
Yadav Brava U. Bordeaux [18]	BiCMOS Up to 500 GHz STMicro	MLIN	36.8 / 91 µm	5.74 / 5.8 / 12.5µm	43x27	[123, 0] µm (structure are in line)	Slot in GND plane generates inaccurate results-coupling to adjacent structure is not significant – Probable crosstalk
This work U. Bordeaux	BiCMOS Up to 500 GHz STMicro	MLIN	65µm / 140 µm	7.7 / 5.6 / 28µm	40x25	[207, 133] µm (structure are staggered)	Probable non-negligible crosstalk above 400 GHz

*Table I: review of calibration lines realized for the on-wafer calibration structures to use with TRL method, * Inter-probe distance is taken from the middle of the pad port 1 to the middle of the pad port 2.[2] Distance is taken from pad (external part) structure 1 to pad structure 2 and is defined thanks to a vector.*

C. Innovative approach for calibration lines:

If the on-wafer TRL approach has many advantages and is an accurate method, there are still some measurement difficulties: The on-wafer TRL calibration demonstrated in [10], [14], [15] brings the reference level to the top metal while the transistor itself is at the M1/contact interface. Hence, calibration is

usually followed by a de-embedding procedure that requires the measurement of several other test structures. The addition of matrix manipulation together with supplementary measurement amplifies the measurement error, complicates and degrades the overall measurement quality of the transistor especially when probe contact difficulties come into play.

To circumvent or reduce this problem, Galatro *et al.* [7] have proposed the design of low loss lines at the M1 level to define the reference plane exactly at the transistor level. The proposed calibration/de-embedding kit contains capacitively loaded inverted CPW lines, allowing to reduce the losses generated by the conductive (i.e., silicon) substrate, by confining the propagating field in the low-loss dielectric layers (see Fig. 5). The structures were specifically designed for (sub-) mm-wave measurements as a supplement to conventional de-embedding kits used at lower frequencies. The results using this calibration/de-embedding kit, realized in a 130-nm BiCMOS technology, were experimentally obtained in the WR-03 waveguide band.

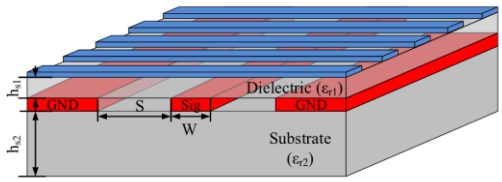


Fig. 5. Simplified sketch of a CL-ICPW section. The transmission line consists of a CPW realized on the lossy substrate, which is characterized by a dielectric constant ε_{r2} and is capacitively loaded by means of floating bars separated by a dielectric layer, with dielectric constant ε_{r1}. Extracted from [7] (copyright to be done)

In the same sense, but with a simpler approach, we attempt to set the reference plane very close to the transistor with a microstrip line at M3 level (0.5µm above M1), while its ground plane is at M1 level. Unfortunately, the small thickness of the M3 line greatly increases the resistive losses and reduces the calibration accuracy.

A second difficulty of the TRL, which is addressed in part V, is the accuracy of the horizontal probe positioning. In fact, the TRL calibration requires the measurement of different line lengths, which forces a horizontal probe displacement that can induce probe error positioning. Moreover, in case of an industrial environment with automatic probe station, manual intervention is required at this stage or it can be replaced by an expensive additional horizontal motorized support installed on the probe holder. To overcome this difficulty, we propose to create a structure based on a repeating pattern to generate lines of different lengths having a scalable behavior with the number of patterns [19], [20] (see Fig. 6).

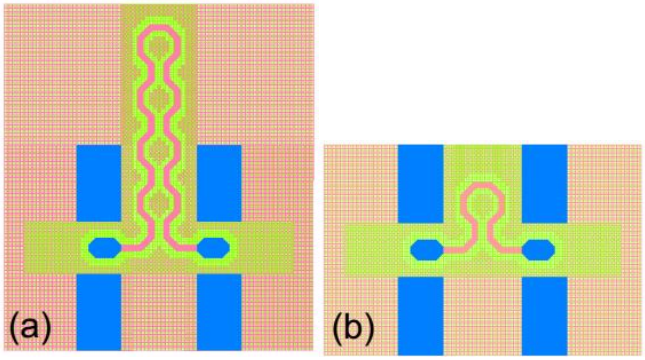


Fig. 6. 2D schematic of the meander line used for the on-wafer TRL calibration for the frequency range from 20 to 400 GHz[19][20].

D. Floorplan:

When building the calibration kit, the positioning of the individual test structures on the chip (floorplan) should not be neglected. Williams et 2013 mention: “These three standards were placed 150 µm apart to reduce the direct coupling between the calibration standards, and allow the crosstalk between the probes and the access lines to be characterized and at least partially removed from the measurements, as explained in [7]”. Also Schmückle *et al.* [21] have evidently underlined the influence of the neighboring structure on the measurement accuracy. To prove this, identical thrus were positioned on a GaAs substrate with different neighbors and different distances. The measurement results evidently demonstrate the influence of the neighbors and the same is confirmed by the EM simulation. Fig. 7 from [21] illustrates the electric field distribution of two similar structures at two different positions on the wafer. Two conclusions can be drawn from this:

i) “the fields are not at all confined to the intended structure but show significant spatial extension involving the neighboring line elements”; ii) “the intensity of the stray fields increases with frequency and that more and more elements are involved in the resulting behavior”.

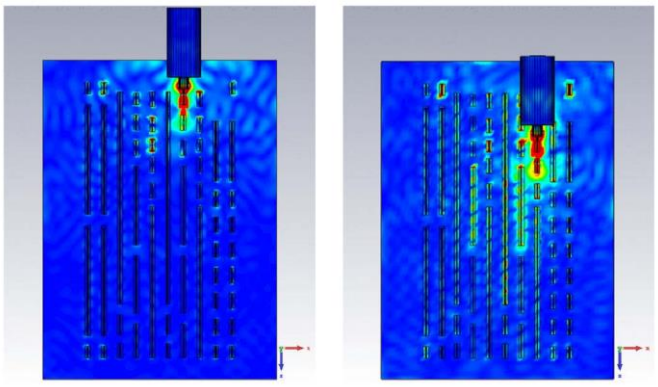


Fig. 7. Magnitude of the electric field of two identical thru at two positions simulated at 85 GHz extracted from [21], (copyright to be done)

While Schmückle’s study [21] highlights an unexpected deviation in the measurement of the magnitude of S_{21} of a line of about 0.3 dB at 70 GHz on a GaAs substrate, we observed an even higher unexpected deviation in the order of about 1 dB on a line at 450 GHz on a BiCMOS technology. Our observation is consistent with the second point of their analysis, which states that the stray fields increase with frequency. To ensure that this

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behavior was correlated with neighboring structures, we further investigated this effect through EM-simulation. The EM simulation is performed by reproducing the measurement environment and placing the calibration structures with and without neighbors and including probes. The application of the TRL calibration in both cases, measurement and EM-simulation, plainly reveals the influence of the neighbors with the occurrence of a "oscillating" trend with increasing frequency [10] (see Fig. 8).

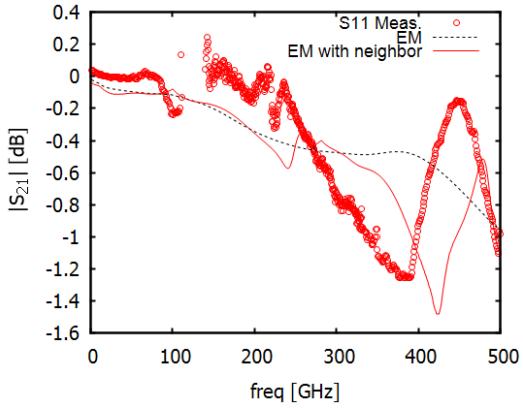

Fig. 8. S_{21} parameter measurements of a line up to 500 GHz showing unexpected behavior: impact of adjacent structures confirmed with EM simulation

This effect is enhanced when a very dense floorplan is designed. Measurements shown in Fig. 8 are from our first mmW on-wafer calibration kit, where the test-structures were placed very close together. The neighborhood effect does not occur in the new version of the calibration kit where the distance between structures is increased and the structures are staggered (see Fig. 9).

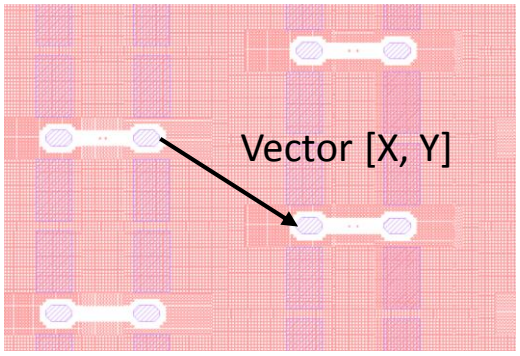

Fig. 9. Typical floorplan using staggered structure[X,Y]=[207,133] µm

IV. MODELS OF PROBES IN THE WHOLE FREQUENCY BAND

The design of the mmW calibration kit should not be done without considering the probe used. Of course, the pitch needs to be considered, but other factors such as the probe-to-substrate and probe-to-neighbors coupling or probe-to-probe coupling are generally correlated to the probe topology and geometry. A complete description of probe topology and technology is given in [2].

Andrei *et al.* [22] have highlighted the probe-to-substrate coupling by measuring the same device with and without dicing the die at the pad periphery. Their conclusion obviously discloses that the Cascade's Infinity probes used in the study are affected by the probe-to-substrate coupling despite the microstrip line technology that provides a ground plane between the probe and the wafer.

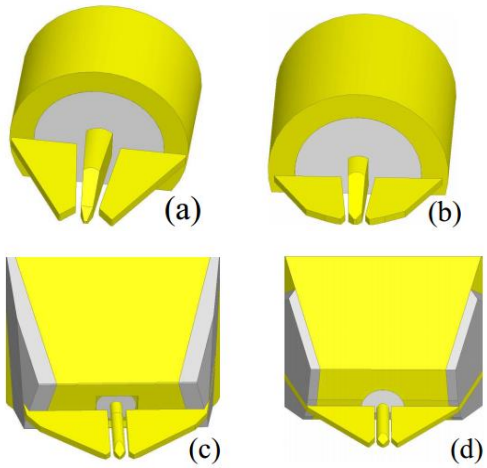

Fig. 10. EM probe models based on Picoprobe GGB (a) 1 GHz -110 GHz, (b) WR5, (c) WR3 and d) WR2.2. In all models, white=coaxial insulator, gray=solder, yellow=metal.

In previous work [10], [11], we have elaborated a methodology for building virtual measurements by introducing the probe into the EM environment and reproducing the complete calibration and de-embedding procedure. A similar approach was published in parallel in [23], [24] applied to III-V technologies. In addition, this study is applied to the circuit scale and also covers a large part of the measurement environment with DC probe needle and bond wire (see Fig. 11).

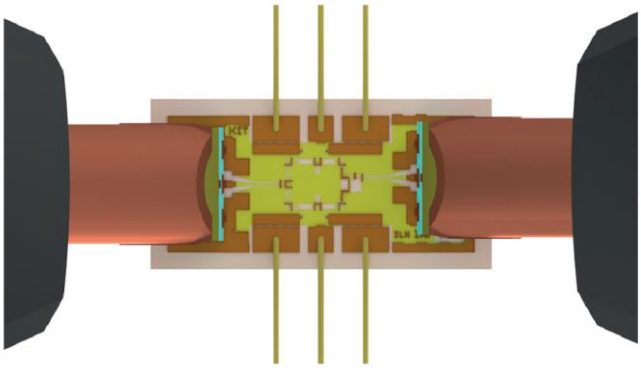

Fig. 11. Simulation scenario including RF probes (Infinity Cascade), DC probe, bond-wire and III-V circuit of a digital phase shifter working from 220 to 325 GHz. Extracted from [23], see also [24]

Later it is proposed [25] to study the side effect induced by "the probe construction together with neighboring elements, for the most common planar transmission lines, coplanar waveguides, and thin-film microstrip lines".

To complete this study, [26] developed some accurate EM models of each Picoprobe GGB probe used for measurements from DC to 110 GHz and in the WR5.1, WR3.4 and WR2.2 bands. These models are based on a detailed analysis with microscopic imaging of the probes at various angles. The analysis of the pictures of these four probes undoubtedly revealed that the geometry of the probes was really different and consequently the way the probes confined the EM field towards the pads was also different. The Fig. 12 draw attention

about the distribution of the electric field of the WR5.1 probe and the WR3.4 probe for the same test structure in the simulation at 220GHz. This figure unmistakably emphasizes the behavior of the probe, which differs dramatically in terms of coupling.

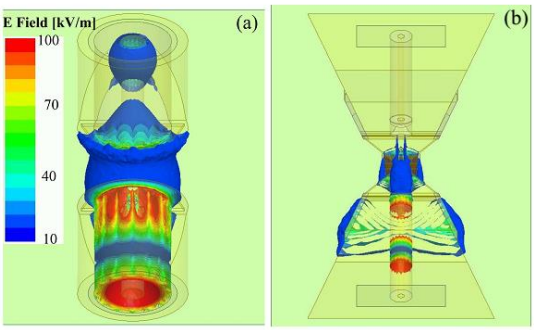

Fig. 12. Simulation of Electric Field highlighting stray field on a transistor open at 220 GHz using two Picoprobe from GGB at the edge of their frequency band: a) WR5.1: 140-220 GHz, b WR3.4: 220-325 GHz

In addition, when measuring the C_{12} capacitance of a transistor open, we noticed specific signatures and discontinuities that correspond to probe's own frequency band. This was noticed in three generations of on-wafer calibrations kits with different pads, different BEOL and different floorplans[10], [13], [20]. One of this typical signatures is the occurrence of a sudden decrease of the C_{12} capacitance calculated from (-imag(Y_{12}/ω)) from 70 GHz and up to 220 GHz, as described in Fig. 13. Thanks to the EM simulation including the probe and the application of the complete TRL calibration procedure with EM data, it is possible to reproduce this unexpected behavior, as shown in Fig. 13. In the same way, this effect can be completely suppressed by changing the probe geometry used below 220 GHz by using the front-end geometry of the WR3.4 or WR2.2 probe. Therefore, the two calibration kits developed in [10], [18] and the one from this paper are obviously incompatible with the 220 GHz Picoprobe from GGB probe, and the calibration kits deserve to be redesigned taking into account the geometry of this probe. Another solution would be to use better designed probes.

Only limited effort has been made in this direction, with the exception of the University of Virginia, which together with Dominion has proposed new probe architectures based on silicon MEMS technology and designed for measurements up to 1.1 THz [27]–[30].

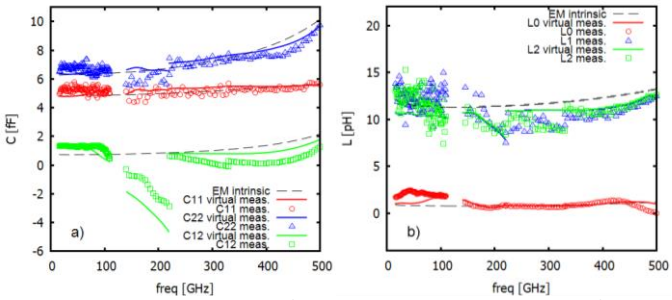

Fig. 13. (a) Capacitances of the transistor-open; b) Inductors of the transistor-short. In both the panel, measurement (symbols), virtual measurement (EM with probe and calibration represented by solid line) and EM intrinsic simulation (dashed line) are shown up to 500 GHz using an on-wafer TRL calibration kit (thru of 65µm) fabricated using B55 technology- STMicroelectronics.

V. CONTROL OF EXPERIMENTAL PARAMETERS

Previous studies have confirmed that probes can be the source of discontinuities from band-to-band. But also the control of experimental setup parameters is of great importance to avoid discontinuities and to obtain realistic measurement results.

Therefore, an important task for these settings is to control the power over a wide frequency range, especially for SiGe HBTs, which can become nonlinear even at a power level of -30 dBm. An exhaustive and well-controlled procedure has been proposed in [31].

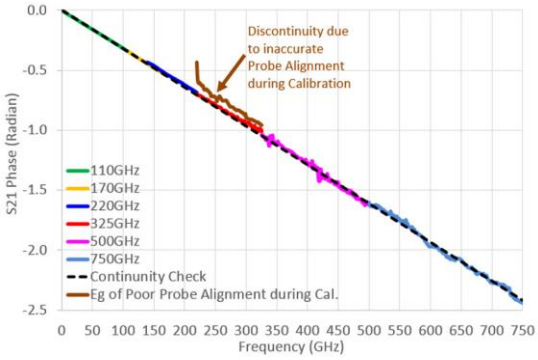

Fig. 14. Phase versus frequency (-0.185 Deg/GHz) for the 0.5ps Line extracted from [32].

Another challenge is the control of DC contacts for each frequency band, which can lead to problems especially on aluminum pads. Of course the probes have to be purchased according to the material of the pads. Another possibility proposed in [14] is to add gold plating on aluminum pads to obtain reliable contacts. In [32], a method is proposed to monitor the DC contact by adding a DC sense probe. In case of DC contact problems, it is sometimes necessary to move the probe to clean the tips or simply make another contact. Unfortunately, moving the probe can cause inaccuracies in the RF calibration. This was investigated in [32][10] and [33]. The authors from [32] recommend to plot the inductance and the phase (see Fig. 14) of a verification line to assess the accuracy of the calibration. The Fig. 14 shows an example of inaccurate probe alignment during ISS calibration resulting in inaccurate measurement. In the same sense, we proceed to a voluntary inaccurate probe position on the line of our on-wafer calibration kit. This positioning error was measured exactly by optical interferometry (see Fig. 15). This probe position error of about 15µm on the pad leads to an inaccuracy of about 0.4 fF when measuring a transistor open in the WR2.2 band and of about 3° when measuring the phase on a line at 500 GHz. These results were confirmed by the EM simulation.

VI. TRANSISTOR CHARACTERIZATION AND MODELLING

Above 110 GHz, only a few modelling demonstrations have been carried out so far [7], [8]. For example, Galatro *et al.* [7] show a comparison of the HICUM model [34], [35] with measurements. Despite precautions regarding the measurement procedure, i. e. calibration and de-embedding, a certain discrepancy between the two data appears which is in the order of about 5dB and about 30-40 ° on the phase of S_{12}. Other parameters show a fairly good agreement considering the

frequency range. Unfortunately, the model does not cover the entire frequency range. In [4], the model is shown on the whole frequency range and many bias points up to 325 GHz.

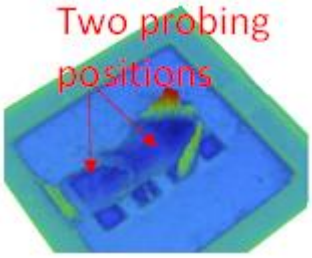

Fig. 15. 3D imaging of the signal pad used in the WR-2 band. Images are taken by optical interferometry. Images show two probe contacts at different positions on the pad where Pad size is38x38µm².

Knowing that most of the transistor parameters are extracted with DC measurement and S-parameter measurement below 40 GHz, even for a technology with a f_T/f_{MAX} above 300 GHz, the accuracy of the model above 110 GHz is unfortunately not guaranteed.

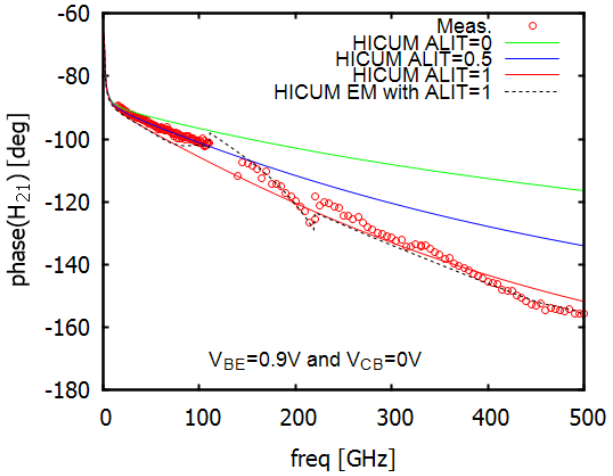

Fig. 16. Phase of H_{21} parameters for peak f_T operating points, Measurement (symbols), virtual measurement (EM-HICUM with probe with calibration-de-embedding shown in dashed line) and HICUM simulation for different set of parameters ALIT (solid line). Data is calibrated using an on-wafer calibration followed bya de-embedding technique. The calibration kit structures and DUT are fabricated usingB55 technology- STMicroelectronics.

Some parameters still cannot be extracted at low frequency, such as the NQS parameters of the HICUM model: for example, the phase of the H_{21} is very sensitive to the ALIT parameter, which models the delay between the intrinsic base-emitter voltage and the voltage controlled current source. Imagine the following modeling scenario: -i) measurement results are available up to 40 GHz, only. In this case, setting the ALIT parameter equal to zero gives a sufficient accuracy; -ii) measurement results are available up to 110 GHz; now, ALIT=0.5 gives the best fit in this frequency range, while ALIT=1 is too large and overestimates the phase of H_{21}. -iii) Measuring at higher frequencies gives a better result, but stopping the measurement at 220 GHz without EM simulation will cause difficulties for compact modelling. First, the measurement shows an unexpected trend compared to the HICUM model. A first guess would lead us to change the parameters to match this unexpected trend or even to modify the HICUM equation. Therefore, the method proposed in [36], which reproduces a virtual measurement by EM modelling including probes and calibration/de-embedding test structures associated with the compact model is a very efficient method to verify the fit of the compact model and the measurements. This is shown in the Fig. 16, where this method is able to reproduce unexpected trends and discontinuities. Finally, we can conclude that very high frequency measurements are mandatory for precise compact model parameter extraction, but cannot be used without a detailed control of the measurements thanks to the above described advanced modelling method.

If the ALIT parameter is an example, other parameters in the HICUM model such as ALQF, which models the vertical NQS effect on the diffusion charge, or the fcrbi parameter, which is required for lateral NQS modelling or substrate related parameters [37], require measurements above 110 GHz.

After adjusting all NQS parameters, the HICUM model, on which we have grafted a substrate model [37],gives quite good results, as shown in Fig. 17.

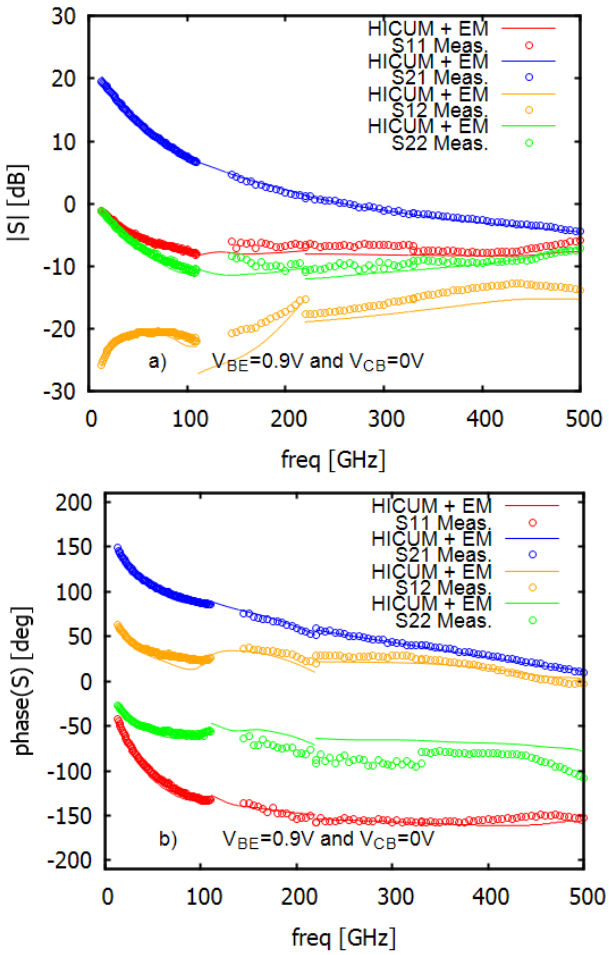

Fig. 17. Magnitude and phase of the S-parametersof a SiGe HBT for V_{BE}=0.9 V V_{CB}=0V.In the figures, measurement result is shown by symbols, , EM-HICUM with probe with calibration-de-embedding are shown by solid lines. Both actual measurement and virtual measurement data are calibrated using an on-wafer calibration followed by a de-embedding technique where structures are fabricated usingB55 technology- STMicroelectronics.

VII. Conclusion

On-wafer characterization of silicon THz transistor is a new challenge that have some peculiarities compared to III-V THz transistors. If the research community in these two fields agree to use on-wafer calibration followed by de-embedding, the implementation of the calibration kit will differ mainly due to the BEOL, which is very different for advanced silicon technologies compared to III-V technologies. On the one hand; III-V technologies have gold plated pads that eliminate many uncertainties associated with the probe contact. On the other hand, their less complex BEOL requires the use of CPW lines, which must be carefully designed to avoid high order modes. Williams *et al.* [12] use a modified BEOL with BCB, which is not common in III-V technologies. In silicon technologies, the complex BEOL technology with 7 or more metallization layers allows the design of optimized microstrip lines, but the troubles are caused by the probe contact on aluminum pads. Despite the great lead of the III-V community on THz transistor, most transistor measurements are performed below 110 GHz [38]–[40].

We believe that the gap between silicon and III-V technology for THz application will be greatly reduced thanks to the versatility of silicon technology and to the massive efforts of the community on the various topics such as the technology process, the characterization and the modelling and the circuit design. Hence, in this review, we aimed to give a feedback on the experience of the research community in characterizing silicon technologies in the THz domain, especially with respect to the design of the calibration kit, the influence of measurement environment, the influence of the probe and the evaluation of the measurement accuracy. A correct design of the lines, the ground plane, the floorplan and a systematic EM simulation procedure including the probes for the measurement analysis are the key points for the THz measurement and transistor modelling.

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