Electrical and electrothermal 2D simulations of a 4H-SiC high voltage current limiting device for serial protection applications

F. Nallet, A. Senes, Dominique Planson, Marie-Laure Locatelli, J.P. Chante, D. Renault

► To cite this version:

F. Nallet, A. Senes, Dominique Planson, Marie-Laure Locatelli, J.P. Chante, et al.. Electrical and electrothermal 2D simulations of a 4H-SiC high voltage current limiting device for serial protection applications. 12th International Symposium on Power Semiconductor Devices & ICs. Proceedings, May 2000, Toulouse, France. pp.287-290, 10.1109/ISPSD.2000.856827 . hal-02972084

HAL Id: hal-02972084

<https://hal.science/hal-02972084>

Submitted on 20 Oct 2020

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

Electrical and Electrothermal 2D Simulations of a 4H-SiC High Voltage Current Limiting Device for Serial Protection Applications

F. Nallet, A. Sénès*, D. Planson, M.L. Locatelli, J.P. Chante, and D. Renault

Centre de Génie Electrique de Lyon (CEGELY) UMR 5005 – INSA de LYON, bât. 401
20, av. A. Einstein – 69621 VILLEURBANNE Cedex Tel: (33) 04 72 43 82 38
E-mail: nallet@cegely.insa-lyon.fr

*Schneider Electric S.A. Direction Scientifique et technique 33, bis, av. Maréchal Joffre – 92002 Nanterre Cedex

Abstract— This work presents a novel field for solid state power devices : a 4H-SiC specific device is examined as a current limiting device for serial protection application. The device structure is a vertical power MOSFET like with a existing N channel. Its performances is simulated with ISE TCAD tools. A study of its electrothermal behavior is presented, demonstrating the SiC superiority over silicon with regards to this field.

Index terms-- SiC, current limiting device, serial protection, temperature, simulation.

I. INTRODUCTION

Silicon carbide is well adapted for the power electronic needs. Already, many prototypes have been built and most of them show interesting abilities. It would be possible to translate in SiC technology most of the commercial silicon device and, therefore, to push away the limits of the semiconductor power device. The silicon carbide properties ($E_g \approx 3$ eV, $E_c \approx 2$ MV.cm⁻¹, $\lambda_{300K} \approx 4.5$ W.K⁻¹.cm⁻¹) allow to study specific device design for new application fields. This paper presents a silicon carbide high voltage current limiting device for 20 A/(300V to 600V) applications. Typically, this kind of device has to work under high temperature conditions without failure. A simulation study of the static I-V characteristics is proposed. Electrothermal simulations have been performed to take into account self-heating during a current surge wave. The parameters of the models used for the simulations [1] are:

Electron mobility model:

$\mu_{\text{dop}} = \mu_{\text{min1e}} \frac{\mu_{\text{min2}} \left(\frac{T}{300} \right)^{-\alpha}}{1 + \left(\frac{T}{T_0} \right)^{\beta}} + \frac{\mu_{\text{min2}} \left(\frac{T}{300} \right)^{-\alpha}}{1 + \left(\frac{T}{T_0} \right)^{\beta}}$	Parameter	4H-SiC
---	-----------	--------

	μ_{min1} [cm ² /V.s]	20
	μ_{min2} [cm ² /V.s]	0
	μ_L [cm ² /V.s]	700
	ξ	3
	μ_1 [cm ² /V.s]	0
	C_r [cm ⁻³]	4.5×10^{17}
	α	0.45
	C_s [cm ⁻³]	3.43×10^{20}
	β	2
	P_c [cm ⁻³]	0
$\mu(E) = \frac{\mu_{\text{low}}}{\sqrt{1 + \left(\frac{\mu_{\text{low}} E}{V_{\text{sat}}} \right)^2}}$	$V_{\text{sat}} = V_{\text{sat},0} \left(\frac{T}{T_0} \right)^{-V_{\text{sat},\alpha}}$	Parameter 4H-SiC
	v_{sat} [cm/s]	2×10^7
	$v_{\text{sat},\text{exp}}$	0.5

Impact ionization model:

$a = g_a \exp\left(\frac{-\phi}{E}\right)$ <p>with</p> $g = \frac{\tanh\left(\frac{\hbar W}{600k}\right)}{\tanh\left(\frac{\hbar W}{2kT}\right)}$	Parameter	4H-SiC
	$a_{n,p}$	3.09×10^6 cm ⁻¹
	$b_{n,p}$	1.8×10^7 V/cm
	E_0	4×10^5 V/cm
	$\hbar W$	0.09 eV

Thermal conductivity:

$\lambda(T) = \frac{1}{a + bT + cT^2}$	Parameter	4H-SiC
	λ	
	a	0.01 K.cm/W
	b	6×10^{-4} cm/W
	c	6×10^{-7} cm/W.K
	C	3 J/K.cm ³

II. DEVICE STRUCTURE.

Figure II-1 shows the device structure. The design looks like a vertical power MOSFET with a gate-source short-circuit and a preformed N channel. The epitaxial layer is optimized to withstand 600V. The channel is defined by the region between the P buried layer [2] and the SiC/oxide interface. The peripheral protection is realized by guard rings. They are integrated in the process flow of the active

region. The device is normally on. The current conduction is unidirectional and the current limiting behavior is available for positive drain to source bias voltage.

Figure II-1: Vertical cut of the device and its guard rings peripheral protection (the channel length 'Lchannel' and the intercell length 'Lintercell' are noted).

III. I – V STATIC CHARACTERISTICS.

A. Static characteristic

A typical I-V curve of a current limiter is shown on the Figure III-1. The channel design controls the limitation current $I_{SATURATION}$ and the on-resistance R_{ON} . The breakdown voltage (V_{br}) is withstood by the adjusted N epilayer for 600V capability ($6 \mu\text{m}/10^{16} \text{cm}^{-3}$). Therefore, the R_{ON} value is the addition of $R_{channel}$, R_{drift} and $R_{intercell}$ (Figure II-1).

Figure III-1: typical I-V characteristic of a current limiting device.

For $0 < V_{DS} < V_{SATURATION}$, the current increases linearly with V_{DS} . When V_{DS} is over $V_{SATURATION}$, the reverse space charge region due to the $P^+/N_{channel}$ junction is wide enough to pinch off the channel. Then, the current can not increase more, and, remains equal to $I_{SATURATION}$. 2D process simulation and 2D electrical simulations with the tools package ISE TCAD [3] allow to study the electrical behavior the device. The figure III-2 shows a simulated characteristic with a current saturation of 1500 A/cm^2 and a specific on-resistance equals to $10 \text{ m}\Omega \cdot \text{cm}^2$ (compared to a

silicon 600V structure $45 \mu\text{m}/10^{14} \text{cm}^{-3}$, only $R_{drift} = w_{epi}/(qn\mu_n) \approx 250 \text{ m}\Omega \cdot \text{cm}^2$).

Figure III-2: I-V curve at T=300K (channel depth=0,3 μm ; channel length=4 μm ; channel doping level= $2 \cdot 10^{17} \text{cm}^{-3}$, Lintercell=10 μm)

B. Simple analytical model

Figure III-3: Left picture: 2D mapping of the current inside the device near the channel region. Right picture: simplified current path in the channel.

As is shown on figure III-3 (left picture), the current flow crosses the channel horizontally, and then goes down through the intercell region and the epilayer. 2D simulations are needed to evaluate the parasitic effects of the intercell JFET and SiC/oxide interface charge. However an simple analytical model can be extracted from 2D simulations. The saturation effect can be described by the JFET equation [4] with $V_{GS}=0\text{V}$ (figure III-3, right picture).

The built-in voltage and pinch-off voltage expressions are given by:

$$V_{bi} = \frac{kT}{q} \ln \left(\frac{N_A N_{channel}}{n_i^2} \right) \quad \text{and} \quad V_p = \frac{X_{jchannel}^2 q N_{channel}}{2e}$$

The space charge width expressions for both edges of the channel as defined on figure III-3 are as follows:

$$W_D = \sqrt{\frac{2e(V_{Channel} + V_{bi})}{qN_{Channel}}} \quad \text{and} \quad W_S = \sqrt{\frac{2eV_{bi}}{qN_{Channel}}}$$

The current versus voltage expression is:

$$I_{Channel}(V_{Channel}) = \frac{W}{L_{Channel}} \frac{\mu N_{channel} q^2 N_{Channel}^2}{e} gg(V_{Channel})$$

where W is the third dimension of the channel and with

$$gg(V_{Channel}) = X_{jchannel} \frac{W_D^2 - W_S^2}{2} - \frac{W_D^3 - W_S^3}{3}$$

The saturation current is given when $W_D = X_{jchannel}$. This model is used to roughly evaluate the range of each channel parameter, before running the necessary 2D numerical simulations for the device optimization.

IV. ELECTROTHERMAL SIMULATION.

In case of current surge, the current limiting device has to operate under current and high voltage simultaneously. Therefore, the self-heating of the device generates high temperature spot and could start up a thermal run away failure. Electrothermal 2D simulations have been performed to take into account the effects of the temperature on carrier mobility [5,6], carrier concentration [9]. The carrier mobility model [10,11] used is also a doping and electric field dependent model.

Figure IV-1: Current density and the maximum temperature inside the device versus time during a 500V/1ms V_{DS} -ramp. (channel depth=0,2 μm ; channel length=4 μm ; doping level= $2 \cdot 10^{17} \text{ cm}^{-3}$, $T_A=300\text{K}$, $R_{TH}=0.5 \text{ K.cm}^2/\text{W}$ at the backside, $R_{TH}=\infty$ at the topside).

Figure IV-1 shows an example of the average current density versus time and the corresponding maximal temperature inside the device during a 500V/1ms V_{DS} -ramp. When the temperature increases, the carrier mobility starts to decrease and leads the current to do the same. The hot spot is located at the end of the channel, close to SiC/oxide interface. Then, the stress of the oxide layer is quite important: high electric field ($\approx 5 \text{ MV/cm}$) and high temperature (600 K). Figure IV-2 shows the average power losses in the device versus time under the same conditions as figure IV-1. The power reached after 1ms is up to 25 kW/cm^2 and seems to saturate as the current decreases. The device keeps a good behavior even under such high

temperature conditions. The current level through the device essentially depends on the channel parameters and the electron mobility. The device structure allows to consider a good mobility value in the channel contrary to the classical SiC-MOSFET in which the inversion layer mobility is reduced by the SiC/oxide interface quality [12].

Figure IV-2: Average power versus time (Same conditions as figure IV-1).

For comparison with the silicon case, we studied a similar structure, as there is no commercial silicon current limiting device acting in the range of 20A/600V. The silicon device is a power MOSFET with an implanted channel [13], the low doped region is optimized for 600V ($45 \mu\text{m}/10^{14} \text{ cm}^{-3}$). The same thermal boundary condition as for the SiC device is used for the silicon device: $R_{TH}=0.5 \text{ K.cm}^2/\text{W}$. The resulting saturation current is 60 A/cm^2 and the on-resistance is 600 $\text{m}\Omega.\text{cm}^2$ (figure IV-3). Contrary to the SiC structure, after 0.9ms, the temperature inside is so high (intrinsic carrier level is enough) that a thermal run-away occurs and fails the silicon device (figure IV-3).

Figure IV-3: Thermal run-away of a silicon current limiting device (same V_{DS} -ramp condition and thermal boundary conditions as for the SiC device figure IV-1).

In case of a current surge during at least 10ms:

To verify the current limiting ability during a current surge, some electrothermal simulations have been performed with a copper layer (1mm) added to the backside. In this case, the thermal conductivity and the thermal capacitance of the heat-sink are considered. Figures IV-4 and IV-5 show the

simulation results. The V_{DS} waveform is a 500V/1ms ramp during the first 1ms and then a constant (500V). The maximal temperature stabilizes close to 900 K and the device keeps working. The considered structure is designed for a 1000 A/cm² saturation current density (figure IV-5).

Figure IV-4: Electrothermal behavior in case of >10ms current surge.

Figure IV-5: Comparison of the static I-V characteristic and electrothermal transient behavior (same structure as figure IV-4).

	SiC	Silicon
$J_{SATURATION}$	1000 A/cm ²	60 A/cm ²
R_{ON}	8 mΩ.cm ²	600 mΩ.cm ²
$V_{SATURATION}$	8V	36V
Max temperature reached	900K	650K (before run-away)
Time without run-away	At least 20ms	0.9 ms

Table 1: Ratings of both SiC and silicon device.

The silicon device is not adapted for this kind of application; the current density range and the specific on-state resistance lead to build device with surface of 1 cm² almost for a saturation current of 60A ($R_{ON} \approx 0.6 \Omega$). To avoid the thermal run-away of the silicon device during at least 10ms, the saturation current density should be reduced and then the surface should be increased. Silicon carbide is

well adapted (Table 1), can work with low surface (6 mm² for $I_{SAT} = 60A$ and $R_{ON} \approx 0.1 \Omega$) and with a thermal boundary of 1 mm copper layer.

V. CONCLUSION

According to our simulation study, silicon carbide seems very attractive for current limiting application. The concept presented here can be applied to a large range of currents and voltages. The breakdown voltage could be improved without dramatically increases the on-resistance value (1500V – 10μm/5 10¹⁵ cm⁻³). The device could even be controlled with a gate electrode for the switching off. It could be useful not only for serial protection but also for other applications, as for example, the motor starting phase.

Acknowledgment

We acknowledge SCHNEIDER ELECTRIC S.A for their support.

References

- [1] F. Nallet, D. Planson, K. Isoird, M.L. Locatelli, J.P. Chante, "Comparison Of Static, Switching And Thermal Behavior Between a 1500V Silicon and SiC Bipolar Diodes", CAS'99 Proceedings, pp. 195-198, October 1999
- [2] P.M. Shenoy, B.J. Baliga, "High Voltage Planar 6H-SiC ACCUFET", Materials Science Forum Vols. 264-268 (1998) pp. 993-996, Trans Tech Publications, Switzerland.
- [3] ISE Integrated Systems Engineering AG, Zurich/CH (1998)
- [4] S.M. Sze, "Physics Of Semiconductor Devices", 2nd Edition, John Wiley & Sons, Inc, ISBN 0-471-09837-X
- [5] Pensl G. et al, "Electrical And Optical Characterisation of SiC", Physica B 185 (1993), pp 265-273
- [6] T. Troffer, M. Schadt, T. Frank, H. Itoh, G. Pensl, "Doping of SiC by Implantation of Boron and Aluminium", Phys. Stat. Sol. (a) 162, 277 (1997)
- [7] St.G. Müller, R. Eckstein, "Experimental and theoretical analysis of the high temperature thermal conductivity of monocrystalline SiC", ICSCIII'97 Sweden.
- [8] Glen A. Slack, "Thermal conductivity of Pure and Impure silicon, SiC, and diamond", *J. Apply. Phys.* 35 (12), pp. 3460-66, Dec 1964.
- [9] R. Raghunathan, B. J. Baliga, "Temperature dependence of hole impact ionization coefficients in 4H and 6H-SiC", *Solid State Electronics*, vol 43, pp. 199-211, 1999
- [10] D. M. Caughey and R. E. Thomas, "Carrier mobilities in Silicon empirically related to doping and field", *Proc. IEEE*, pp. 2192-93, Dec. 1967.
- [11] C. Canali, G. Majni, R. Minder, and G. Ottaviani, "Electron and hole drift velocity measurements in Silicon and their empirical relation to electric field and temperature", *IEEE Trans. on Elect. Dev.*, Vol. ED-22, pp. 1045-47, 1975.
- [12] T. Ouisse, "Electron Transport at the SiC/SiO₂ Interface", *phys. Stat. Sol (a)* 162, 339 (1997)
- [13] J.L. Sanchez, Ph. Leturcq, P. Austin, "Design and fabrication of new silicon high voltage current limiting devices", 8th Int. Symp. on Power Semi. Devices and ICs (ISPSD'96), Hawaii (USA), 20-23 Mai 1996, pp.201-205