Low temperature high voltage analog devices in a 3D sequential integration

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ABSTRACT

We built an original stackable 2.5V device on FDSOI with analog performance comparable to high temperature reference and passing the PBTI reliability criteria. In depth characterization of low temperature (LT) gate stack devices with thick EOT are investigated, enabling to draw guidelines for future optimization. This paper demonstrates the feasibility of LT high V_{DD} analog devices, which can be used for sensor read out operation, paving the way to ultra-miniaturized smart sensor arrays.

INTRODUCTION

3D sequential integration (3DSI) consists in stacking active device layers on top of each other, in a sequential manner [1]. 3DSI has been identified as a key technology for More-Than-Moore applications, thought to be particularly adapted for miniaturized smart sensors arrays [2,3] (Fig. 1). The challenge of 3DSI relies in processing top devices with a limited thermal budget (TB), to prevent degradation of the bottom layer. While significant work has been done to develop high-performance low TB devices for digital applications $V_{DD}=0.8/1V$ [4-9], almost no work has been published on higher voltage devices. This work presents for the first time, 2.5V devices fabricated with TB in the 500°C range. In-depth electrical characterization is provided in order to conclude on the potential use of these devices for analog applications.

LOW TB 2.5V ANALOG MOSFET

Architecture - The fabricated FDSOI device have 30nm thick undoped channel, 25nm BOX, and $SiO_2 = 6nm/TiN/Poly-Si$ gate stack (Fig. 2). A High Temperature Oxide (HTO) is used as reference. Three types of LT oxides (<500°C) have been compared (1: 6nm plasma oxidation in O_2/H_2 (named $PI-O_2/H_2$); 2: 1.6nm plasma oxidation in $O_2+PEALD$ deposition ($PI-O_2+PEALD$); 3: 6nm PEALD). Post Deposition Treatments (PDT) has also been tested (450°C O_2 plasma densification and 500°C N_2 furnace anneal). For LT devices, Solid Phase Epitaxy Regrowth (SPER) at 500°C 30min was used for junction activation. The HTO ref device underwent conventional high temperature S/D activation anneal (Fig.3).

Gate Stack Characterization - The I_{ON}/I_{OFF} trade-off is shown (Fig. 4), where a clear I_{ON} shift is observed for the LT oxide splits w.r.t HTO. Given that all the LT splits have the same S/D process, the effect is attributed to the gate stack properties, analyzed independently for N&P in the following part. Several techniques are used to extract oxide features: low field mobility (μ_0) from the Y function [10], interface state density (D_{it}) from the Subthreshold Slope SS [11] and oxide trap volumetric density (N_t) from Low Frequency Noise measures (LFN) [12] at $T=25^\circ C$. Bias Temperature Instability (BTI) at $T=125^\circ C$ is also characterized using a fast measurement technique [13].

NMOS devices - Fig. 5 a-c depicts the maximum low-field mobility (μ_0), D_{it} and N_t . Higher D_{it} values are extracted on LT oxides. This results in an enhanced Coulomb scattering effect, degrading the mobility w.r.t HTO. The $PI-O_2/H_2$ exhibit better mobility amongst the LT splits, explained by its lower $D_{it}=2 \times 10^{-11}/cm^2/eV$. The later also presents the lower $N_t=3 \times 10^{18} eV/cm^3$; It may result from a better passivation of the dangling bonds by H^0 incorporated during the

plasma oxidation step [14]. Concerning PDT efficiency, better surface passivation is achieved with a reactive plasma O_2 applied on $PI-O_2+PEALD$, while the effect is limited for the furnace N_2 split. Further improvement of the Si/SiO_2 interface can be achieved with a forming gas under High-Pressure Deuterium anneal (HPD₂) [15]. Finally, PBTI is investigated (Fig. 5 d). PBTI in LT oxides are comparable, or even better for the $PI-O_2/H_2$ w.r.t HTO. It also largely meets the 5 years requirement at $V_{DDmax}=2.5V$. Note that N_t and PBTI results are not correlated. This is because traps responsible for both phenomena are not same (Fig. 7). Noise is mainly sensitive to D_{it} while PBTI is due to trapping in a band of “deep” defects localized above the silicon conduction band.

PMOS devices - Fig. 6 b-c report D_{it} & N_t densities. Both are (1) much higher than for NMOS and the HTO and (2) almost independent of the LT oxide. This asymmetry between N&P implies that not only silicon dangling bonds contribute to D_{it} & N_t , but also border traps (Fig. 7). D_{it} for PMOS actually refers to the sum of interface and border traps, and not to pure dangling bonds, with the method to extract D_{it} from the SS not being able to separate the two contributions. Moreover, these N_t values are well correlated to NBTI results [Fig. 6 d)], suggesting that, this time, the defects responsible for noise & NBTI are the same. Comparing the oxides, the TTF for the best LT oxide $PI-O_2/H_2$ is degraded by ~4 decades w.r.t. HTO. Additionally, no improvement has been achieved with PDT. This confirms that NBTI remains a major issue for LT gate stacks [15-17]. NBTI was associated to traps located in the interlayer and high-k [17]. Despite the high-k suppression of our stack, NBTI remains problematic, which could be an indication that the traps are actually mainly located in the SiO_2 .

Oxide traps on N&P devices - Three types of oxide traps have been identified: “deep”, border and interface traps (Fig. 7). For NMOS, the majority of active traps are interface/dangling bonds located in the bandgap, which affects mobility features. There are also some high energetic “deep” traps in the bulk of the SiO_2 , responsible for electron trapping upon high field PBTI stress. For PMOS, in addition to dangling bonds, border donor traps must be considered. They are located close to the Si/SiO_2 interface (~1nm depth), and affect all the device characteristics such as SS, noise and NBTI.

Analog Figure of Merit - N&P gm/Id ratio of the HTO reference and the best LT split ($PI-O_2/H_2$) are compared (Fig. 8). In the region below threshold ($I_D=1 \times 10^{-9}A$), gm/Id values in the range of $30V^{-1}$ are found for both HTO and the LT device. Additionally, the same voltage gain is observed between long and short L_G , offering a range of utilization for circuit designers. Similarly, no degradation is observed for the nominal gate length ($L_G=300nm$) from the analog gain gm/gd (Fig. 9).

CONCLUSIONS

This work enable to conclude on the feasibility of stacking high voltage analog devices in a 3DSI for More-than-Moore applications. Low-cost and low thermal budget 2.5V devices show good analog performance. Reliable NMOS devices were demonstrated, ideal for readout circuits with NFETs only. An identification of the defects present in LT SiO_2 oxides is provided by means of complementary electrical characterization.

Fig. 1 Schematics of digital/analog bilayer sensors interface module for sensing applications for a) Back side sensors and b) for above IC sensors. In both cases, analog devices have to be fabricated at LT. (SSI = smart sensor interfaces)

Fig. 2 TEM cross-section of the proposed analog FDSOI architecture. $T_{Si} = 30\text{nm}/\text{SiO}_2 = 6\text{nm}$.

Fig. 3 a) Detailed process flow of HT and LT devices and b) summary of the LT oxide with its respective split name. Owing to the thicker SiO_2 , different oxide deposition are used in comparison to advanced digital devices. Post deposition treatments such as plasma densification and furnace anneal were also tested.

Fig. 4 I_{ON}/I_{OFF} trade off of N&P devices for all LT oxide splits and HTO reference. $L = 1\mu\text{m}$, $V_{DD} = 2.5\text{V}$. I_{ON} shift between LT splits is attributed to the gate stack dielectric.

Fig. 5 a) Mobility peak μ_0 . b) Calculated interface state density. c) Bulk oxide trap density deduced from LFN measurements with the CNF/CMF model. Inset: fit of the normalized drain current noise S_{Id}/I_d^2 with drain current I_d . d) PBTI TimeToFailure vs Oxide field. All oxides fulfill the 5 years requirements (purple dashed line). ΔV_{th} of 50mV is used as criterion for BTI lifetime prediction. The grey square area represents the forbidden zone, where the criteria is not reached.

Fig. 6 a) Mobility peak μ_0 . b) Calculated interface state density. c) Bulk oxide trap density N_t . d) NBTI TimeToFailure vs oxide field. Unlike NMOS, no significant differences between LT splits are seen on the mobility. Also, all splits present a larger amount of D_{it} and N_t and no improvement after PDT is observed. The NBTI remains critical for all LT oxides - extrapolated 5y TTFs fall inside the forbidden zone.

Fig. 7 Summary of oxide traps impacting device performance and reliability. a) 3 types of traps are identified namely deep -/0, border +/0 and interface defects. b) PBTI in NMOS is driven by e^- trapping in high energetic defects. c) NBTI in PMOS is controlled by the filling & creation of both Si dangling bonds and hole border traps.

Fig. 8 N&P FETs gm/Id ($V_d=0.9\text{V}$) of HT & the best LT split $\text{PI-O}_2/\text{H}_2$. ($L_g = 1\mu\text{m}$ and $L_g = 0.3\mu\text{m}$).

Fig. 9 N&P FETs gm/gd versus L_g . The LT split $\text{PI-O}_2/\text{H}_2$ is not degraded w.r.t to the HTO reference.

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