

Performance and Low-Frequency Noise of 22-nm FDSOI Down to 4.2 K for Cryogenic Applications

Bruna Cardoso Paz, Mikaël Cassé, Christoforos Theodorou, Gérard Ghibaudo, Thorsten Kammler, Luca Pirro, Maud Vinet, Silvano de Franceschi, Tristan Meunier, Fred Gaillard

▶ **To cite this version:**

Bruna Cardoso Paz, Mikaël Cassé, Christoforos Theodorou, Gérard Ghibaudo, Thorsten Kammler, et al.. Performance and Low-Frequency Noise of 22-nm FDSOI Down to 4.2 K for Cryogenic Applications. IEEE Transactions on Electron Devices, 2020, 67 (11), pp.4563-4567. 10.1109/TED.2020.3021999 . hal-02969741

HAL Id: hal-02969741
https://hal.science/hal-02969741

Submitted on 25 Nov 2021

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

Performance and Low Frequency Noise of 22nm FDSOI down to 4.2K for Cryogenic Applications

Bruna Cardoso Paz, Mikaël Cassé, Christoforos Theodorou, Gérard Ghibaudo, Fellow IEEE, Thorsten Kammler, Luca Pirro, Maud Vinet, Silvano de Franceschi, Tristan Meunier and Fred Gaillard

***Abstract*—This work presents the performance and low frequency noise of 22nm FDSOI CMOS technology. The experimental measurements and the analysis are performed as a function of temperature for the first time, focusing on cryogenic applications, down to 4.2K. The back bias impact on device performance is evaluated. The results reveal that the threshold voltage tuning is found to be temperature independent, allowing extra drain current improvement. This is particularly interesting for short channel devices, whose drain current gain with temperature lowering is expected to be smaller in comparison to long channel MOSFETs. Low frequency noise is characterized by means of time-domain current sampling measurements. Moderate and strong inversion regimes are investigated. The carrier number with correlated mobility fluctuations model can well describe the 1/f noise behavior down to 4.2K. The physical origin behind the drain current low frequency noise to signal power augmentation with temperature lowering could be mainly attributed to the normalized transconductance improvement.**

***Index Terms*—Cryogenic applications, FDSOI MOSFET, low frequency noise.**

I. INTRODUCTION

THE interest in cryogenic electronics relies on several applications, such as space and cooling systems [1], [2], and has been recently boosted by the quantum computing field [3], [4]. Recently, monolithic integration between qubits and readout circuitry has been demonstrated at 2K in 22nm FDSOI technology [5], and the electrical performance of several CMOS technologies has shown to be significantly improved with temperature (T) decrease [6]–[8]. On the other hand, in [9] it is indicated that the low frequency noise to signal power increases at cryogenic T, especially in the presence of subband scattering mechanisms [10]. Moreover, in [11] the authors claim that low frequency charge noise is one of the key parameters to improve qubit fidelity in Si spin qubits.

To the best of our knowledge, the performance of 22nm FDSOI MOSFETs at deep cryogenic temperatures has not been explored yet, especially regarding the device optimization by means of forward back biasing (FBB). Furthermore, there is a lack of information on low frequency noise (LFN) behavior at cryogenic temperatures available in literature for commercial technologies. In this work, our goal is to cover the above mentioned topics, concerning advanced FDSOI MOSFET characterization at 4.2K, with special focus on the origin of LFN down to 4.2K and the underlying physics.

This work was partially supported by the French Authorities within the frame of NANO2022 project, the ERC Synergy QuCube (Grant No. 810504 — QUCUBE — ERC-2018-SyG), and EU H2020 RIA project SEQUENCE (Grant No. 871764).

B. C. Paz, M. Cassé, M. Vinet and Fred Gaillard are with CEA-Leti, Université Grenoble Alpes, MINATEC Campus, 38054 Grenoble, France. (bruna.cardosopaz@cea.fr)

C. Theodorou and G. Ghibaudo are with IMEP-LAHC, CNRS, Université Grenoble Alpes, MINATEC Campus, 38016 Grenoble, France.

T. Kammler and L. Pirro are with GlobalFoundries, 01109 Dresden, Germany.

S. de Franceschi is with CEA-IRIG, 38054 Grenoble, France.

T. Meunier is with Institut Néel, 38042 Grenoble, France.

II. DEVICES CHARACTERISTICS AND METHODOLOGY

Si NMOSFETs and SiGe (with Ge content around 25%) PMOSFETs fabricated with gate-first High-K Metal Gate integration in commercial 22nm FDSOI CMOS technology [12] were evaluated in this work. The undoped semiconductor channel is about 6nm thin, whereas the buried oxide thickness is 20nm and the equivalent oxide thickness (EOT) is around 1.3nm.

Experimental measurements were performed down to 4.2K using a manual cryogenic probe station. Fast IV module B1530A from Agilent was used for low frequency noise characterization through time-domain current sampling measurements [13]. For spectral analysis, Welch function was used to apply the Fourier transform and obtain the power spectral density.

III. PERFORMANCE DEPENDENCE ON TEMPERATURE

Fig. 1 presents the drain current (I_{DS}) as a function of the gate voltage (V_{GS}) at high and low drain bias (V_{DS}), for N- and PMOS, down to 4.2K. Temperature lowering leads to expected threshold voltage (V_{TH}) and I_{DS} increase, in absolute values, for both N- and PMOS. As T decreases, the balance between mobility increase and V_{TH} shift towards higher absolute value originates the zero-temperature coefficient (ZTC). Since the T-dependence of V_{TH}, $|\Delta V_{TH}/\Delta T|$, is higher for PMOS (≈0.71mV/K, in comparison to ≈0.57mV/K for NMOS), larger V_{DS} dependence if found for V_{ZTC} [14].

Fig. 2 (a) shows V_{TH} as a function of T for NMOS at V_{DS} = 50mV and 0.9V, and at a back gate bias (V_B) of 0V and 1.4V. The applied 1.4V at the back bias gives the same V_{TH} value as for the device

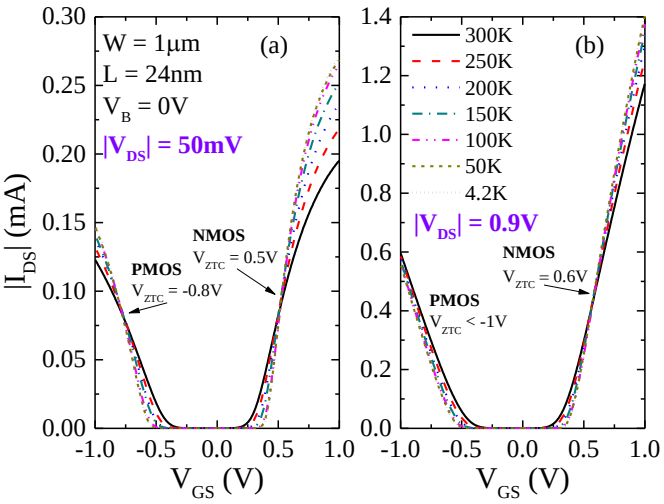


Fig. 1. $|I_{DS}|$ *versus* V_{GS} at $|V_{DS}|$ = 50mV (a) and 0.9V (b), for N- and PMOS, varying T from 300K to 4.2K.

operating at room temperature. Fig. 2 (b) indicates the V_B required to shift V_{TH} back to its value at 300K for each temperature operation. FBB is an efficient way to correct the significant V_{TH} increase with T lowering and, therefore, enhance power efficiency. The measured Drain-Induced Barrier Lowering (DIBL) is ≈74mV/V at both conditions, at 300K with V_B = 0V and at 4.2K with V_B = 1.4V.

Fig. 3 (a) presents V_{TH} as a function of V_B for short-channel N- and PMOS at 300K and 4.2K. The back bias efficiency, evaluated through the body factor ($\gamma = \Delta V_{TH}/\Delta V_B$) does not change with T. This is because the doping concentration of the back planes in ultra-thin body and buried oxide MOSFETs is high enough to be always activated in such a way that they do not suffer from any freeze-out effects [15], which could reduce γ at low T. Fig. 3 (b) shows γ as a function of T for N- and PMOSFETs with three different channel lengths, L = 24nm, 70nm and 1µm. Fig. 3 (b) confirms that γ is T-independent, since $\Delta\gamma/\Delta T < 5\%$ for all studied devices. Therefore, the back bias remains a powerful tool down to cryogenic T and can still be used to facilitate circuits design [16]. We can observe slightly lower |γ| as the channel length becomes shorter, likely due to stronger influence of source and drain potentials inside the channel in shorter transistors. The difference between γ in N- and PMOS is expected since the position of the inversion layer in the channel (centroid of charges) differs according to the type of carriers (hole *versus* electron) and channel material (SiGe *versus* Si) [17].

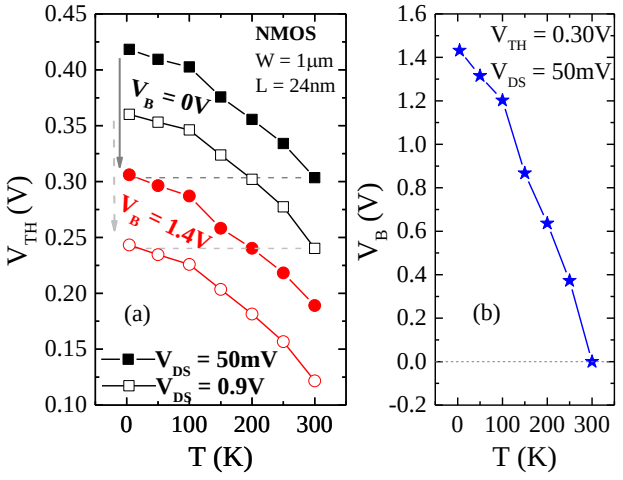


Fig. 2. V_{TH} *versus* T at V_{DS} = 50mV and 0.9V, and at V_B = 0V and 1.4V (a). V_B needed to shift V_{TH} back to its value at 300K for each temperature operation, at V_{DS} = 50mV (b).

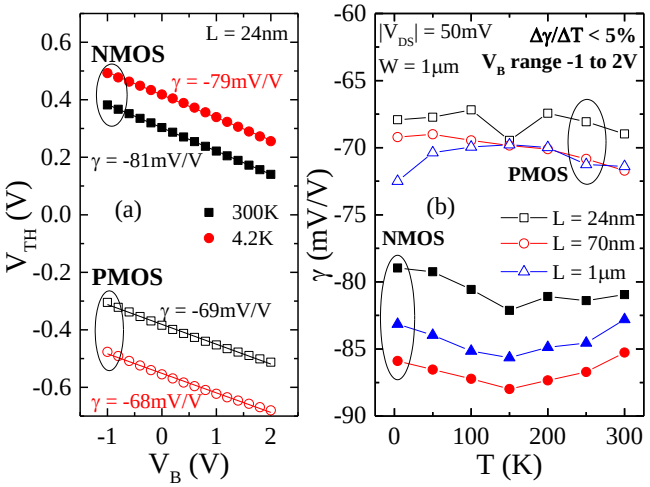


Fig. 3. V_{TH} *versus* V_B (a) and γ *versus* T (b) for N- and PMOS, at $|V_{DS}|$ = 50mV.

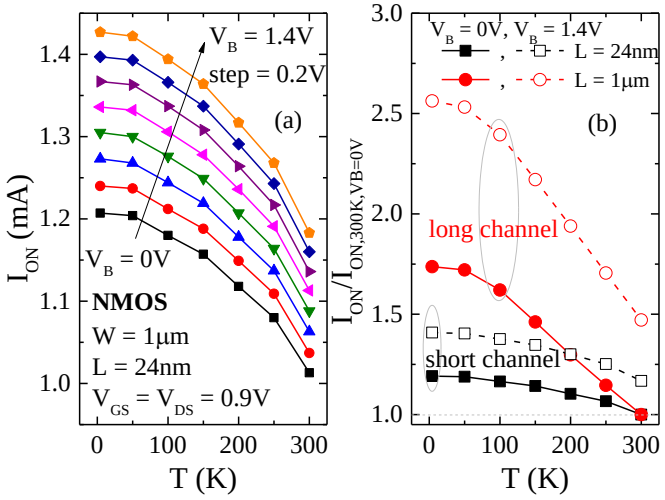


Fig. 4. I_{ON} *versus* T for NMOS, at $V_{GS} = V_{DS}$ = 0.9V, and varying V_B (a). $I_{ON}/I_{ON,ref}$ *versus* T for long and short channels NMOS, at $V_{GS} = V_{DS}$ = 0.9V, and at V_B = 0V and 1.4V (b).

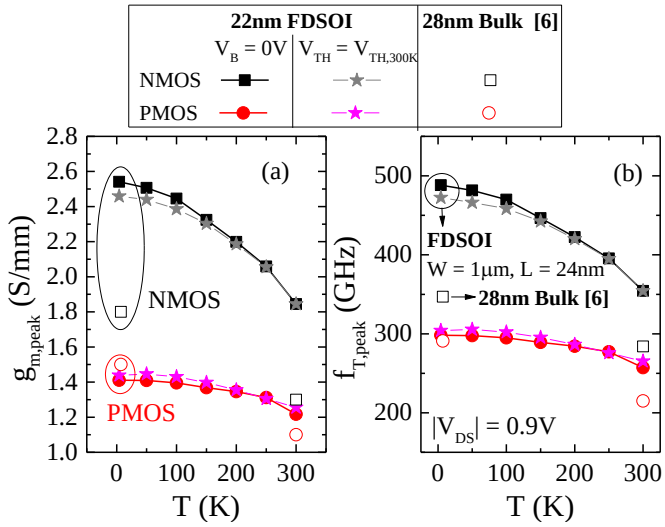


Fig. 5. $g_{m,peak}$ *versus* T (a) and $f_{T,peak}$ *versus* T (b) for N- and PMOS, at V_B = 0V and at V_B needed to keep V_{TH} constant = $V_{TH,300K}$. $|V_{DS}|$ = 0.9V.

TABLE I
EXTRACTED THRESHOLD VOLTAGE

	22NM FDSOI – THIS WORK		28NM BULK – [6]	
	NMOS	PMOS	NMOS	PMOS
300K	0.24V	-0.33V	0.26V	-0.37V
7K	0.36V	-0.50V	0.35V	-0.45V

Fig. 4 (a) shows the on-state current (I_{ON}) as a function of T for NMOS at $V_{GS} = V_{DS}$ = 0.9V and varying V_B. The I_{ON} gain observed with T decrease is attributed to the effective mobility increase due to suppression of phonon scattering contribution [18], whereas the I_{ON} gain with FBB is the consequence of the V_{TH} shift, and thus gate voltage overdrive ($V_{GT} = V_{GS} - V_{TH}$) increase. Fig. 4 (b) shows I_{ON} normalized by I_{ON} extracted at 300K and no back bias, $I_{ON}/I_{ON,ref}$, as a function of T for short and long NMOSFETs. The I_{ON} gain with T reduction and FBB is higher for the long channel MOSFET in comparison to short channel one. This could be explained by the fact that shorter MOSFETs suffer from stronger self-heating effect [19], due to higher normalized input power, but also from larger access resistance impact and stronger contribution of T-independent transport mechanisms, related to neutral defect scattering and/or ballisticity effect [20].

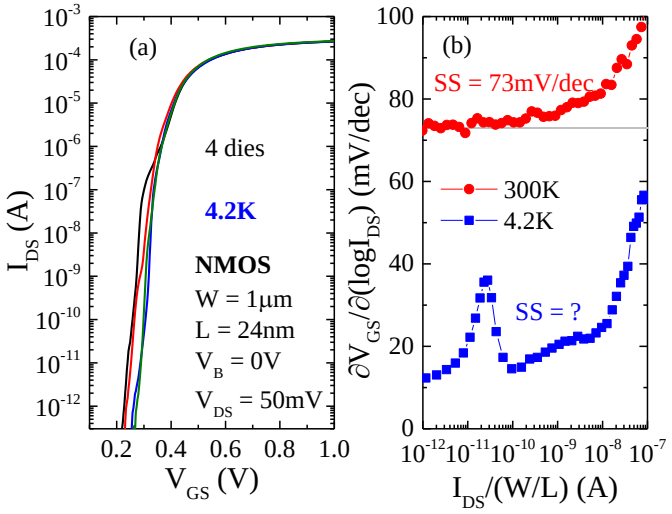


Fig. 6. I_{DS} *versus* V_{GS} (a) and $\partial V_{GS}/\partial(\log I_{DS})$ *versus* $I_{DS}/(W/L)$ (b) for short channel NMOS, at V_{DS} = 50mV.

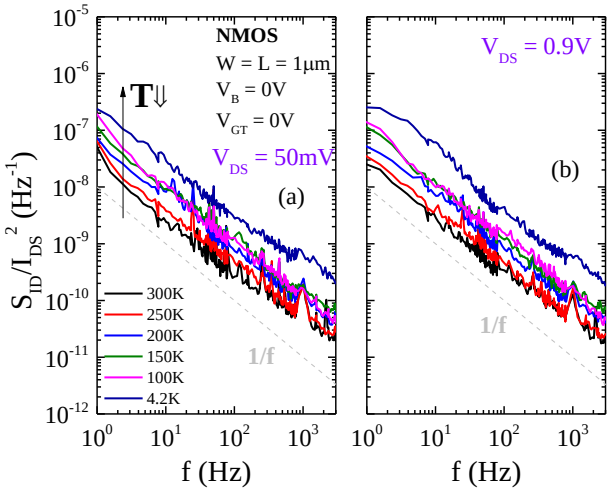


Fig. 7. S_{ID}/I_{DS}^2 *versus* f for NMOS, varying T, at V_{GT} = 0V and at V_{DS} = 50mV (a) and 0.9V (b).

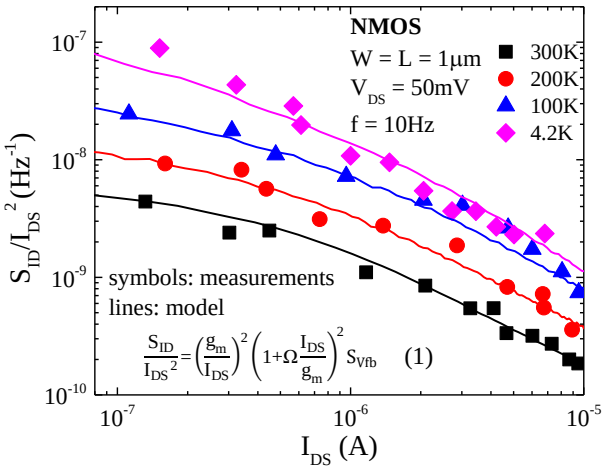


Fig. 8. S_{ID}/I_{DS}^2 *versus* I_{DS} for NMOS at different T conditions, $|V_{DS}|$ = 50mV, and at f = 10Hz. Lines indicate the CNF/CMF model [23]. $\Omega = 4V^{-1}$.

Fig. 5 (a) shows the maximum transcondutance ($g_{m,peak}$) and (b) the respective cutoff frequency ($f_{T,peak}$) as a function of T. The $f_{T,peak}$ values in this work were calculated from $g_{m,peak}/(2.\pi.C_{ox}.W.L)$ where C_{ox} = 0.028F/m^2 is the oxide capacitance per unit area, and are very similar to those obtained using RF characterization in [12], at 300K. Curves are presented for two bias configuration, at fixed V_B = 0V and at V_B required to keep V_{TH} constant at its value obtained at 300K ($V_{TH,300K}$). A very small V_B impact in $g_{m,peak}$ (around ±3%) is observed for the short channel transistors in Fig. 5, while for long channel MOSFETs, FBB is found to improve $g_{m,peak}$ results in a more significant way (up to +11%, not shown). This indicates that power consumption optimization can be achieved by means of back biasing, while >450GHz cutoff frequency is kept. Moreover, we clearly observe the $g_{m,peak}$ (and therefore $f_{T,peak}$) improvement with T lowering for both NMOS (up to 38%) and PMOS (up to 16%). The results obtained in this work for 22nm FDSOI are benchmarked against 28nm Bulk CMOS technology [6]. RVTn and HVTp flavors from [6] were chosen for comparison to match similar V_{TH} to our devices, as indicated in Table I. From the $f_{T,peak}$ values in Fig. 5 (b), it is observed that FDSOI outperforms Bulk, especially for the NMOSFET, where a large $g_{m,peak}$ gain is obtained at cryogenic temperatures.

A. *Subthreshold regime*

Fig. 6 presents $I_{DS}(V_{GS})$ for a short device measured in 4 different dies at 4.2K (a), and the swing $\partial V_{GS}/\partial(\log I_{DS})$ as a function of the normalized current at 300K and 4.2K (b). Unlike the room temperature operation, where the subthreshold swing (SS) can be easily extracted, the appearance of oscillatory regime likely due to quantum interference in the subthreshold region at cryogenic temperatures makes it difficult to extract SS at 4.2K, due to the strong dependence of this parameter on the current level used for the extraction. As shown in Fig. 6 (a), this phenomenon presents high variability. The extracted ideality factor (η) is ≈1.22 at 300K, and more than 10 at 4.2K, which cannot be explained by an increase of the interface trap density, but the appearance of an exponential tail of states in the subband, as discussed in [21], [22], which leads to the SS saturation *versus* T below ≈50K. From a performance point of view, even though the experimental SS is much higher than the theoretical limit at 4.2K (SS ≈ 0.8mV/dec), it induces an off-state current (I_{OFF}) reduction of several orders of magnitude in comparison to the room temperature operation, lying below the equipment accuracy (1fA).

IV. Low Frequency Noise

Fig. 7 presents the normalized drain current power spectral density (S_{ID}) as a function of frequency (f), varying T, in linear (a) and saturation (b) regimes. From 300K down to 4.2K, both N- and PMOSFET (not shown) exhibit 1/f noise behavior. Moreover, S_{ID}/I_{DS}^2 increases with temperature reduction. In order to identify the sources of noise and explain its behavior with T, S_{ID}/I_{DS}^2 values at 10Hz are presented as a function of I_{DS}, from moderate to strong inversion in Fig. 8. The lines indicate the carrier number fluctuations with correlated mobility fluctuations (CNF/CMF) analytical model described in equation (1), where Ω is a noise parameter related to the Coulomb scattering coefficient and S_{Vfb} is the flat band voltage power spectral density related to the trapping/detrapping of carriers in slow oxide states [23]. Since good agreement between the data and the model is obtained from 300K down to 4.2K, we can conclude that carrier number fluctuation and correlated mobility fluctuation are the sources of noise, and the 1/f noise to signal power increases with T lowering because of the g_m/I_{DS} improvement, on the same way as previously found for bulk CMOS [24]. Moreover, as the 1/f noise decays with exponent equal to 1, *i.e.* trap distribution exponential factor = 1, the oxide traps are mostly uniformly distributed in depth, inside the gate oxide.

Results of S_{Vfb} were extracted using the equation (1), for N- and

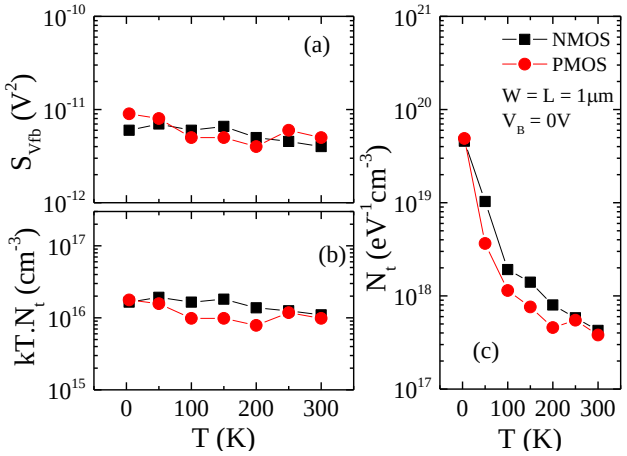


Fig. 9. S_{Vfb} (a), kT.N_t (b) and N_t (c) *versus* T for N- and PMOS. $N_t = S_{Vfb}.W.L.f.C_{ox}^2/q^2.\lambda.kT$, where λ is the tunneling constant in the dielectric.

PMOS. For all T conditions, Ω is found to be constant and equal to $4V^{-1}$. We can observe, in Fig. 9 (a), that S_{Vfb} values are roughly constant with T. The same behavior is verified for the calculated oxide trap density, N_t, normalized by 1/kT in Fig. 9 (b). Fig. 9 (c) shows a large increase of the active trap density at cryogenic temperatures. This is because the accessed energy distribution gets closer to the conduction (for NMOS) and valence (for PMOS) bands as T reduces. The high N_t values obtained at 50K and 4.2K can be explained by the existence of the disorder-induced exponential tail at the subband edges, where the Fermi level lies at very low temperatures [25].

V. Conclusion

In this work, we have shown that FDSOI is a good option for cryogenic-CMOS applications. While MOS performance significantly improves with T lowering, reaching I_{ON} > 1.2mA/µm and f_T close to 500GHz, high back biasing efficiency remains a powerful tool for circuit optimization down to 4.2K. Back biasing can be safely used for V_{TH} tunability, improving circuits performance at low T, especially when low dynamic power consumption and high bandwidth are required, e.g. quantum integrated circuits [26]. The g_m/I_{DS} improvement was correlated to the normalized drain current power spectral density increase at cryogenic T, being the CNF + CMF model valid from 300K down to 4.2K. Both noise parameters S_{Vfb} and Ω were found to be approximately constant with T, for the studied drain current range.

References

[1] T. Chen *et al.*, "CMOS reliability issues for emerging cryogenic Lunar electronics applications," *Solid-State Electron.*, vol. 50, no. 6, pp. 959–963, Jun. 2006, doi: 10.1016/j.sse.2006.05.010.

[2] F. Zocca, A. Pullia, S. Riboldi, A. D'Andragora, and C. Cattadori, "Setup of cryogenic front-end electronic systems for germanium detectors read-out," in *2009 IEEE Nuclear Science Symposium Conference Record (NSS/MIC)*, Oct. 2009, pp. 368–372, doi: 10.1109/NSSMIC.2009.5401690.

[3] F. Jazaeri, A. Beckers, A. Tajalli, and J.-M. Sallese, "A Review on Quantum Computing: Qubits, Cryogenic Electronics and Cryogenic MOSFET Physics," *ArXiv190802656 Phys. Physicsquant-Ph*, Aug. 2019, Accessed: Aug. 08, 2019. [Online]. Available: http://arxiv.org/abs/1908.02656.

[4] E. Charbon *et al.*, "Cryo-CMOS for quantum computing," in *2016 IEEE International Electron Devices Meeting (IEDM)*, Dec. 2016, p. 13.5.1-13.5.4, doi: 10.1109/IEDM.2016.7838410.

[5] S. Bonen *et al.*, "Cryogenic Characterization of 22-nm FDSOI CMOS Technology for Quantum Computing ICs," *IEEE Electron Device Lett.*, vol. 40, no. 1, pp. 127–130, Jan. 2019, doi: 10.1109/LED.2018.2880303.

[6] J. C. Bardin *et al.*, "Design and Characterization of a 28-nm Bulk-CMOS Cryogenic Quantum Controller Dissipating Less Than 2 mW at 3 K," *IEEE J. Solid-State Circuits*, vol. 54, no. 11, pp. 3043–3060, Nov. 2019, doi: 10.1109/JSSC.2019.2937234.

[7] H. Bohuslavskyi *et al.*, "28nm Fully-depleted SOI technology: Cryogenic control electronics for quantum computing," in *2017 Silicon Nanoelectronics Workshop (SNW)*, Jun. 2017, pp. 143–144, doi: 10.23919/SNW.2017.8242338.

[8] R. M. Incandela, L. Song, H. Homulle, E. Charbon, A. Vladimirescu, and F. Sebastiano, "Characterization and Compact Modeling of Nanometer CMOS Transistors at Deep-Cryogenic Temperatures," *IEEE J. Electron Devices Soc.*, vol. 6, pp. 996–1006, 2018, doi: 10.1109/JEDS.2018.2821763.

[9] D. Boudier, B. Cretu, E. Simoen, A. Veloso, and N. Collaert, "Detailed characterisation of Si Gate-All-Around Nanowire MOSFETs at cryogenic temperatures," *Solid-State Electron.*, vol. 143, pp. 27–32, May 2018, doi: 10.1016/j.sse.2018.02.015.

[10] B. Nafaa *et al.*, "Low-frequency noise measurements at liquid helium temperature operation in ultra-thin buried oxide transistors – Physical interpretation of transport phenomena," *Solid-State Electron.*, vol. 150, pp. 1–7, Dec. 2018, doi: 10.1016/j.sse.2018.08.010.

[11] T. Struck *et al.*, "Low-frequency spin qubit energy splitting noise in highly purified 28 Si/SiGe," *Npj Quantum Inf.*, vol. 6, no. 1, pp. 1–7, May 2020, doi: 10.1038/s41534-020-0276-2.

[12] R. Carter *et al.*, "22nm FDSOI technology for emerging mobile, Internet-of-Things, and RF applications," in *2016 IEEE International Electron Devices Meeting (IEDM)*, Dec. 2016, p. 2.2.1-2.2.4, doi: 10.1109/IEDM.2016.7838029.

[13] C. G. Theodorou *et al.*, "New LFN and RTN analysis methodology in 28 and 14nm FD-SOI MOSFETs," in *2015 IEEE International Reliability Physics Symposium*, Apr. 2015, p. XT.1.1-XT.1.6, doi: 10.1109/IRPS.2015.7112833.

[14] A. A. Osman, M. A. Osman, N. S. Dogan, and M. A. Imam, "Zero-temperature-coefficient biasing point of partially depleted SOI MOSFET's," *IEEE Trans. Electron Devices*, vol. 42, no. 9, pp. 1709–1711, Sep. 1995, doi: 10.1109/16.405293.

[15] A. Beckers, F. Jazaeri, H. Bohuslavskyi, L. Hutin, S. De Franceschi, and C. Enz, "Design-oriented Modeling of 28 nm FDSOI CMOS Technology down to 4.2 K for Quantum Computing," *2018 Jt. Int. EUROSOI Workshop Int. Conf. Ultim. Integr. Silicon EUROSOI-ULIS*, pp. 1–4, Mar. 2018, doi: 10.1109/ULIS.2018.8354742.

[16] F. Arnaud *et al.*, "Enhanced design performance thanks to adaptative body biasing technique in FDSOI technolologies," in *2017 IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S)*, Oct. 2017, pp. 1–5, doi: 10.1109/S3S.2017.8308754.

[17] J. Noel *et al.*, "Multi-$_T$UTBB FDSOI Device Architectures for Low-Power CMOS Circuit," *IEEE Trans. Electron Devices*, vol. 58, no. 8, pp. 2473–2482, Aug. 2011, doi: 10.1109/TED.2011.2155658.

[18] M. Casse *et al.*, "Carrier transport in HfO2/metal gate MOSFETs: physical insight into critical parameters," *IEEE Trans. Electron Devices*, vol. 53, no. 4, pp. 759–768, Apr. 2006, doi: 10.1109/TED.2006.870888.

[19] K. Triantopoulos *et al.*, "Self-Heating Effect in FDSOI Transistors Down to Cryogenic Operation at 4.2 K," *IEEE Trans. Electron Devices*, vol. 66, no. 8, pp. 3498–3505, Aug. 2019, doi: 10.1109/TED.2019.2919924.

[20] G. Ghibaudo *et al.*, "Electrical transport characterization of nano CMOS devices with ultra-thin silicon film," in *2009 International Workshop on Junction Technology*, Jun. 2009, pp. 58–63, doi: 10.1109/IWJT.2009.5166220.

[21] G. Ghibaudo, M. Aouad, M. Casse, S. Martinie, T. Poiroux, and F. Balestra, "On the modelling of temperature dependence of subthreshold swing in MOSFETs down to cryogenic temperature," *Solid-State Electron.*, vol. 170, p. 107820, Aug. 2020, doi: 10.1016/j.sse.2020.107820.

[22] H. Bohuslavskyi *et al.*, "Cryogenic Subthreshold Swing Saturation in FD-SOI MOSFETs Described With Band Broadening," *IEEE Electron Device Lett.*, vol. 40, no. 5, pp. 784–787, May 2019, doi: 10.1109/LED.2019.2903111.

[23] Ghibaudo G., Roux O., Nguyen-Duc Ch., Balestra F., and Brini J., "Improved Analysis of Low Frequency Noise in Field-Effect MOS Transistors," *Phys. Status Solidi A*, vol. 124, no. 2, pp. 571–581, Feb. 2006, doi: 10.1002/pssa.2211240225.

[24] I. M. Hafez, G. Ghibaudo, and F. Balestra, "Flicker noise in metal-oxide-semiconductor transistors from liquid helium to room temperature," *J. Appl. Phys.*, vol. 66, no. 5, pp. 2211–2213, Sep. 1989, doi: 10.1063/1.344321.

[25] I. M. Hafez, G. Ghibaudo, and F. Balestra, "Assessment of interface state density in silicon metal-oxide-semiconductor transistors at room, liquid-nitrogen, and liquid-helium temperatures," *J. Appl. Phys.*, vol. 67, no. 4, pp. 1950–1952, Feb. 1990, doi: 10.1063/1.345572.

[26] L. L. Guevel *et al.*, "19.2 A 110mK 295µW 28nm FDSOI CMOS Quantum Integrated Circuit with a 2.8GHz Excitation and nA Current Sensing of an On-Chip Double Quantum Dot," in *2020 IEEE International Solid- State Circuits Conference - (ISSCC)*, Feb. 2020, pp. 306–308, doi: 10.1109/ISSCC19947.2020.9063090.