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CMOS Active Gate Driver for Closed-Loop dv/dt Control of GaN Transistors

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Abstract— This paper shows both theoretical and experimental analyses of a fully integrated CMOS active gate driver (AGD) developed to control the high dv/dt of GaN transistors for both 48 V and 400 V applications. To mitigate negative effects in the high-frequency spectrum emission, an original technique is proposed to reduce the dv/dt with lower switching losses compared to classical solutions. The AGD technique is based on a subnanosecond delay feedback loop, which reduces the gate current only during the dv/dt sequence of the switching transients. Hence, the dv/dt and di/dt can be actively controlled separately, and the trade-off between the dv/dt and E_{ON} switching energy is optimized. Since GaN transistors have typical voltage switching times on the order of a few nanoseconds, introducing a feedback loop from the high voltage drain to the gate terminal is quite challenging. In this article, we successfully demonstrate the active gate driving of GaN transistors for both 48 V and 400 V applications, with initial open-loop voltage switching times of 3 ns, due to a full CMOS integration. Other methods for dv/dt active control are further discussed. The limits of these methods are explained based on both experimental and simulation results. The AGD showed a clear reduction in the peak dv/dt from -175 V/ns to -120 V/ns for the 400 V application.

Index Terms— Active gate driver, dv/dt , EMI, electromagnetic interference, GaN, HEMT Transistors, wide-bandgap semiconductor, closed-loop systems, driver circuits, feedback circuits, switching circuits, power electronics.

I. INTRODUCTION

Wide-bandgap (WBG) power devices can be used in power converters to improve both their efficiency and power density. Power transistors that can handle high currents and high voltages based on GaN or SiC technologies are expected to represent a growing market in the coming years. Double-digit annual growth in sales and implementation of WBG power devices in the next five to ten years is expected [1]. A steady-growing market is also expected for aircraft applications [2], where higher DC bus voltages are being implemented and more electrical energy is being embedded to replace hydraulic and pneumatic systems in full electric solutions. However, for the same ON-state R_{DS_ON} resistance, WBG power devices have smaller C_{GD} parasitic capacitors compared to silicon IGBTs and MOSFETs, leading to faster switching speeds with higher dv/dt values. The difficulties in driving these new WBG transistors present several drawbacks for system designers and involve design trade-offs. For silicon carbide (SiC) technology, previous work [3]-[14] has presented different gate drivers to drive SiC transistors while adapting the previously developed techniques for silicon IGBTs or power MOSFETs. The main adaptations are for higher switching speeds, shorter delay times and switching times and specificities of SiC MOSFETs (e.g., driving voltages). In the context of lower voltages and higher frequencies, for GaN transistors, other solutions have been previously proposed [15], where the design can be optimized for reliability, EMI issues or performance.

Indeed, a high turn-on dv/dt value can induce currents by capacitive coupling (through the C_{GD} Miller capacitance) between the two transistors in a power commutation-cell, and crosstalk conduction can occur [3],[4]. This phenomenon is also described in the literature as cross conduction and extra-losses and possible failure in inverter-leg operation or synchronous buck can occur. This

problem is frequently observed with WBG devices because the threshold gate voltages and maximum gate voltage are lower than those in silicon. In addition, the threshold voltage for a SiC device decreases with temperature, which reduces its immunity, whereas some GaN devices are not affected by this property. Another disadvantage of high dv/dt is the use of volume-consuming EMI voltage common mode dv/dt filters [17]. For aircraft applications, the size and weight of such filters are key parameters for the system design [18]. Another disadvantage of high dv/dt values is a drain-source overvoltage during turn-off, mainly due to high related di/dt and the presence of parasitic inductors involved in the switching-loop. Finally, a fourth disadvantage is the high frequency induced common mode and differential mode current in the switching node [5]. Consequently, the common mode transient immunity (CMTI) of isolation barriers must comply with higher dv/dt values [19].

Among all the possible ways to control the dv/dt of a power transistor, several options emulate a C_{GD} external capacitance. In [20], a method using discrete transistors was proposed to actively drive silicon IGBT devices. In [21], a similar approach was adapted for GaN transistors, with discrete components. This solution has a lower bandwidth, and additional stray inductance between device's gate and source electrodes and therefore, cannot handle dv/dt 's in the order of 100's of V/ns. Moreover, in the topology proposed in [21], a higher delay is required for the biasing of the transistors involved in the feedback loop, limiting the capability to operate at higher dv/dt values. When increasing the dv/dt dynamic, the transient behavior of the feedback-loop becomes a key point to address. Indeed, one must avoid a prohibitive delay time to properly bias the several transistors involved in the feedback loop. With faster dv/dt values, it is also critical to limit the direct capacitor coupling between the drain and gate terminals of the power devices, to prevent detrimental effects through Miller coupling. Compared to [21], it is then desired to increase the feedback loop gain and to further reduce the value of the high voltage capacitor required for the active gate drive technique. Due to a smaller capacitor, its integration can also be possible. This paper proposes a novel method with a faster and simpler topology to control the turn-on transient based on a full monolithic CMOS gate driver offering very large bandwidth analog circuits. An improved solution, where all required devices are integrated into one ASIC, following the trend of integration [22]-[24], is presented, discussed and experimentally demonstrated.

II. ACTIVE GATE DRIVERS FOR SILICON AND WIDE BANDGAP POWER TRANSISTORS

The classical trade-off between dv/dt and the amount of switching energy (E_{ON}) is discussed in the following section. Then, the state-of-the-art for gate drivers with dv/dt control for power electronic applications is discussed. Our proposed method is then presented and compared to other approaches.

A. Proposed technique: turn-on control

The proposed active gate driver (AGD) technique is implemented only during turn-on. Indeed, the turn-off switching speed is mainly controlled by the load current amplitude and not directly by the gate driver when using high speed devices in high efficiency applications [25]. Nevertheless, our technique can be easily applied for the active control of the turn-off, should a hard turn-off be required by the application (the high dv/dt at turn off undergone at high load current can thus be limited by dynamically re-biasing the gate slightly higher than its threshold). The effects of temperature, load current and input voltage transients for the proposed technique are not discussed in this article. Without any active gate driving, a simplified expression for dv/dt during turn-on is introduced in (1). The derivative of the drain to source voltage (dv_{DS}/dt) depends on the gate current i_{GM} (gate current during the Miller plateau) and the gate to drain capacitance C_{GD} :

$$\frac{dv_{DS}}{dt} = -\frac{i_{GM}}{C_{GD}} = -\frac{v_{DRV}-v_M}{R_G C_{GD}} \quad (1)$$

where v_{DRV} is the gate driver supply voltage, v_{M} is the Miller plateau voltage (between external gate and source electrodes), and R_{G} is the external gate resistance, neglecting physical effects for simplicity.

The main idea of the active gate driving is to control dv/dt by emulating an increase in the Miller capacitance (or C_{GD} equivalent capacitance) of the power device only during the switching event and the dv/dt sequence. To do so, a current proportional to dv_{DS}/dt has to be subtracted from the gate current during the turn-on event. Hence, a feedback loop is used to generate this current, which is directly connected to the gate of the power device to reduce the gate current amplitude during the Miller plateau. This feedback method has been previously proposed but with key limitations:

--With discrete components, only low switching speeds can be actively driven (e.g., fall time of tens or hundreds of nanoseconds, as in [21]).

--With integrated solutions in CMOS gate drivers, only low-voltage applications are addressed, where the maximum drain to source voltage is lower than the CMOS technology limit (e.g., <48 V, as in [26]).

Fig. 1 shows a transistor-level diagram of the proposed method. A small value capacitor C_S is used as a sensor of the derivative of the voltage v_{DS} . A capacitor with a high breakdown voltage is required, since it has to sustain the high voltage of the DC bus. To amplify the current generated into this sensor during the dv/dt , a large bandwidth gain current mirror is proposed, which is the core idea for this method. The main challenge in this approach is to propose a circuit that can simultaneously supply a high amplitude feedback current with a very small time-delay response.

Typically, this feedback current i_{FB} may be higher than 1 A, and the delay in the feedback loop should be lower than 1 ns. This feedback current i_{FB} is proportional to the derivative of the power transistor voltage v_{DS} , current gain G and the value of the capacitor C_S acting as a dv/dt sensor (as shown in (2)). Typical C_S values are much lower than the GaN C_{RSS} , leading to C_S in the order of 0.7 pF to 2 pF. To reach these specifications, a CMOS integration with an optimal design is required.

$$i_{\text{FB}} = -G \cdot C_S \frac{dv_{\text{DS}}}{dt} \quad (2)$$

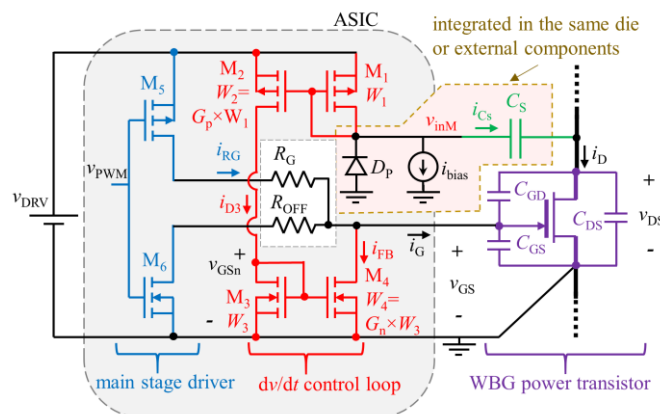


Fig. 1. Transistor-level schematic of the CMOS gate driver with a dv/dt feedback control loop for turn-on control.

Applying Kirchhoff's law at the gate node, the dv_{DS}/dt reduction is proportional to the feedback current i_{FB} . The following expression is obtained (valid as long as there is a current flowing through C_S with $i_{FB} < i_{RG}$ for stable operation, and a constant v_M voltage on the dv/dt sequence:

$$\frac{dv_{DS}}{dt} = -\frac{v_{DRV}-v_M}{R_G C_{GD}} + \frac{i_{FB}}{C_{GD}} = -\frac{v_{DRV}-v_M}{R_G (C_{GD}+GC_S)} \quad (3)$$

Note that the feedback circuit acts like an active equivalent gate-drain capacitor placed in parallel with C_{GD} equal to $G \cdot C_S$. Due to the feedback current amplification through current mirrors, the sense capacitor C_S can be downsized and further integrated on-

chip. The feedback loop is composed of four low-voltage transistors, M1 to M4, and a high-voltage sensing capacitor C_S . The current buffer, also called the main stage driver, is composed of a PMOS transistor M5 and a NMOS transistor M6 used to source and sink the high gate currents, respectively. This buffer has a split output architecture, making it possible to use different resistors to adjust the turn-on and turn-off switching losses separately. The capacitors C_{GD} , C_{GS} and C_{DS} are intrinsic to the GaN power transistor. The diode D_P is used only as a protection device at the input of the current mirror and is reverse biased during normal operation. In case the current in C_S is too high, the diode D_P will clamp the v_{inM} voltage at -0.7 V, preventing the gate voltage for M1 and M2 will exceed more than the nominal maximum voltage value (5.5 V), therefore preventing breakdown destructive voltage in transistors M1 and M2.

Fig. 2 introduces the waveforms for the main signals related to this approach that are used to actively control dv/dt . At the beginning of the dv/dt phase (at time t_2), a delay T_D is first required before the feedback loop starts to sink the current i_{FB} . This delay is mainly due to the settling time of the feedback loop circuit. The current i_{FB} quickly reaches its final value i_{FB_F} , which is subtracted from the current i_{RG} provided by the driver. When i_{FB_F} increases, the gate current i_G is decreased, leading to an increase in time t_3 in order to provide enough time to transfer the overall charge required by the gate of the power transistor during the Miller plateau. As a result, the dv_{DS}/dt is actively reduced. For the sake of simplicity, a constant Miller Plateau voltage was considered.

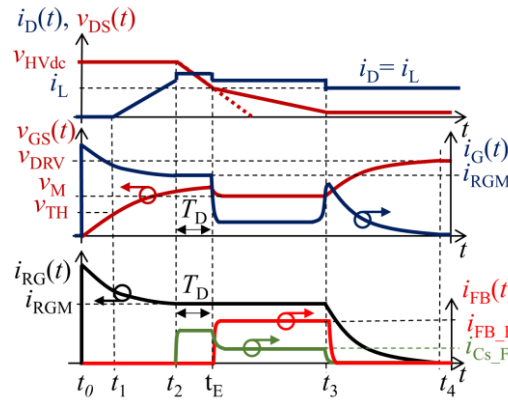


Fig. 2. Theoretical waveforms showing the influence of the feedback loop time delay T_D . i_{RGM} is the current provided by the driver to the power transistor during the dv/dt event.

During the turn-off transition, the sensing capacitor C_S sources (instead of sinking) a current that flows through the body diode of M1. The width of M1 (W1) has to be sized correctly to handle the C_S discharge current without breaking M1 or increasing the voltage at node v_{inM} too much.

It can be noted that if the total subtracted current i_{FB_F} increases too much, due to a high loop gain and overly fast feedback response, it can accidentally reach the value of the current supplied by the driver. In that case, the gate current i_G in the power device during the Miller plateau is cancelled. Then, the v_{DS} and v_{GS} voltages start to oscillate and the closed-loop system becomes unstable. A limit of the method comes from the maximum amount of time T_D required by the feedback current loop to operate. If this time delay is higher than the duration $t_3 - t_2$ observed in open-loop, the turn-on transition will be missed, and the feedback loop will have no effect on reducing dv/dt . It is important to ensure that the loop is able to operate as fast as possible. Finally, the time delay T_D characterizes the system performance both in terms of time response and stability. In our case, we will optimize the integration and circuit design to have less than 1 ns delay and to actively control initial fall time of 3 ns and above ($dv/dt_{peak} = -175$ V/ns in the case of 400 V applications).

B. Benefits of the Active Gate Driver

When designing a half bridge, there is a trade-off between the switching losses (E_{ON} , E_{OFF}) and switching speed (dv/dt , di/dt). As long as the Miller effect is an active phenomenon (all turn-on or some turn-off transients at high load current), dv/dt is typically limited by the choice of the gate resistor R_G . Fig. 3 introduces this classical trade-off (solid line) for the specifications detailed in the next sections (obtained with a Cadence™ simulation with a model of a GS66508T GaN device). This work proposes to reduce the dv/dt leading from the point A to the point C (dashed line) but with fewer switching losses compared to a simple change in the gate resistor value R_G (from point A to B). This change in the EMI-loss trade-off can be further dynamically tuned while changing the AGD parameters.

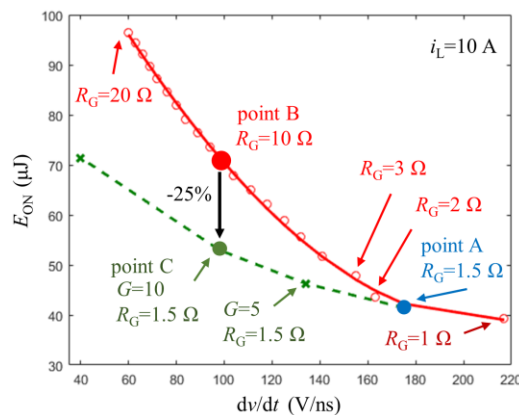


Fig. 3. Trade-off E_{ON} vs dv/dt as a function of R_G (solid line) or closed-loop gain G (dashed line) values for a constant bus voltage, load current and temperature. The proposed method aims to reach the point C without increasing the external gate resistor R_G .

The amount of saved energy during turn-on is explained in Fig. 4. The proposed method reduces the amount of switching losses because the dv/dt value is reduced without modifying di/dt . As a consequence, the dissipated switching energy during the di/dt event (hatched area in Fig. 4 (d)) is canceled with our technique. The proposed method will not change di/dt because the proposed feedback loop will not be active during this phase. First, the di/dt value can be set by adjusting the value of R_G , and then dv/dt can be separately adjusted to reduce the negative effects of the EMI. One has to note that the parasitic stray inductance is neglected in this section of the paper (to explain the method), which is reasonable for high-frequency applications of GaN power transistors with optimal PCB designs (e.g., power loop stray inductances in the range of 1 nH). As a positive consequence, both points B and C (Fig. 3) will also generate a lower drain current overshoot during the dv/dt sequence $[t_4, t_2]$ (Fig. 4) than point A; i.e., the dv/dt generates an extra transient current proportional to the parasitic drain-source capacitors of the power transistors.

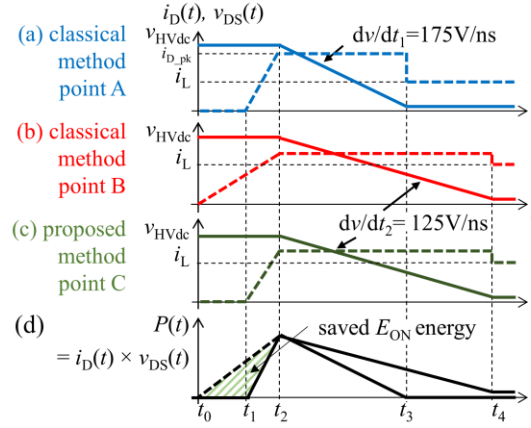


Fig. 4. Waveforms with different values of dv/dt and di/dt for the operating points A, B and C. The saved energy is due to the reduction of dv/dt without changing di/dt .

C. Summary/Benchmark

The proposed method has several advantages compared to other methods used to control dv/dt .

--Compared to an added constant external capacitor C_{GD} , the emulated capacitance $G \cdot C_s$ will not affect the device immunity through Miller coupling. The risk of a cross conduction fault is then mitigated. Another advantage is that the emulated capacitance can change through the feedback gain G . Moreover, the value of the required high-voltage C_s capacitor can be reduced using our technique; hence, its integration within the CMOS circuit is possible.

--Compared to open-loop techniques, the closed-loop method adapts the response for different systems and power devices under different conditions, while an open-loop approach would have to be designed for each different application and power device [27].

--Compared to other previously demonstrated closed-loop techniques, our approach is simple, extremely fast and highly integrated. While other closed-loop methods convert analog signals to digital signals using an ADC, their speed is limited to tens or hundreds of nanoseconds. Very high switching speeds and/or very short switching times cannot be controlled by the solutions presented today in the literature [10].

--Compared to other integrated solutions [28], [29], our solution offers both low (e.g., 48 V) and medium voltage (e.g., 400 V) applications, while using only low voltage CMOS devices and technology (e.g., 10 V, 20 V). Only a small (pF range) high-voltage sense capacitor is required, which is easily integrated with standard low-voltage CMOS technologies.

III. CMOS ULTRA-FAST ACTIVE GATE DRIVER

The best way to implement the proposed method is by the use of an integrated analog circuit designed to minimize the delay T_D of the feedback loop, while allowing high gain and large feedback currents.

A. Overall design approach and CMOS Active Gate Driver performance

As introduced in Fig. 1, two stages of current mirrors are cascaded. Therefore, the total response time is defined by several consecutive phenomena.

This time delay results from a succession of several events. During the turn-on of the power transistor and the dv/dt sequence, the voltage v_{DS} drops down from the voltage of the DC bus to a value close to zero. This transient is shown in Fig. 5(a). This signal, $v_{DS}(t)$, is the input signal of the feedback loop. Because the terminal v_{inM} of the sensing capacitor C_s is at a quasi-constant voltage with respect to the voltage range of v_{DS} , the derivative of $v_{DS}(t)$ will generate a proportional quasi-constant current flowing through

C_S , the $i_{C_S}(t)$ current, as shown on the second waveform Fig. 5(b). This current will charge the parasitic capacitor C_{GP} present on node v_{inM} , involving the gates of the PMOS transistors M1 and M2, and change the biasing-voltage of the first current mirror, as shown in Fig. 5(c). As soon as this voltage crosses the PMOS threshold voltage v_{Th_p} , a current will start to flow through the channel of M2, as shown in Fig. 5(d). This current charges the gates of the transistors M3 and M4, leading to an increase in the voltage $v_{GSn}(t)$, as shown in Fig. 5(e). Finally, when v_{GSn} reaches the NMOS threshold voltage v_{th_n} , the output current i_{FB} of the second current mirror starts to rise, as shown in Fig. 5(f). As soon as this current i_{FB} is no longer equal to zero, after time t_D , the feedback loop starts to operate and dv/dt is reduced and controlled.

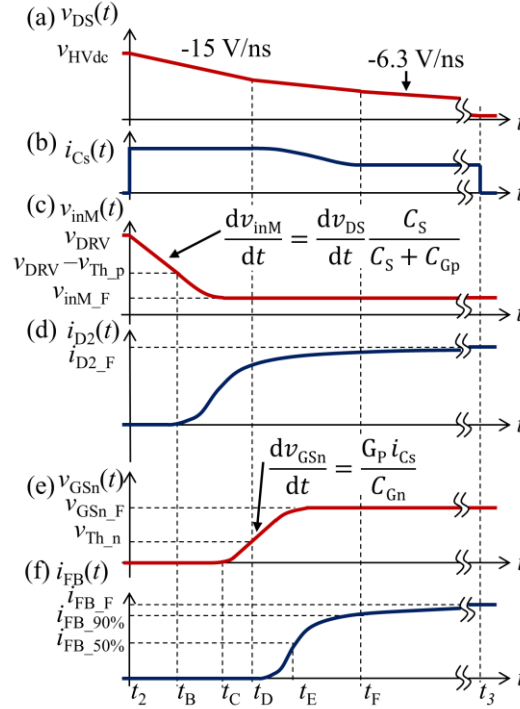


Fig. 5. Waveforms for the voltages and currents of the current mirrors between times t_2 and t_3 (where C_{GP} and C_{Gn} are respectively the total amount of parasitic capacitance viewed at the gate of M1 and M3). The feedback loop delay is detailed and expressed as $T_{D(50\%)} = t_E - t_2$.

In practice, the gain G of the feedback loop will vary according to the desired reduction in dv/dt . For instance, the higher the gain G is, the larger the i_{FB_F} is, leading to a reduced dv/dt during turn-on. One can also note that t_E will be larger when large gain values G are set. Since the current mirror is composed of two stages, the gain G is the product of the two intermediate gains of each stage (G_p and G_n in Fig. 1). Based on simulations in Cadence™ with the design kit provided by the CMOS foundry, total delay times $t_E - t_2$ in the range of 290 ps to 640 ps can be achieved (see Table II in [28] for more details). These values are functions of the gain G , which is proportional to the sizes of the current mirror transistors, with lower gains leading to shorter delay times.

Fig. 6(a) shows the dv_{DS}/dt reduction for the system operating at point A (open-loop) and C (closed-loop), as defined in Fig. 3 and 4. Fig. 6(b) shows the extension of the Miller plateau due to the added virtual capacitance effect and closed-loop control. Fig. 6(c) shows the gate current i_G that is going to the power device gate terminal, and Fig. 6(d) shows the drain current i_D of the power transistor and a beneficial reduction in overcurrent, while keeping the same initial di/dt .

A current biasing circuit is connected to the v_{inM} node. Compared to the i_{C_S} amplitude, a small current is sunk from this node that helps to precharge the intrinsic capacitances of the 4 transistors in the current mirrors, allowing a faster response. It should be noted that, in practice, both the feedback loop delay $T_{D(50\%)}$ and its bandwidth are affected both by the sizing of the several transistors involved in the current mirrors and the choice of the sensing capacitor C_S value. The final transistor sizes implemented

are the results of an optimization process involving both theoretical analysis and simulation validations using accurate CADENCE™ SPECTRE transistor models of the CMOS technology.

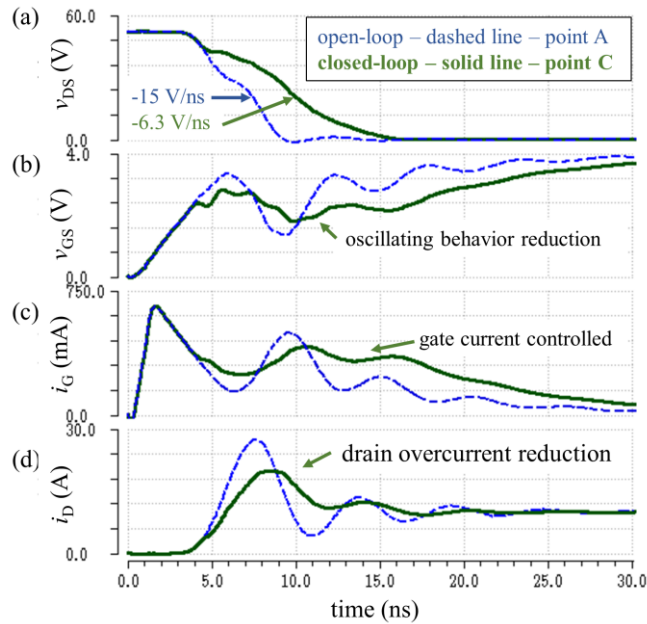


Fig. 6. Simulation waveforms for (a) v_{DS} , (b) v_{GS} , (c) i_G and (d) i_D with (case C) and without (case A) the proposed method, including estimated PCB parasitic elements; (d) also shows a beneficial effect of reduction in overcurrent (i_D) during turn-on that is also provided by the proposed method. Case study for the 48 V application.

TABLE I DIMENSIONING OF CMOS TRANSISTORS WIDTH		
Type	Key consideration to fix Width/Length	
M1	PMOS	W_1 fixed by minimum v_{inM} voltage at the highest $i_{CS} = C_s \cdot \text{Max}(dv_{DS}/dt)$, saturation regime
M2	PMOS	$W_2 = G_p \times W_1$
M3	NMOS	W_3 is fixed to obtain $v_{GSn} = v_{drv}/2$ for the highest i_{CS} , saturation regime
M4	NMOS	$W_4 = G_n \times W_3$, where $G = G_p \times G_n$
M5	PMOS	W_5 is fixed by the maximum source current for the GaN transistor, saturation regime
M6	NMOS	W_6 is fixed by the maximum sink current for the GaN transistor, saturation regime

*Note all PMOSs and NMOSs used have a v_{DSmax} and $v_{GSmax} = 5$ V and a length set to minimum.

The C_s sense capacitors are integrated with the CMOS AGD. Since C_s must have a breakdown voltage higher than the GaN power device, five different designs were considered that used different metal layers and inter layer dielectrics (Fig. 7). Integrated capacitance values of 0.7 pF, 1 pF and 1.5 pF have been implemented and tested. The breakdown characterization was performed under high vacuum, whereas the capacitance measurement was carried out with a HIOKI IM3570 using probe tips and calibration. As presented in Fig. 7, there is a common-mode parasitic capacitance between the LV node and the CMOS substrate that needs to be taken into consideration, which will add common mode current and a voltage divider effect to the sensing capacitor C_s .

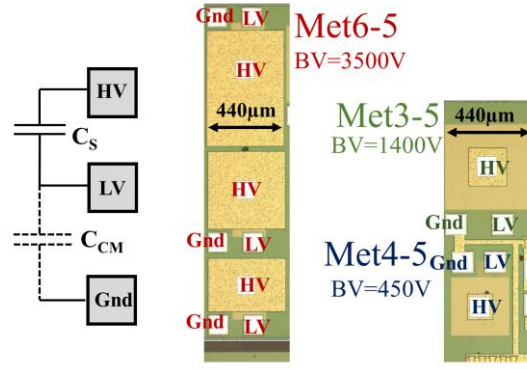


Fig. 7. Schematics and optical microscope pictures of the CMOS-integrated pF-range HV capacitors.

B. PCB Design

The analog circuits were implemented in 0.18 μm CMOS technology (AMS H18A6), and the fabricated test chip was packaged in a 6 mm \times 6 mm QFN with 24 pins. Two PCB versions (Fig. 8) were realized with layout considerations to minimize the parasitic inductances of both the power and control loops of the power transistor. The PCB uses 4 layers for the prototypes for the EPC2001C transistors and 6 layers for prototypes with GS66508T transistors. Two low-voltage decoupling capacitors with a capacitance of 1 μF are placed close to the gate driver to supply the peak current required during the switching transients, in addition to decoupling the capacitors integrated on-chip. The sensing capacitor C_s was integrated either on-chip or externally. Attention is made to minimize the PCB parasitic capacitance between drain and source of the power device.

A CMOS gate driver was implemented for the low-side power transistor, while the gate of the high-side transistor was shorted to its source. The output power load is an air inductor with a low parasitic capacitance.

Please notice that our AGD topology can be adapted to any WBG power transistor, but due to the limit of v_{DS} of integrated current mirror and main buffer MOSFETs (5.5 V), the built prototype is limited to driving transistors from 0 to 5 V.

Consequently, this PCB is only used for double pulse tests with our CMOS AGD driving EPC GaN HEMTs or GaN System devices, with the active control implemented at the low-side transistor. Neither the drain nor the gate currents are probed to comply with extremely low parasitics both for the power loop and the driving loop. The parameters are summarized in Table II. In the case of GaN System devices, the gate driver supply voltage is not optimal to achieve a low ON-state resistance after turn-on. This result occurs due to the 5 V CMOS transistors used for M1 to M6 (Fig. 1), which were chosen for the first CMOS AGD prototype. Nonetheless, it is possible to drive such GaN devices under these conditions and to achieve a high switching speed, as demonstrated hereinafter.

C. Impact of the proposed method on the total gate charge

The emulated gate-to-drain capacitor ($C_{GD} + G \cdot C_s$) leads to an extended Miller plateau, which will have an impact on the total amount of gate charge provided by the gate driver supply. Since charge is subtracted during a turn-on event through transistor M4, the amount of charge required to turn-on the power device will increase. Indeed, in the proposed improved gate driver circuit, the amount of charge subtracted by the current mirror has to be provided by the driver power supply v_{DRV} . This additional amount of gate driver energy E_{DRV_SUP} is given by:

$$E_{DRV_SUP} = v_{HVdc} \cdot G \cdot C_s \cdot v_{DRV} \quad (4)$$

Eq. (4) shows that the extra energy supplied by the driver will increase proportionally to the gain of the internal current feedback circuit G . A decrease of 58% (from -15 V/ns to -6.3 V/ns) in dv_{DS}/dt will produce an increase of 58% in the energy provided by

the driver $E_{\text{DRV_SUP}}$. Since the switching energy of the power device is considerably higher than the energy required by the driver, this increase in driver energy has a limited impact. For the 400 V application, the gate charge is increased by 44% from point A to B. One can note that this additional gate driver energy is inherent to the proposed close-loop control, and other previously demonstrated approaches are subject to such an energy increase [20], [21].

TABLE II
TEST BENCH AND MEASUREMENT SETUP FOR EPC2001C AND FOR GS66508T

Name	Parameter	
DC bus voltage	50 V	400 V
Power transistor	EPC2001C 100 V 36 A 7 m Ω	GS66508T 650 V 30 A 50 m Ω
C_{RSS}	20 pF (datasheet max value)	2 pF-60 pF
V_{DRV}	4 V	3 V
C_{S} sensing capacitor	2 pF ceramic external capacitor MC0805N2R0C500CT	1 pF ceramic external (MC0805N1R0C501CT) or integrated (Met6-5) capacitors
R_{G} (ON)	4.4 Ω	1.5 Ω
Load inductor	$L=270 \mu\text{F}$ $C_{\text{p}}=160 \text{ pF}$ 150 A	$L=270 \mu\text{F}$ $C_{\text{p}}=160 \text{ pF}$ 150 A
T_{A}	22°C	22°C
Oscilloscope	Tektronix DPO4054 500 MHz	Tektronix DPO4054 500 MHz
Probes	P6139B 500 MHz	LeCroy PPE 2 kV 400 MHz
i_{L}	1.3 A	2.5 A

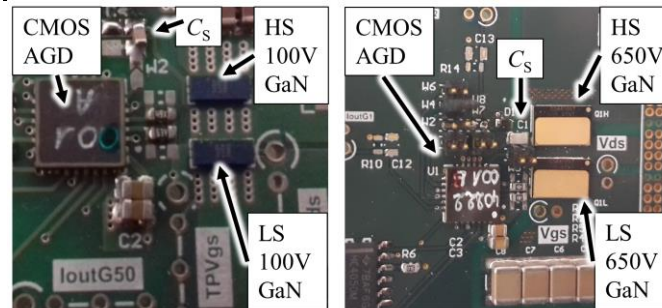


Fig. 8. Prototypes for a double-pulse test-bench with the proposed dv/dt control circuit.

D. Application to a 100 V GaN power commutation cell

Using the fabricated CMOS AGD with the integrated buffer, Fig. 9 shows experimental waveforms obtained during the turn-on with and without the closed-loop control, with the same gate resistor and driving voltages for the same test parameters as previously described in Table II. For the closed-loop, a prebiasing current of 20 μA was applied at the input of the current mirror (v_{inM} node) using a sourcemeter unit Keithley 2612B. Without the closed-loop control, the fall time is 4.36 ns (90%-10% $v_{\text{DS}}(t)$), with a peak dv/dt of -15 V/ns. Even with this fast switching event, the AGD is able to actively control the dv/dt sequence from the beginning, without modifying di/dt . It is possible to see the di/dt sequence in the v_{GS} signals because it is the interval between v_{TH} (around 1.7 V from the datasheet) and the beginning of the dv/dt phase, the second line marked in Fig. 9. The i_{L} is not measured in our circuit to reduce the power loop inductance. However, the $v_{\text{GS}}(t)$ signal with and without the closed-loop control clearly shows that the di/dt sequence remains almost identical in both cases (Fig. 9 and Fig 10 marked as di/dt sequence). One can also note that the

reduced dv/dt with the closed-loop feedback allows the reduction of the drain current overshoot and subsequent gate overvoltage before the Miller plateau. Due to the AGD, the fall time is increased from 4.36 ns to 7.37 ns (90%-10% v_{DS}) without affecting the gate charge before the Miller plateau. This increase in fall time corresponds to the reduction in peak dv_{DS}/dt from -15 V/ns to -6.3 V/ns as shown in Fig. 7. One must note that all the analog circuits are integrated within the CMOS AGD; only the driver supply decoupling capacitors, HV-sensing capacitor (for some tests) and gate resistors are external devices. It should also be emphasized that due to the high speed and large gain of the integrated current mirrors, the HV-sensing capacitor C_S is designed in the pF range, allowing its further integration within the CMOS chip (please see table II for values).

Fig. 10 shows the measured v_{GS} waveforms in open-loop and in closed-loop with gains of 10 and 50 for the same value of sensing capacitor $C_S = 2$ pF (external). The duration of the Miller plateau is successfully increased with higher feedback gain values (“effect 1” in Fig. 10). It is also clear that the di_D/dt phase is not affected by the closed-loop control. The di/dt value is estimated to be approximately 1A/ns, since the v_{GS} signal changes from v_{TH} to v_M in approximately 1 ns. Please note that measurements are carried out with $i_L=2$ A to obtain higher values of dv/dt to explore the speed limits of the method. In addition to the reduction of the dv_{DS}/dt with higher closed-loop gains, the drain overcurrent during turn-on is also reduced. This effect can be seen in Fig. 10 (“effect 2”) where $i_D(t)$ and $v_{GS}(t)$ are linked by the transconductance of the GaN transistor in this operation state. Reducing the drain overcurrent and gate overvoltage before the Miller plateau is a clear proof of the ultrafast closed-loop control. Due to the AGD, the classical design trade-offs in operating conditions and reliability issues are clearly pushed forward.

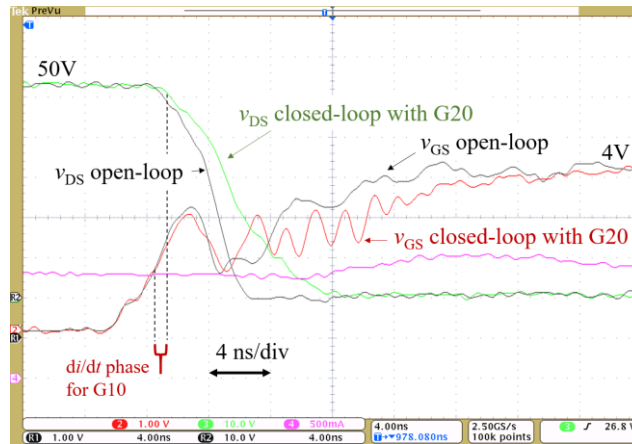


Fig. 9. Measured $v_{DS}(t)$ and $v_{GS}(t)$ waveforms for open-loop (without the proposed method) and closed-loop (with the proposed method) controls.

To compare the implementation of the AGD with a gain of 50, Fig. 11 shows a comparison between the experimental results and simulated waveforms. Increasing the feedback gain of the current mirrors decreases dv_{DS}/dt while maintaining an identical di/dt sequence.

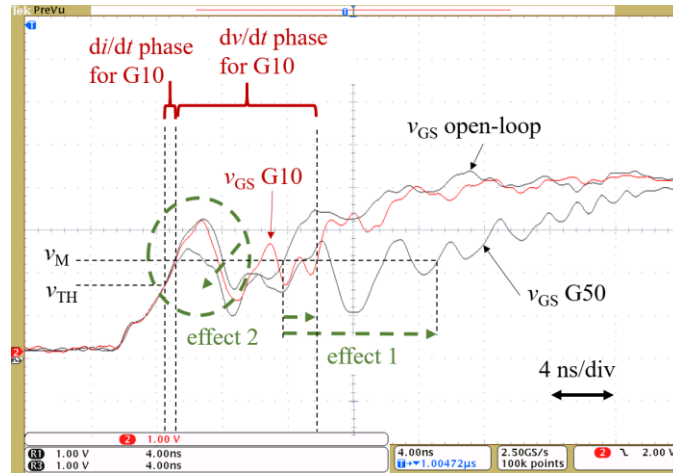


Fig. 10. Measured $v_{GS}(t)$ for open-loop (without the proposed method) and closed-loop controls with mirror gains equal to 10 and 50.

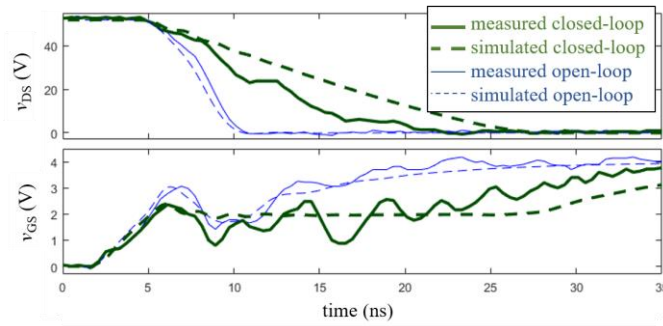


Fig. 11. Measured and simulated waveforms $v_{DS}(t)$ and $v_{GS}(t)$ for open-loop and closed-loop controls using a current mirror with gain of $G=50$. A prebiasing current of 150 μA is used in this measurement.

E. Application to a 650 V GaN power commutation cell

Fig. 12 shows the implementation of our technique with a GaN System transistor GS66508T for gain $G=10$ and $C_S=1$ pF. The fall time during turn-on (v_{DS} , 90% to 10%) is increased from 3.3 ns (open-loop) to 8 ns (closed-loop). The peak dv/dt value of -175 V/ns is therefore reduced to -120 V/ns with our CMOS AGD. A biasing current of 320 μA is applied, and one can observe that dv/dt starts to be attenuated in less than 1 ns. All the parameters for the results are described in Table II. Without an integrated analog feedback loop, such a result would not be possible. This experimental result shows, for the first time, the active control of 650 V GaN devices with extremely high switching speeds, both in open- and closed-loops. Fig. 13 shows a similar result, where the high-voltage capacitor is integrated on the same CMOS chip as the gate driver (1 pF, 3.5 kV breakdown, see section IV). The small differences in switching speeds between Fig. 12 and Fig. 13. can be explained by the use of a different PCB board, albeit from the same design (typical dispersion in power devices, CMOS gate driver and PCB parasitics). Nonetheless, this result clearly shows that the AGD can be fully functional, even with the high-voltage sense capacitor C_S monolithically integrated within the CMOS AGD.

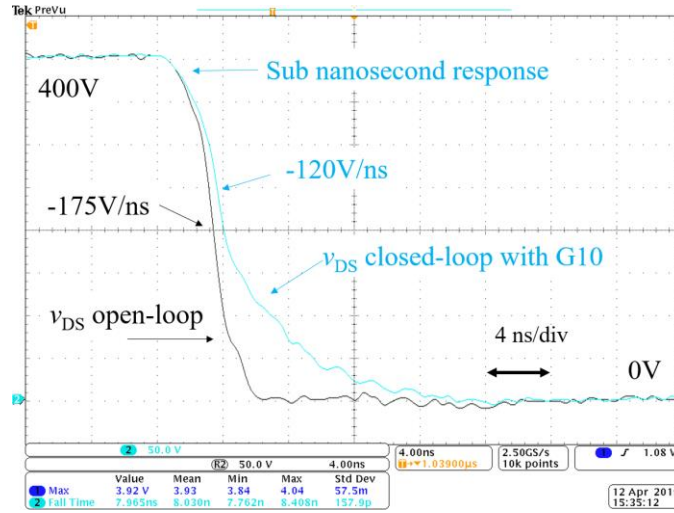


Fig. 12. Measured $v_{DS}(t)$ waveforms for open-loop (without the proposed method) and closed-loop (with the proposed method) controls for 650 V GS66508T GaN transistors. $i_{bias}=320 \mu A$.

Please note that the effect of a biasing current improving the feedback response time can be seen comparing Fig. 12 ($i_{bias}=320 \mu A$) and Fig. 13 without biasing current. The attenuation in dv/dt occurs latter in Fig. 13 compared to Fig. 12, as predicted and discussed before.

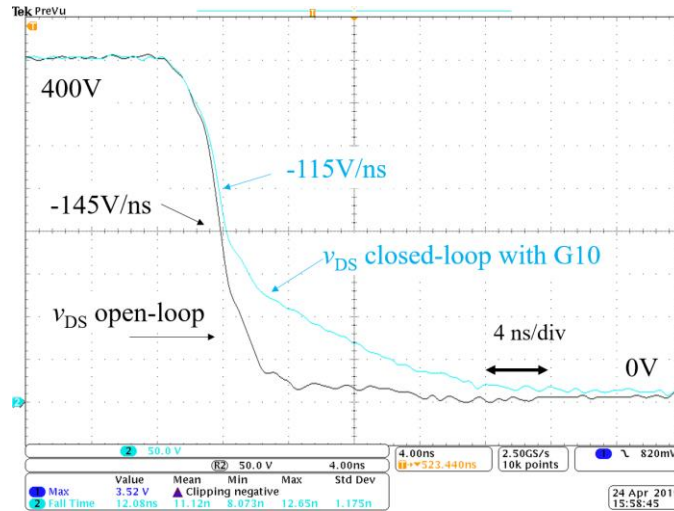


Fig. 13. Measured $v_{DS}(t)$ waveforms with an embedded sensing capacitor C_S and without an i_{bias} current for this measurement.

F. Benefits for the E_{ON} vs. dv/dt trade-off

Table III shows the simulated values in Cadence™ related to the points presented in Fig. 3 and Table II according to the experimental results obtained with the closed-loop systems. E_{ON} is calculated by simulations using the SPICE-compatible model of the transistor provided by the manufacturer for each GaN power device. Comparing points A, B and C, the maximum value of dv_{DS}/dt was reduced by 61% with our technique, while increasing E_{ON} by only 46% (point C, closed-loop), whereas it would have increased by 100% with a larger gate resistor (point B) for the same dv_{DS}/dt . This balance sheet must be further confirmed by E_{ON} measurements in our prototype. In this work, the drain current of the GaN transistor was not measured, as it would have increased the power loop parasitic inductance and therefore limited our capability to show a very fast active gate control.

G. Effect of the closed-loop control in the frequency domain

The experimental data for $v_{DS}(t)$ for the turn-on, turn-off, ON and OFF-states measured with the double pulse method are merged into a periodic signal, with a 1 MHz switching frequency and a duty cycle of 0.5. The Fourier transform of such a $v_{DS}(t)$ signal is shown in Fig. 14 and Fig. 15 for 48 V and 400 V applications, respectively, for both the open-loop and closed-loop controls. An analytical expression for the expected attenuation $K_{dB(G20)}$ at high frequency is provided by (5). Consequently, for the reduction in the peak dv/dt during turn-on with the closed-loop control, the v_{DS} spectrum is reduced at high frequency, e.g., 13 dB μ V lower at 100 MHz (48 V application, Fig. 14) or 7.6 dB μ V at 100 MHz (400 V application, Fig. 15). This is a clear advantage of the AGD for reducing the high-frequency voltage content of the switching nodes with fewer switching losses compared to a classical adjustment of the gate resistor.

$$K_{dB(G20)} = 40 \log \left(\frac{dv/dt_{(G20)}}{dv/dt_{(OL)}} \right) \quad (5)$$

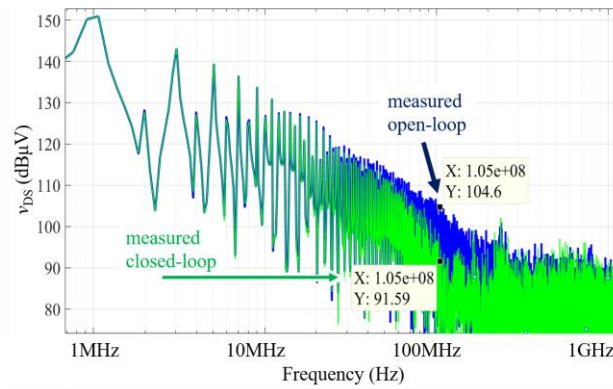


Fig. 14. v_{DS} spectrum with open and closed-loop during turn-on calculated from data measured for the EPC transistor with all the parameters in Table II.

IV. CONCLUSION

While the typical fall times for GaN HEMTs are as low as a few nanoseconds in 48 V and 400 V applications, it is quite challenging to achieve a closed-loop feedback from the high-

TABLE III
SIMULATED E_{ON} IN OPEN AND CLOSED-LOOP
FOR TWO DIFFERENT GAN VOLTAGE-RANGE APPLICATIONS

$i_L=1$ A						
	100 V GaN EPC2001C tests at 50 V $G \times C_s=20$ pF			650 V GaN GS66508 tests at 400 V $G \times C_s=20$ pF		
Point*	R_G (Ω)	E_{ON} (μ J)	$ dv/dt $ (V/ns)	R_G (Ω)	E_{ON} (μ J)	$ dv/dt $ (V/ns)
A	4.4	1.42	15	1.5	18.18	175
B	22	1.845 (+30%)	4.715 (-68%)	10	19.62 (+7.9%)	97 (-44%)
C	4.4	1.62 (+16.1%)	4.67 (-68%)	1.5	18.81 (+3.4%)	97 (-44%)
$i_L=20$ A						
Point*	R_G (Ω)	E_{ON} (μ J)	$ dv/dt $ (V/ns)	R_G (Ω)	E_{ON} (μ J)	$ dv/dt $ (V/ns)
A	4.4	5.488	14	1.5	60.88	119
B	16.6	12.42 (+126%)	5.189(-63%)	13	122.2(+100%)	46 (-61%)
C	4.4	11.51 (+110%)	5.163(-63%)	1.5	89.14(+46%)	46 (-61%)

*Similar points as defined in Fig. 3 and Fig. 4 for peak dv/dt values.

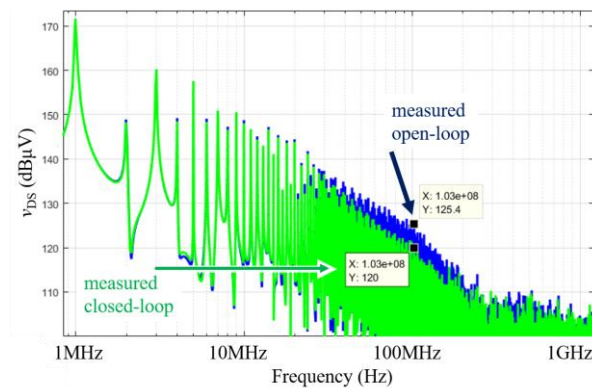


Fig. 15. v_{DS} spectrum with open and closed-loop during turn-on calculated from data measured for the GaN Systems 650 V transistor with all the parameters in Table II.

voltage drain to the low-voltage gate node. In this context, an ultrafast method to actively control the dv/dt rate of the GaN HEMT drain-source voltage during turn-on is proposed and experimentally demonstrated. The key challenges are to achieve a subnanosecond delay for the feedback loop and to integrate all active and passive devices within a CMOS gate driver. Here, a CMOS AGD was designed, characterized and further implemented with 100 V and 650 V GaN transistors.

The CMOS AGD is based on a standard low-voltage CMOS technology. Due to the AGD, the dv/dt sequence can be actively tuned, without modifying the di/dt sequence. The Miller plateau is then extended, with benefits on reliability consideration with a lower capacitive drain overcurrent and gate overvoltage during the active gate driving. Compared to classical methods (e.g., fixed or variable gate resistors), switching losses are reduced for the same level of dv/dt reduction. The AGD showed a clear reduction in the peak dv/dt in 400 V and 48 V applications from -175 V/ns to -120 V/ns and from -15 V/ns to -6.3 V/ns, respectively.

To achieve this active control with extremely fast GaN devices, the response time of the feedback loop ranges between 290 ps and 640 ps (gain and bias dependent). Since the technique used here is based on the use of active devices, the feedback gain can be further adapted to comply with system-level considerations (e.g., best trade-off between switching losses vs. EMI). As a future work, EMI radiative measurements will be considered to confirm the benefits of the AGD.

V. APPENDIX

Fig. 16 and Fig 17 shows that the system proposed in this paper will not affect the turn-off behavior because the discharge current of C_S will pass through the body diode of M1. Fig. 18 shows the feedback loop delay measured by connecting the current mirror input to the drain of the power device (for normal operation) and its output to a 14.7 Ω resistor to v_{DRV} . The potential at the output of the current mirror (M4 Drain potential) is referred to as v_{out_M} in the figure.

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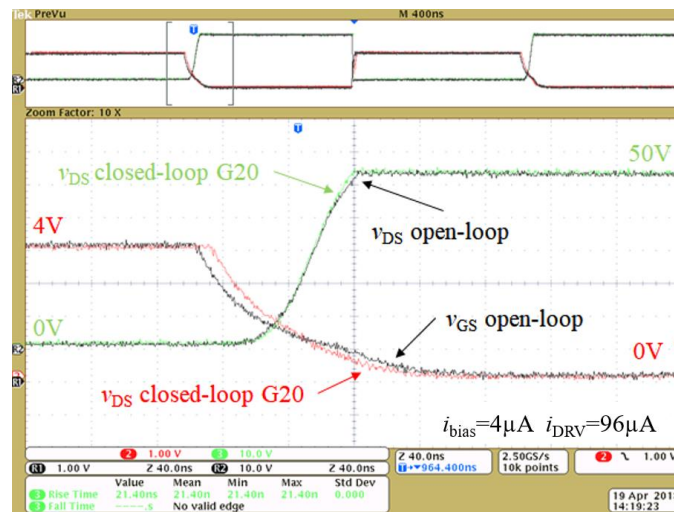


Fig. 16. Measured $v_{DS}(t)$ and $v_{GS}(t)$ waveforms for open-loop (without the proposed method) and closed-loop (with the proposed method) for a turn-off event (case EPC2001C $v_{HVdc} = 50$ V).

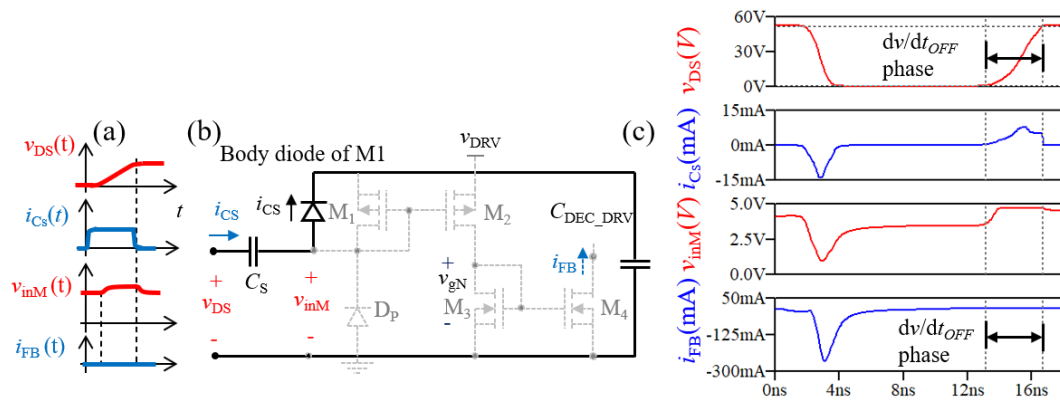


Fig. 17. The behavior of the system during the turn-off event. (a) Theoretical waveforms during turn-off, (b) the discharge path of C_S capacitor during turn-off event and (c) simulation showing the feedback system will not source a current (i_{FB}) during a turn-off event.

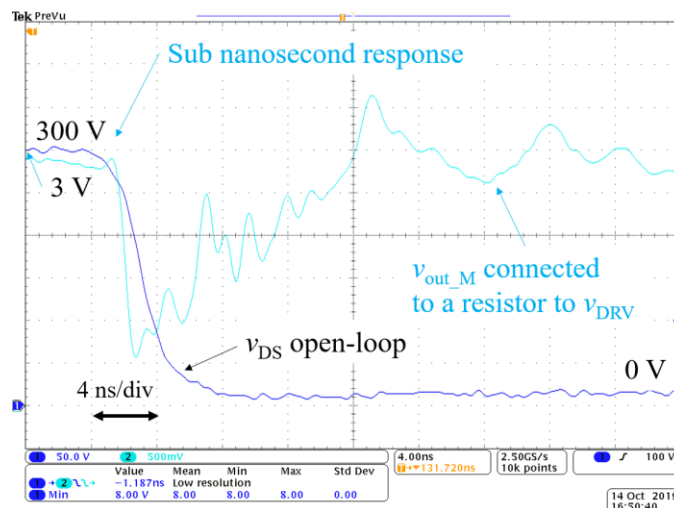


Fig. 18. Measurement of the feedback loop delay (T_D) for a current mirror with a gain of 10 and without a biasing current (i_{bias}) (case GS66508T $v_{HVdc} = 300$ V).

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