Fast-Convergence Self-Adjusting SECE Circuit With Tunable Short-Circuit Duration Exhibiting 368% Bandwidth Improvement

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A. Morel, *Member, IEEE*, A. Quelen, C.A. Berlitz, D. Gibus, P. Gasnier, A. Badel and G. Pillonnet, Senior *Member, IEEE*

***Abstract*— The harvesting frequency bandwidth (HBW) of a resonant-based electromechanical harvester is inherently limited by its quality factor. Electrical tuning of the resonant frequency leveraged by a significant electromechanical coupling is a promising approach to enhance the HBW and paves the way toward industrialization of robust vibration energy harvesting system. However, it remains challenging to design a self-powered harvesting IC that includes self-tuning capabilities, especially at low vibration amplitude. This paper describes the shorted synchronous electrical charge extraction (SSECE) strategy and proposes a dedicated self-powered integrated circuit including power stage, sensors to sequence the harvesting phases and power sensing. An on-chip tracker dynamically maximizes the harvesting power when the piezoelectric-based harvester characteristics or excitation frequency shifts. The experimental results show a 368% HBW enlargement with the highest convergence FoM (0.213) and the lowest power-peak frequency compared to prior art.**

Index Terms—*Frequency tuning, Piezoelectricity, Self-tuning, Synchronous harvesting strategy, Vibrations energy harvesting.*

I. Introduction

Energy scavenging has been widely investigated during the last decades to extend the lifetime of electronics devices, initially limited by the energy storage. Harvesting vibrations is particularly interesting in closed and confined environment, when the scavenger is located close to vibration sources e.g. motors and machine tools. Piezoelectric energy harvesters (PEH) exhibit good capabilities to transduce a mechanical stress to electrical charges in cm^2-scale footprint over large temperature ranges with reasonable material cost.

During the last two decades, researchers have proposed linear and synchronous harvesting strategies to efficiently extract the energy from PEH. Synchronous Electrical Charge Extraction (SECE) and Synchronized Switch Harvesting on Inductance (SSHI) received a great interest from the integrated circuit community since their extraction efficiencies largely outperform the full-bridge rectifier (FBR) interface. However, FBR, SECE and SSHI suffer from similar narrow harvesting bandwidth (HBW) e.g. below a few percents of the resonant frequency. In others words, the harvested power drastically decreases if the vibration frequency and the PEH resonant frequency are not aligned. In most applications, the ambient vibration and PEH resonant frequencies may not be equal due to aging, temperature variations, or due to non-constant frequency sources. This non-robustness of piezoelectric resonant-based energy harvesters constitutes a major obstacle toward massive spreading into industrial applications. To overcome the currently limited HBW, frequency-tuning strategies have been proposed to electrically adjust the resonant frequency of the harvester [1]. These strategies are based on the emulation of electrically-induced damping and mass by the harvesting interface leveraged by the harvester electromechanical coupling and quality factor.

Based on SECE, the phase-shifted SECE (PSECE) adjusts the phase-shift of the energy extraction event in order to tune the harvester dynamics [2]. The frequency tuning synchronous electrical charge extraction (FTSECE) adjusts two parameters (the voltage inversion ratio and energy extraction phase-shift) to maximize the HBW [1]. Based on parallel SSHI (PSSHI), the delayed PSSHI adjusts the phase of the charges' inversion to improve the extraction efficiency on a larger frequency range than standard PSSHI [3]. Our group has proposed the phase-shifted short-circuit SECE, a two-parameter strategy consisting in PSECE with an additional short-circuit phase of tunable duration [4]. Prior publications describe only two integrated-circuit interfaces [1,2] that embed the aforementioned tunable strategies along with self-tunability capabilities. In [1], the maximum power point tracking (MPPT) of a FTSECE is controlled by five parameters couples stored in a pre-programmed look-up table. To become robust to the harvester drifts while removing any pre-calibration, our group has already developed a MPPT to dynamically adapt the PSECE strategy [2].

In this letter, we propose a self-adjusted shorted SECE (SSECE) strategy implemented with an integrated circuit fabricated in 0.6μm CMOS technology. This new strategy is a single-parameter variant of the double-parameter strategy introduced in [4], with a phase-shift fixed to 0°. Hence, the SSECE relies on the tuning of the short-circuit (SC) duration to enlarge the HBW of a PEH. Implemented in the same silicon as [2] (with a few shared functions), the circuit introduced in the present letter dynamically adjusts the SC duration thanks to a tunable time-reference along with a sub-μW perturb and observe (P&O) MPPT algorithm. Thanks to this tunable SC, the IC achieves up-to 368% increased bandwidth with improved performances in the [51Hz, 56Hz] range compared to [2]. Finally, the convergence time is 10.7 seconds faster than in [2], leading to a convergence FoM 5 times greater.

II. Shorted-SECE IC interface

The proposed IC harvesting interface based on SSECE strategy is depicted in Fig. 1. An on-chip negative voltage converter (NVC) made of four cross-connected mosfets rectifies the v_p AC signal provided by the PEH under vibration stimuli. The transistors M_1, M_2 and M_3 ensure the classical SECE energy extraction sequencing, while an extra transistor M_0 is added to allow the tuning of the SC duration. The parameter $\Delta\phi$ is adjusted to adapt

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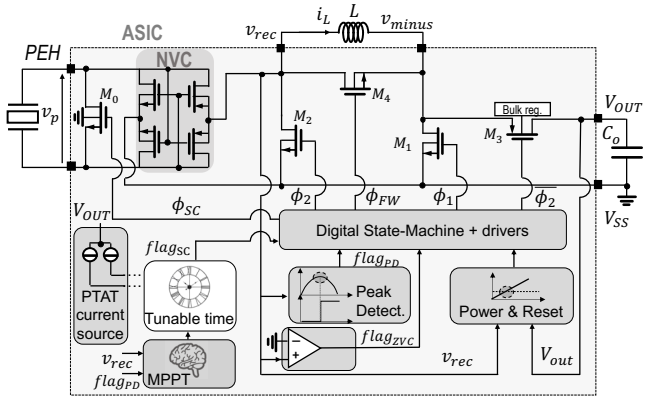

Fig. 1. Proposed IC based on SSECE including the power path, drivers, power sensing, phase detections and perturb & observe MPPT algorithm on a single CMOS chip.

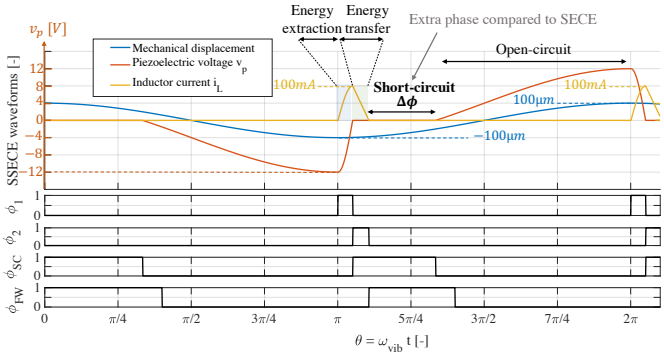

Fig. 2. Proposed SSECE waveforms with the associated MOS control signals.

the resonant frequency of the harvesting system to the vibration frequency. The cold-start circuit is included on-chip but not shown in Fig.1 for the sake of clarity.

By using sensors and a sequential logic circuit, the IC schedules four distinct phases (energy extraction, energy transfer, short circuit and open-circuit, shown in Fig. 2) to efficiently extract the energy from the PEH under a larger HBW than non-tunable SECE. Compared to the standard SECE, the proposed SSECE includes an extra short-circuit time whose duration has a direct impact on both the electrically-induced damping and resonant frequency [4].

The four SSECE phases are described next. First, the PEH is short-circuited by M_0: v_p remains equal to 0V during this SC phase. After a tunable SC duration $\Delta\phi$, the system enters into the open-circuit phase: all transistors are non-conducting and electrical charges are accumulating in the piezoelectric material, hence v_p is increasing. When the rectified piezoelectric voltage v_{rec} reaches an extremum, sensed by the peak detection block, the system moves to the energy extraction phase. Consequently, M_1 is conducting which electrically connects the off-chip inductor L to the PEH. Because of the LC loop formed between this inductance and the piezoelectric material intrinsic capacitance, the energy is quickly transferred from the PEH to the inductor. v_{rec} quickly decreases and the current in the inductor i_L increases. A voltage comparator used in its zero-voltage crossing (ZVC) configuration senses the instant v_{rec} reaches zero, meaning that all the energy has been transferred from the PEH to the inductor. Thereafter, the system turns into the energy transfer phase: the inductor is now connected to the external storage capacitor C_o through M_2 and M_3. The current in the inductor decreases as the energy is transferred from L to C_o. When i_L crosses zero, meaning the inductor has transferred all its energy to the storage capacitor, the system goes back to the first phase (SC). This transition is sensed by the same comparator used in its zero-current crossing (ZCC) configuration. M_4 is turned on in order to evacuate any remaining current in the inductor.

III. Voltage Comparator with Two Functions (ZVC/ZCC)

The transistor-level schematic of the comparator is shown in Fig.3. It consists in a two-stage comparator with a hysteresis control used to switch between its ZVC and ZCC modes. First, during energy extraction, the comparator works in its ZVC configuration. The two resistances of the first stage are asymmetric (R=30kΩ) in order to generate a -40mV offset. As soon as v_{rec} goes under this threshold value, the comparator output, $flag_{ZVC}$, is set high, which symmetrizes the two resistances of the first amplification stage, nullifying the offset. Concurrently, the system turns into the energy transfer phase. As i_L starts to decrease, the rectified piezoelectric voltage v_{rec}, fixed by the inductor current flowing through the on-state resistance of M_2, grows from a negative value to 0V. Therefore, by sensing the instant v_{rec} crosses 0V, the comparator senses the instant the current crosses 0A. The bias current I (100nA) shown in Fig.3 comes from a PTAT current source (shown in Fig. 1) and is copied multiple times inside the comparator thanks to current mirrors. The high voltages MOS M_{11} and M_{16} are used to inject an additional current to the first and second amplification stage when the rectified piezoelectric voltage gets close to 0V. This helps increasing the precision of the comparator when needed while keeping its overall consumption low. Thanks to this technique, and because the comparator is turned off most of the time (approximately 0.3% of the vibration's semi-period), its power consumption remains lower than 50nW.

IV. Short-Circuit Angle Tuning

A. Tunable short-circuit duration

As shown in Fig.4, the tunable short-circuit duration generated by a digitally adjustable 8-bits bus called $\Delta\phi_{ctrl}$. When the system enters in the SC phase, a 15kHz oscillator starts oscillating and sequences an 8-bits counter. When the output bus of the counter becomes equal to $\Delta\phi_{ctrl}$, $flag_{SC}$ signal ends the SC phase. In the IC, the duration of the short-circuit phase is always between 0s ($\Delta\phi_{ctrl}$ = 0) and 2.55ms, which is enough to emulate a 0° to 180° SC angular duration for vibration frequencies greater than 29Hz. The oscillator is composed of a current-controlled ring oscillator (RO). The 20nA currents come from the PTAT current source shown in Fig.1. In order to set the oscillation frequency to 15kHz, we connected three on-chip 450fF capacitors to the drains of M_{31}, M_{32}, and M_{33}. This current-controlled structure avoids any cross-conduction in the RO inverters over the operating supply voltage range (up to 5V). The sawtooth wave (with 1.8-2V amplitude) produced by the ring oscillator is transformed into a square wave thanks to two inverters gates. These inverters are supplied by the peak value of the drain voltage seen by the current-controlled RO transistors thanks to a 2.4pF decoupling capacitance. Finally, a level-shifter translates the low amplitude generated by the RO to the supply voltage rails. The overall power consumption of this circuit lies around 80nW (V_{OUT}=3V, $\Delta\phi$=45°).

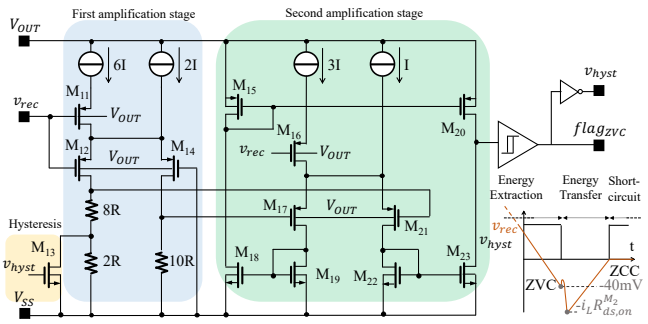

Fig. 3. Voltage comparator schematic working in two configurations: Zero Voltage Crossing (ZVC) and Zero Current Crossing (ZCC).

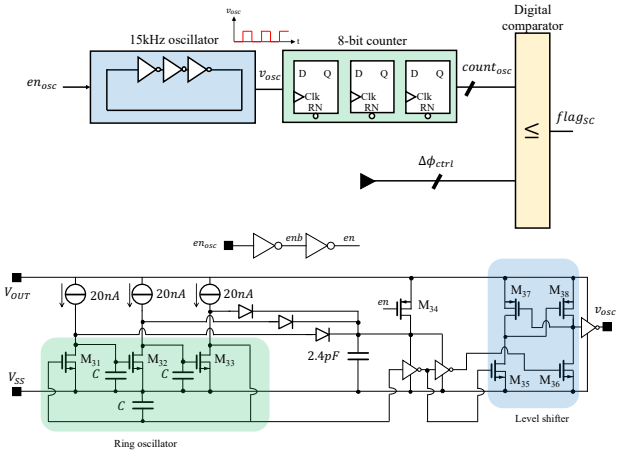

Fig. 4. Schematic of the tunable short-circuit duration.

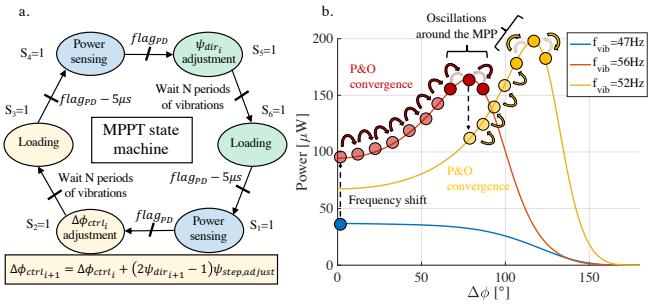

Fig. 5. a. State-machine of the proposed P&O algorithm and b. simulated trajectory of the Δϕ convergence with the P&O algorithm.

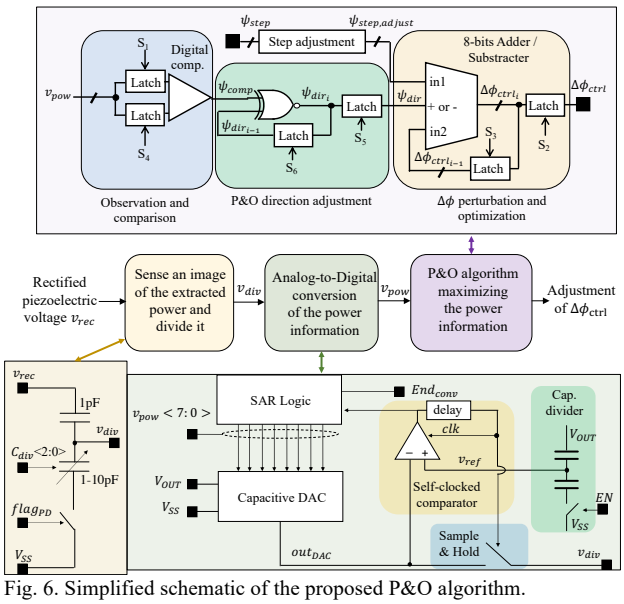

Fig. 6. Simplified schematic of the proposed P&O algorithm.

B. *On-chip perturb and observe algorithm*

In order to dynamically adjust the value of the short-circuit phase $\Delta\phi_{ctrl}$ without any calibration, an on-chip perturb and observe algorithm has been integrated (Fig.5.a) as previously presented in [2]. In a first state (S_1), the algorithm senses the extracted power $P_{PEH}(i)$, digitalizes the power information. Thereafter, in S_2, the algorithm perturbs the harvesting system by increasing or decreasing the short-circuit duration $\Delta\phi$. The system keeps working with this new $\Delta\phi$ during the next N periods of vibrations. In S_4, the algorithm senses the new value of the extracted power $P_{PEH}(i+1)$, and compares it to the previous power acquisition $P_{PEH}(i)$. If the new value is greater than the previous one, the algorithm does not change the direction of the perturbation ($\psi_{dir,i} = \psi_{dir,i-1}$) and will keep on increasing (or decreasing) the short-circuit duration the next time it enters in state S_2. In the one hand, if $P_{PEH}(i+1) < P_{PEH}(i)$, the sign of the perturbation is changed. In this case, the algorithm will start decreasing (or increasing) the short-circuit duration the next time it enters in state S_2.

As shown in Fig.6, the algorithm senses the peak value of the piezoelectric voltage $v_{rec,peak}$ at the end of the open-circuit phase. Indeed, maximizing $v_{rec,peak}$ is the same as maximizing the extracted power, since the extracted power is proportional to the squared peak piezoelectric voltage [4]. To match the operating voltage of the ADC (<5V), an on-chip capacitive divider is used to generate v_{div}, a fraction of the relatively high voltage generated by the PEH (up-to 20V). Then v_{div} is digitalized thanks to an 8bits successive approximation analog-to-digital converter (ADC SAR). Finally, the power information is sent to a digital circuit which realizes the state-machine operation described by Fig.5.a.

A simulated trajectory of the Δϕ convergence is given in Fig.5.b by playing a sequence including two vibration frequency shifts (from 47Hz to 56Hz then from 56Hz to 52Hz). After each frequency shift, the P&O algorithm tracks the new maximum power point (MPP) by tuning the value of Δϕ. When the MPP is reached, the P&O algorithm oscillates around it. During normal operation, the algorithm consumption lies around 30nW.

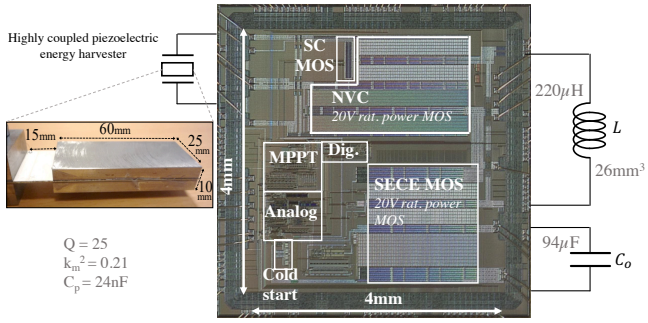

Fig. 7. Micrograph of the proposed integrated circuit.

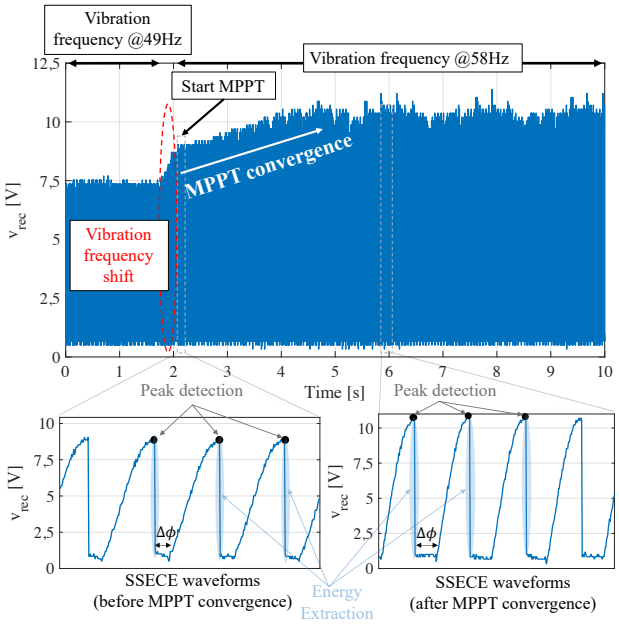

Fig. 8. Experimental waveforms of the rectified piezoelectric voltage v_{rec} during the MPPT convergence of the proposed IC. The harvested power is proportional to the squared peak of the rectified piezoelectric voltage.

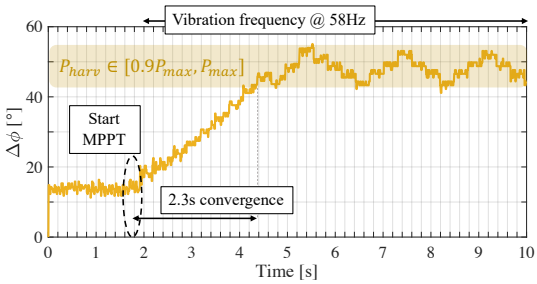

Fig. 9. Measurement of the angular short-circuit duration Δϕ during the MPPT convergence of the proposed IC.

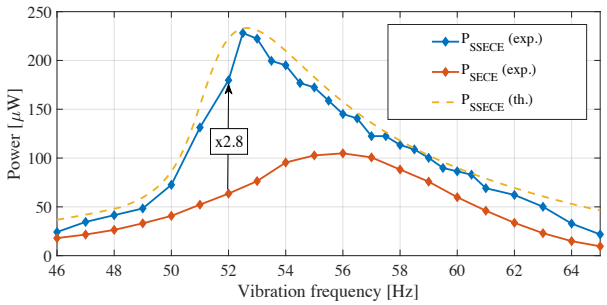

Fig. 10. Stored power with SSECE and SECE measured with the proposed IC. Dashed lines represent theory predictions from [4].

V. Experimental Results

The SSECE integrated circuit has been fabricated in CMOS 0.6μm technology. A micrograph of the fabricated chip is shown in Fig. 7. The transistors of the power path safely operate up-to 20V ensuring the MPP convergence under up-to 0.2g vibration excitation at resonance. The IC is connected to a highly coupled piezoelectric energy harvester made with PZT material exhibiting an electromechanical coupling k_m^2 of 21%, a quality factor Q of 25 and an intrinsic capacitance of 24nF [5].

The self-powered operation of our circuit is ensured as long as both the amplitude of v_p and the output voltage v_{out} remain greater than 1.9V. Fig. 8 and Fig. 9 show the convergence of P&O algorithm when these conditions are met, and when a vibration frequency shift is applied under a constant acceleration of 0.08g. After the frequency shift, the tunable parameter Δϕ of the implemented SSECE converges toward the optimal value (~50°) to maximize the extracted power from the PEH. In Fig.8, since v_{rec} is acquired for a fairly long time (10s) at a low sampling rate (5kHz), we cannot observe the (relatively quick) instants it drops below 0V.

After the Δϕ convergence, the harvested power has been measured against a large vibration frequency range and has been compared to the standard SECE (Δϕ = 0°) in Fig. 10. Compared to SECE, the SSECE enlarges the off-resonance harvested power up to 280% around 52Hz. The harvesting bandwidth of 7.5Hz (14.7% of the resonant frequency) is 368% larger than the natural bandwidth of the harvester. Table 1 compares the harvesting performances of our IC to prior art. Our IC is the first to embed a self-tuned SSECE. Compared to the PSECE in [2], the SSECE maintains higher harvested power at lower frequencies (in the range [52Hz, 56.5Hz]). This is a key advantage since a lower frequency capability is associated to a larger PEH mass (and thus a larger volume) if the electrically-tuning strategy were not deployed. Indeed, the resonant frequency of the harvester is inversely proportional to the square root of the harvester mass, meaning that harvesting lower frequency vibrations usually takes a larger harvester [4]. The MPPT convergence time (2.3s against 13s in [2]) is also decreased thanks to a better tunable parameter response to frequency shifts.

VI. Conclusion

The proposed harvesting IC interface integrates a tunable SSECE to enlarge the frequency bandwidth by 368% compared to natural frequency of our PEH. By self-tuning a short-circuit duration, the IC senses periodically the extracted power and adapts the tunable parameter to maximize the harvested power. The whole circuit consumption is below 1μW including the power sensing, the P&O algorithm, and the sensors that sequence the four phases of the SSECE. Our circuit achieves a lowest power-peak frequency and faster convergence than the previously proposed PSECE. Its self-powered, self-tuned and self-calibrated capabilities make our IC a promising candidate for industrialization of robust and reliable harvesting systems.

Table 1 – Comparison between our IC and state-of-the-art solutions

	This work	ISSCC'20 [2]	ISSCC'18 [1]	TPEL'15 [3]	JSSC'14 [6]	ISSCC'16 [7]	Unit
Scheme Type	SSECE	PSECE	Delayed SECE	Delayed PSSHI	SECE	PSSHI	-
Technology	0.6	0.6	0.35	Discrete	0.35	0.35	µm
Voltage rating	20	20	5	-	**200**	5	V
Inductance	**220**	**220**	>2000[b]	880	10000	3300	µH
Load independent	**Yes**	**Yes**	**Yes**	No	**Yes**	No	-
Cold start	**Yes**	**Yes**	**Yes**	No	**Yes**	**Yes**	-
Self-powered	**Yes**	**Yes**	**Yes**	No	**Yes**	No	-
Conversion efficiency	**94**	**94**	-	-	61	94 (OPP only)	%
MPPT	**P&O**	**P&O**	LUT	No	No	No	-
Pre-calibration	**No**	**No**	Yes	Yes	**No**	Yes	-
FoM[a] (bandwidth)	368	**446**	256	209[b]	<200	<100[b]	%
FoM[c] (convergence)	**21.3**	3.8	N/A	N/A	N/A	N/A	%
Normalized mass[d]	**114**	111	100	100	N/A	N/A	%

(a) FoM (bandwidth) = bandwidth of the output power over the natural bandwidth of the transducer (f_{res} / Q) (b) Estimated from the paper (c) FoM (convergence) = Q / (τ f_{res}) with τ being the time taken to make the parameters converge when changing the vibration frequency from the lowest to the highest HBW frequency. (d) Equivalent mass of the system to obtain the peak power frequency, divided by the real mass.

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