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Compact Modeling of 3D Vertical Junctionless Gate-all-around Silicon Nanowire Transistors

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***Abstract*—This paper presents a physics based, computationally efficient compact modeling approach for 3D vertical gate-all-around junctionless nanowire transistor (JLNT) arrays designed for future high performance computational logic circuit. The model features an explicit continuous analytical form adapted for a 14 nm channel JLNT technology and has been validated against extensive characterization results on a wide range of JLNT geometry, depicting good accuracy. Finally, preliminary logic circuit simulations have been performed for benchmarking performances of transistor logic circuits, such as inverters and ring oscillators, designed using the developed model.**

Keywords-Junctionless nanowire tranistors, compact model, high-speed logic circuit, heterogeneous integration.

I. Introduction

Data size and functionality requirements for computing systems are increasing rapidly with the expectation that hardware performance will continue to improve. For integrated circuit applications involving high-speed logic computing and low power dissipation, semiconductor technology scaling is mandatory. However, due to the anticipated end of conventional technological roadmap at the 7 nm gate node, it is becoming increasingly challenging for process engineers to maintain device functionality. Particularly, process challenges such as obtaining an abrupt shallow doping gradient at the source/drain junction, could be circumvented by junctionless nanowire transistors (JLNT) [1], due to high and uniform dopant concentration across its body and S/D regions. Combined with the merits of junctionless transistors such as high on/off current ratio or better electrostatic control in a gate-all-around (GAA) structure, vertical integration is an attractive approach because of its intrinsic 3D nature, which is more favorable for gate length and contact area scaling [2]. While JLNTs are certainly crucial building blocks for ultimate scaling of MOS transistors especially to support complex circuit architectures in high-speed logic applications, it is essential for the designers to have a physics-based, accurate, computationally efficient compact model which is independent of fitting parameters, has an explicit and continuous solution over the entire range of operation and is compatible with existing SPICE design framework. There have been several such modeling approaches, including that of [3, 4], which have mainly focused on long-channel JLNTs. Moreover, most of these works have used TCAD data for model validation, and thus lack validation against experimental data from actual JLNTs. This work presents a compact modeling approach developed based on the physics-based JLNT compact model in [3] adapted for nanowire arrays of short channel JLNTs with gate lengths of 14 nm. The drain current equation has been modified to incorporate leakage and band-to-band tunneling currents and access region resistances. Moreover, the model accuracy has been validated against extensive measurements on an emerging vertical JLNT technology from LAAS [5, 6] that has also been exploited previously for extensive noise characterization [7, 8].

II. Compact Model Formulation

The model formulation is based on the unified charge-based control model (UCCM) elaborated in [3] for long-channel devices, which furthers the physical basis of the JLNT model presented in [4]. To overcome the limitations of the latter model, specifically in terms of the piece-wise continuous drain current model that requires additional smoothing functions and fitting parameters to bridge the depletion and accumulation modes of operation, the explicit and non-piece-wise solution in [3] treats the mobile charge (Q_m) as decoupled between the depletion (Q_{DP}) and complementary (Q_C) components. In the depletion mode the UCCM expression has been formulated as [3],

$$Q_{DP} = Q_{eff} LW \left\{ \frac{Q_{sc}}{Q_{eff}} \exp\left(\frac{V_g - V_{th} - \eta V}{\eta \phi_T} + \frac{Q_{dep}}{Q_{sc}} \right) \right\} \quad (1)$$

With the depletion charge, $Q_{dep}=qN_DR/2$, the effective charge during depleteion, $Q_{eff} = Q_{sc}\eta C_{ox}\varphi_T/(Q_{sc}+\eta C_{ox}\varphi_T)$, $Q_{sc}=2\varepsilon_{Si}\varphi_T/R$, R being the nanowire diameter, η being an interface trap parameter, φ_T being the thermal voltage and V is the potential along the channel. Lambert W functions, LW, have been used in both [3] and [4] for developing the solution for total mobile charge in the JLNT. While the expression for Q_{DP} in (1) predicts the depletion contribution correctly (for $V_g<V_{th}$), it underestimates the value of the drain current above the flat-band condition. So in accumulation mode, especially in high accumulation, with $Q_C \geq Q_{dep}$, the charge Q_C has been derived to act complementary to Q_{DP}, considering

that the threshold voltage is pinned at V_{FB} in the accumulation region, in order to avoid using additional smoothing functions and improve simulation time. Under high accumulation $Q_C \geq Q_{dep}$ and Q_C is simplified using another Lambert function as following [3],

$$Q_C = \eta C_c \phi_T LW \left\{ \frac{Q_{sc}}{\eta C_c \phi_T} \exp\left(\frac{V_g - V_{FB} - \eta V}{\eta \phi_T} \right) \right\} \tag{2}$$

With corrected electrostatic control through $C_c = C_{ox} - C_{eff}$, $C_{eff} = 1/C_{ox} + R/2\varepsilon_{Si}$.

Having evaluated both the depletion and complementary parts of the mobile charge, one can formulate the non-pice-wise continuous model of the total drain current in terms of the Q_{DP} and Q_{DC} at the source and the drain end, Q_{DP0}, Q_{C0} and Q_{DPL}, Q_{CL}, respectively,

$$I_{DS,0} = \mu_{eff} \frac{2\pi R}{L_{eff}} \phi_T \left[\frac{Q_{DP}^2}{2\eta C_{ox} \phi_T} + Q_{DP} + \frac{Q_C^2}{2\eta C_c \phi_T} + 2Q_C \right]_{Q_{DPL}, Q_{CL}}^{Q_{DP0}, Q_{C0}} \tag{3}$$

Here, η is an interface trap parameter with corrected electrostatic control in accumulation through $C_c = C_{ox} - C_{eff}$, $C_{eff} = 1/C_{ox} + R/2\varepsilon_{Si}$. The expression of drain current is free of any fitting parameters and can be evaluated based on the physical device parameters such as that of geometry and doping. Additionally, short channel effects were also taken into account considering velocity saturation, an effective mobility, μ_{eff}, and incorporating an effective gate length, $L_{eff} = L - \Delta L$, where L is the physical device gate length and ΔL is calculated following [9],

$$\Delta L = S \sqrt{\frac{\varepsilon_0 \varepsilon_{Si} R}{2C_{ox}}} \ln \left[\frac{(V_d - V_{deff}) \left(1 + \sqrt{1 + \left(\frac{2 \frac{v_{sat}}{\mu} \sqrt{\frac{\varepsilon_0 \varepsilon_{Si} R}{2C_{ox}}}}{V_d - V_{deff}} \right)^2} \right)}{2 \frac{v_{sat}}{\mu} \sqrt{\frac{\varepsilon_0 \varepsilon_{Si} R}{2C_{ox}}}} \right] \tag{4}$$

With, v_{sat} being the saturation velocity and S being a parameter ensuring that ΔL tends to zero below the threshold, defined as [9],

$$S = \sqrt{1 - \frac{1}{1 + B \frac{Q_{DP0} + Q_{C0}}{C_{eff} \phi_T}}} \tag{5}$$

Where $Q_{DP0} + Q_{C0}$ is the total mobile charge at the source, given by the long channel expression and B is a smoothing parameter. Furthermore, the short channel corrections incorporates an effective drain voltage, V_{deff}, through (4) that reaches its maximum at V_{SAT}, the saturation voltage [9],

$$V_{deff} = V_{SAT} - V_{SAT} \frac{\ln\left(1 + \exp\left(A2\left(1 - \frac{V_d}{V_{SAT}}\right)\right)\right)}{\ln(1 + \exp(A2))} \tag{6}$$

Here, $A2$ is another smoothing parameter for the transition of the drain voltage to V_{SAT}. Considering that the source and drain access region resistances degrade the drain current above threshold, the final expression of the drain current can be written as a function of the long channel current ($I_{DS,0}$), using (3), taking into account the corrections due to short-channel effects described by equations (4)-(6), as follows [9],

$$I_{DS} = \frac{I_{DS,0} NF}{1 + 2\pi \frac{R}{L_{eff}} NF \mu_{eff} (R_S + R_D) \left[(Q_{DP0} + Q_{C0}) - \eta_1 \left(Q_{DP0} + Q_{C0} - \left(Q_{DP,VDeff} + Q_{C,VDeff} \right) \right) \right]} \tag{7}$$

Here, R_S and R_D are the source and drain series access resistances, respectively; NF is the number of nanowires in parallel, η_1 is a fine tuning parameter to take into account the drain-voltage dependence of the series access resistances and $Q_{DP,Vdeff} + Q_{C,Vdeff}$ is the total mobile charge at the drain end (pinch-off) of the channel.

Additionally, considering formation of Schottky contacts at the source and drain access regions, the subthreshold leakage currents are also taken into account. Consequently, thermionic (I_{th}), tunneling (I_{tun}) and band-to-band tunneling (BTBT) contributions through gate-induced drain leakage (GIDL) are added as separate branch currents [10] to the total drain current, in order to model the subthreshold behavior of the drain current. The expression used in the compact model for the BTBT current at the drain end reads [10],

$$I_{GIDL} = 2\pi R L_{Access} NF \cdot A_{GIDL} V_{DS} E_{segd}^{\,2} \exp\left(-\frac{B_{GIDL}}{E_{segd}} \right) \tag{8}$$

With L_{Access} being the lengths of the source and drain access regions outside the channel, B_{GIDL} is a physics based parameter with a theoretical value of 21.3 MV/cm [10] and E_{segd} is the electric field in the drain overlap region, given as,

$$E_{segd} = \frac{C_{ox} \sqrt{V_{segd}^{\,2} + (C_{GIDL} V_{DS})^2}}{\varepsilon_0 \varepsilon_{Si}} \tag{9}$$

Here, V_{segd} is the gate-drain voltages across the oxide and A_{GIDL}, C_{GIDL} are two GIDL fitting parameters.

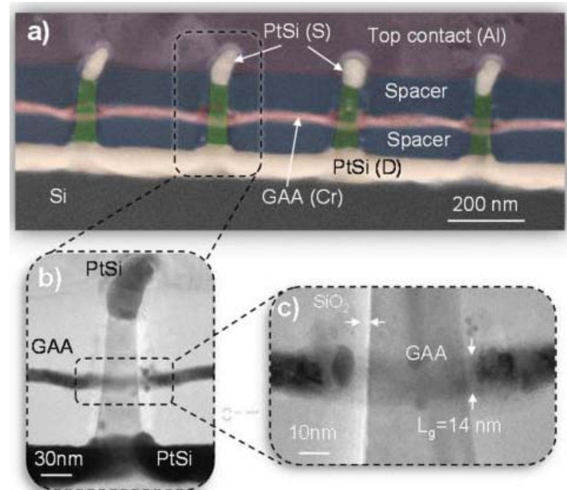

Fig. 1: The vertical JLNT: (a) SEM image of nanowire arrays, (b) single nanowire showing its (c) gate formation (reproduced from [2]).

III. RESULTS AND DISCUSSIONS

The JLNT technology has a junction-less architecture composed of a homogenous highly doped nanowire channel (physical channel length of 14 nm), fabricated on boron doped (2×10^{19} /cm^3) Si Substrate, with the current flowing between the silicided source/drain contacts being controlled by a gate-all-around structure (Fig. 1). More details on the fabrication steps can be found in [5].

A. *Compact Model Validation*

In this work, the compact model presented in the previous section is validated against measurement results on a wide range of geometries and test structures that have diameters (D) ranging between 22 and 50 nm with 16 to 625 nanowires in parallel (NF). Here we show results from nanowires with a diameter of 22 nm with different number of nanowires in parallel. Figs. 2 (a) and (b) show the I_D-V_{GS} and I_D-V_{DS} of a JLNT with 22 nm of nanowire diameter and 16 nanowires in parallel. The model simulation results show very good agreement with the measurements over the entire bias range, indicating accuracy of individual modules of the compact model. A second order validation is performed in Figs. 2 (c) and (d) depicting the transconductance, g_M, and output conductance, g_{DS}, of the JLNT, further affirming model accuracy, despite a somewhat noisy measurements.

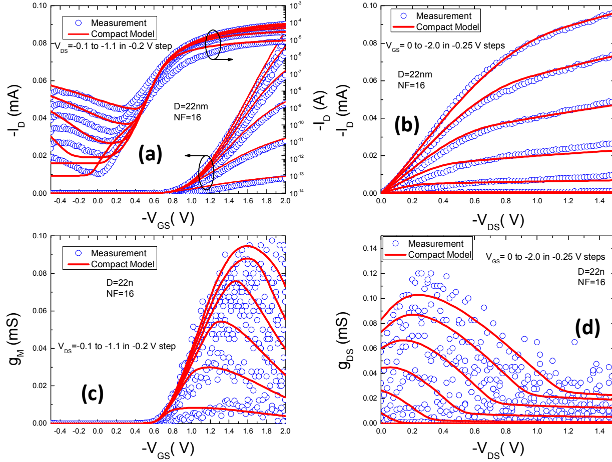

Fig. 2: (a) I_D-V_{GS}, (b) I_D-V_{DS} (c) transconductance and (d) output conductance of a JLNT with 22 nm diameter and 16 nanowires in parallel.

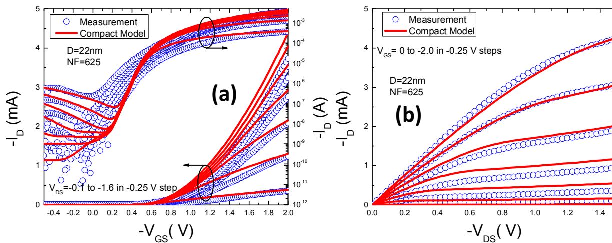

Fig. 3: (a) I_D-V_{GS}, (b) I_D-V_{DS} of a JLNT with test structures having a diameter 22 nm and 625 nanowires in parallel.

Extended model validation has been performed on two other test structures, with different geometries available from the same technology. Figs. 3 (a) and (b) show the I_D-V_{GS} and I_D-V_{DS} of JLNT test structures with a diameter of 22 nm with 625 nanowires in parallel. Good model agreement is obtained in this case as well. Similar validation is depicted in Fig. 4 for a JLNT test structure with a diameter of 22nm and 400 nanowires in parallel, again depicting good agreement with the model simulation.

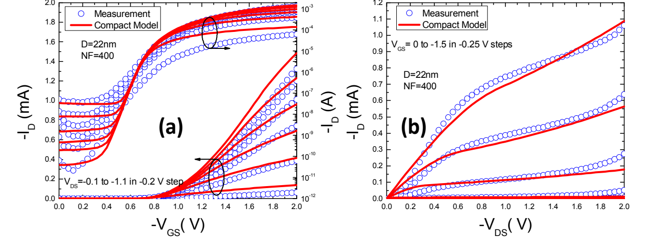

Fig. 4: (a) I_D-V_{GS}, (b) I_D-V_{DS} of a JLNT with test structures having a diameter 22 nm and 400 nanowires in parallel.

Slight discrepancies observed in the subthreshold region of operation will require further investigation and might require additional effects, such as drain-induced barrier lowering (DIBL), to be included within the model implementation and thus lies within the future scope of this work.

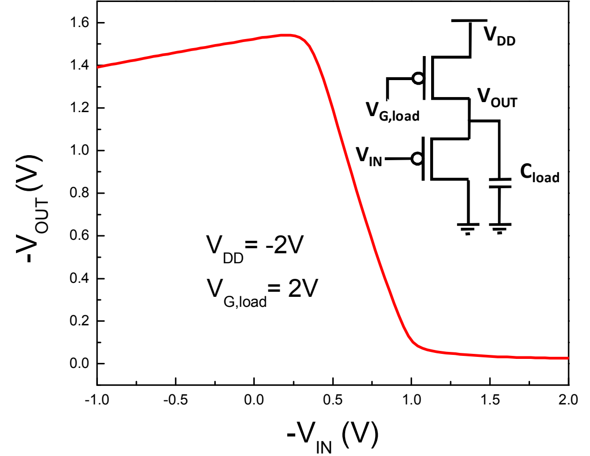

Fig. 5: Transfer Characteristics of an inverter designed with two p-type JLNTs; inset: Schematic of the inverter circuit.

B. *Circuit Demonstraion*

Having validated the accuracy of the compact model at transistor level, we have exploited the model further for logic circuit demonstrations. As a first step toward benchmarking circuit simulation using the model, we have studied a simple inverter circuit designed using two p-type JLNTs (with NW diameters of 32 nm and 16 nanowires in parallel), as illustrated by the schematic shown in the inset of Fig. 5. The upper p-FET acts as an active load when applied a positive load bias, $V_{G,load}$ of 2V and the input signal is applied to the gate of the p-

FET below. A supply voltage, V_{DD}, of -2 V and a load capacitance, C_{load}, of 1 fF have been used in the simulation. Fig. 5 shows the transfer characteristics of the inverter which demonstrates a slight asymmetric yet a rather sharp switching from the high to the low state. Note that our previous works [5, 6] report a proof-of-concept CMOS inverter consisting of both n- and p-type JLNTs, which showed similar characteristics as the present work.

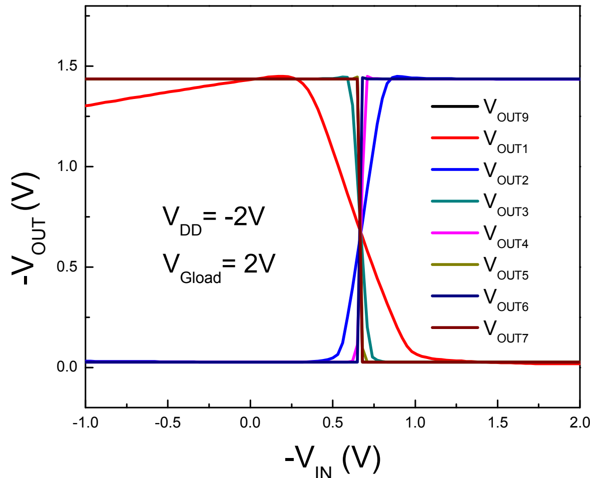

Fig. 6: Transfer Characteristics of a 9-stage ring oscillator depicting intermediate outputs of the cascaded stages.

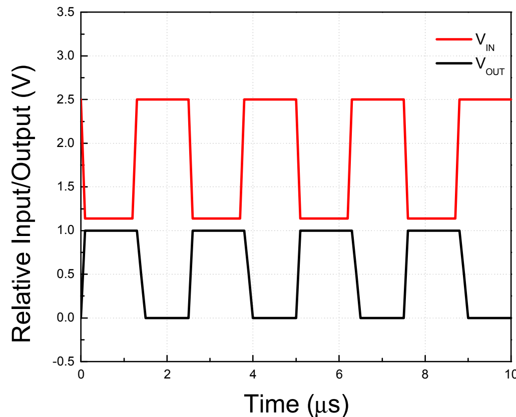

Fig. 7: Transient simulation of the inverter circuit depicting the input and the output waveforms.

Next, we have studied a 9-stage ring oscillator consisting of 9 inverter stages in cascade. Each inverter of the ring-oscillator has the same characteristics as shown in Fig. 5. In Fig. 6, the outputs of the different stages of the ring oscillator are shown on the voltage transfer characteristics (VTC). As observed from the figure, the output of the first stage resembles the VTC of the single stage inverter (Fig. 5), while the high-to-low transition continues to be sharper from one stage to the next. Although, the output of the 9th stage shows almost no switching dissipation, from the output of the third stage onwards the transitions are quite similar and sharp. This indicates that the optimum number of stages required is 3. Finally, Fig. 7 shows the transient simulation of the inverter circuit designed using two p-type JLNTs, demonstrating that for a given input signal V_{IN}, the output signal follows it in opposite phase, in accordance with classical inverter operation.

IV. CONCLUSIONS

In this work, we report a SPICE-compatible Verilog-A compact model for 14 nm gate-all-around vertical junctionless nanowire transistors, validated against extensive measurements on an emerging vertical JLNT technology. Good model accuracy has been observed over different geometries under study. The compact model has been exploited further for studying the performances of transistor logic circuits with active loads, including an inverter and a 9-stage ring oscillator. The proposed modeling framework will be indispensable for future high-performance logic circuit design.

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