A comprehensive in-depth study of tri-state inverter based DCO

Mehdi Terosiet, Eldar Zianbetov, Farouk Vallette, Marie-Minerve Louërat, Patrick Garda, Dimitri Galayko, Sylvain Feruglio

A Comprehensive In-Depth Study of Tri-State Inverter Based DCO

M. Terosiet, E. Zianbetov, F. Vallette, M.M. Louerat, P Garda, D. Galayko, and S. Feruglio,

January 29, 2020

Abstract

This paper proposes an in-depth analysis of the tri-state inverter based digitally controlled oscillator. This oscillator topology has been reported in numerous publication, however its features remain poorly understood. In this study, we propose to focus on these lacks. We specifically addressed the oscillation period and the associated jitter as these quantities are the design key parameters. In this paper, we propose analytical expressions taking into consideration the design, the technology as well as the input code. These equations are suitable for hand calculations and have helped to establish a design methodology for rapid implementation. Two circuits have been designed in STMicroelectronics CMOS 65nm process. The first one was evaluated through simulations. Then, the measurement results obtained with the second circuit manufactured within the same technology node are presented. Finally, the experimental data support the proposed theory.

CMOS, Digitally Controlled Ring Oscillators, Jitter.

1 Introduction

In System-on-Chip (SoC), the clock generation represents a key issue for the proper circuit operation. It is generally based on a Phase-Locked Loop (PLL). These last two decades have witnessed the gradual substitution of the classic analog PLL in favor of the All-Digital PLL (ADPLL) [1–4]. Indeed, digital phase synthesis techniques offer various advantages. Among other things, they can be synthesized in a digital design flow similar to the one used for the major part of the circuit [5].

The Digitally Controlled Oscillator (DCO) is the critical issue of the ADPLL design, since it outscores the main ADPLL characteristics, such as the jitter, the frequency range and the resolution of the system [6]. The LC-based DCOs provide the best noise performance and, thus, are the best candidates for RF applications [7,8]. However, controlled oscillator for on-chip clock generation is usually based on a Ring Oscillator (RO). Ring-architectures are more compact and benefit from their regular periodic spatial structure. Moreover, the possibility to design the oscillator with digital standard cells provided by the foundries makes it a very attractive solution [9, 10]. Hence, this is by far the most used topology for the implementation of the clock generator [11–13].

One of the actual trends in tuning the oscillation frequency is based on the association of a classic RO and an array of Tri-State (TS) inverters as illustrated by Fig. 1 [14–16]. Complications occur when designing the circuit. The literature does not offer a proper design methodology or guidelines, making the design phase time-consuming, even if numerous papers relate this DCO architecture.

In 2011, we addressed a part of this lack by equating the oscillation period as a function of the tuning matrix configuration and the technology parameters [17]. In this further work, we formulate the jitter exhibited by the controlled oscillator as a function of the input code. These equations have been included in a design methodology which highlights the trade-off

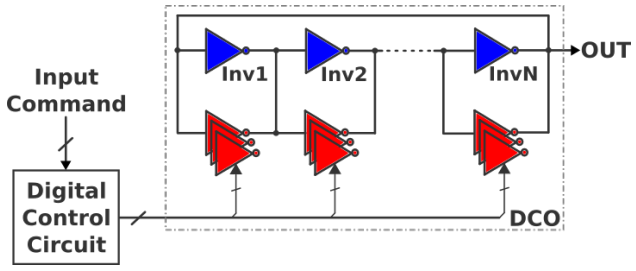


Figure 1: Architecture of the tri-state inverter based DCO.

between period uncertainty and electrical power consumption. Such a study was carried out on a different architecture in [18]. In our approach, we paid much attention to express the DCO parameters, such as oscillation period and jitter, with respect to the well-known results of a classic RO. This will ease the use of our method for interested designers. Moreover, our in-depth analysis enables the sizing of MOSFETs when a full-custom design is preferred for given specifications.

This paper lays out our contribution into seven parts. Following this introduction, Section 2 introduces the background of this study and, more specifically, the DCO period formulation. Starting from these developments, the intrinsic random jitter analysis is done in Section 3. From there, a design guideline is proposed in Section 4 in order to implement the DCO from specifications. On this basis, the developed concepts are validated through simulations in Section 5 with a first study case. Experimentations on a fabricated circuit allows extending the calculation method and the obtained results are shown in Section 6. Finally, in the last Section, the conclusions and perspectives for this work are exposed.

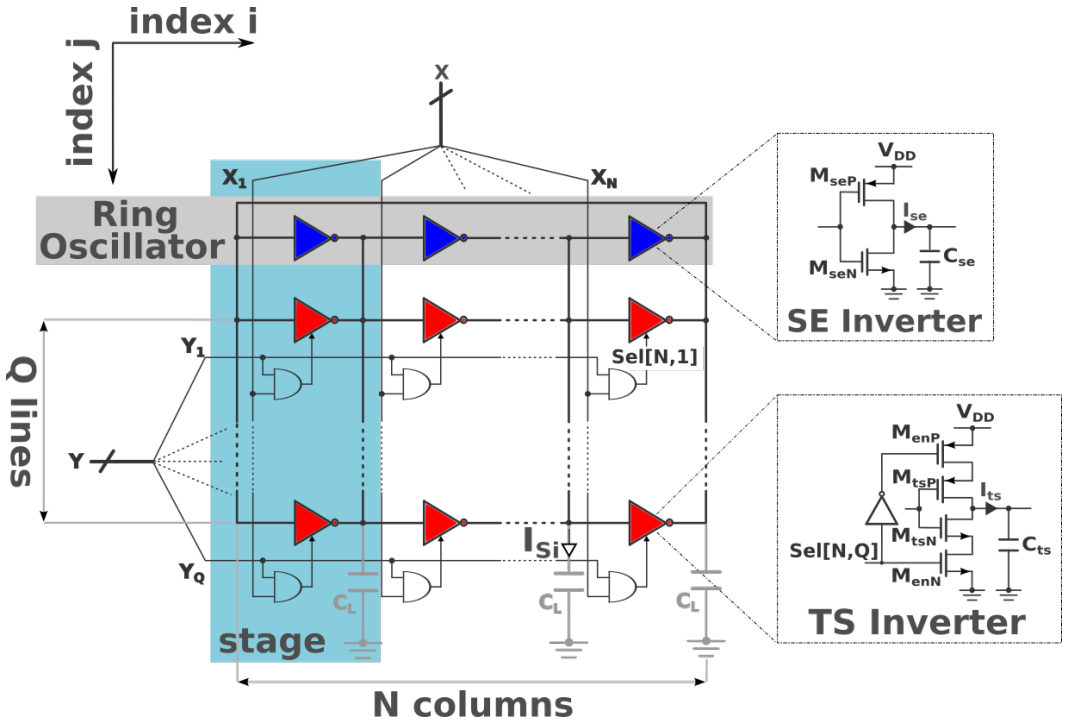


Figure 2: Schematic view of the tri-state inverter based DCO.

2 Background

After a brief description of the DCO topology under study and its operation, the analysis conditions are presented in order to finally express the theoretical oscillation period.

2.1 DCO Architecture

The Fig. 2 illustrates the DCO structure. It is composed of the main chain, a classic RO designed with N usual single-ended (SE) inverters (N is odd and greater than or equal to three), associated to a matrix of TS inverters. Therefore, each stage is defined as a SE inverter with Q TS cells connected in parallel.

The array of $N \times Q$ TS cells and, consequently, the DCO configuration, are controlled by the two-dimensional thermometer code applied through both vectors X and Y. Thus, the $(i,j)^{th}$ TS element is turned-on by a high state of the signal $Sel[i,j]$ ($i = 1, 2, \ldots, N$ and $j = 1, 2, \ldots, Q$). The latter results from the AND operation of the both bits X_i and Y_j. Note that this control scheme activates a rectangular set of TS cells, whose length and width are X and Y.

2.2 Principle of Operation

This circuit is a digital implementation of the current-starved RO [19]. The period of the generated signal is tuned by modulating the fan-out of each stage while its capacitive load remains constant. Indeed, in addition to the current sourced (or sunk) by the SE inverter I_{se}, in the DCO case, the activation of a TS inverter provides an additional charging (discharging) current I_{ts} to the effective capacitive load C_L, see Fig. 2. This capacitor is equivalent to the load introduced by each inverter of the concerned stage and does not depend on the input code in first approximation.

Therefore, as a function of the Y vector, the total current provided by the i^{th} stage (i.e., a single column) to C_L can be approximated by:

$$I_{Si} = I_{se} + I_{ts}X_i \sum_{j=1}^{Q} Y_j = I_{se} + I_{ts}X_i\mathcal{Y} \tag{1}$$

with $\mathcal{Y} = \sum_{j=1}^{Q} Y_j$, the decimal value associated to the word Y, within the range $[0; Q]$.

From there, the delay introduced by the i^{th} stage is defined as:

$$\tau_{Di} = \eta \frac{C_L}{I_{Si}} V_{DD} \tag{2}$$

where η is a dimensionless coefficient (between 0.5 and 0.9) and the supply voltage V_{DD} corresponds to the output voltage swing of each stage. Then, the oscillation period, T_{OSC}, can be derived such as [20]:

$$T_{OSC} = 2 \sum_{i=1}^{N} \tau_{Di} \tag{3}$$

This equation is the starting point for the formulation of the oscillation period. To go further, some assumptions are made.

2.3 Analysis Conditions

In order to obtain a simple and fairly accurate modeling of T_{OSC}, we consider that:

1. All SE inverter stages are identical. It applies to the TS cells too. All transistors have the same channel length.
2. The PMOS and NMOS transistors of all inverters are balanced in order to equalize both charge and discharge currents.
3. The current provided by an enabled TS inverter is a fraction, β, of the current due to a SE one, such as:

$$\beta = \frac{I_{ts}}{I_{se}} \tag{4}$$

   Thus, (1) can be rewritten as follows:

$$I_{Si}[\mathcal{Y}] = I_{se}(1 + \beta X_i \mathcal{Y}) \tag{5}$$

4. The most part of the charges is transferred to (or from) C_L, during transitions, when the active transistors (either M_{seP} and M_{tsP} or M_{seN} and M_{tsN}) operate in the saturation regime [21, 22].
5. The effective load capacitance, C_L, is quasi-invariant with the input code. By taking into account that a transistor parasitic capacitance is a function of its gate surface [23], we define the equivalent stage capacitive load as:

$$C_L = C_{se} + QC_{ts} = C_{se}(1 + \beta Q) \tag{6}$$

   where C_{se} and C_{ts} are the capacitances introduced by a main SE cell and a TS device, respectively.
6. The selection transistors M_{enP} and M_{enN} are considered as perfect switches. Thus, the effect of their equivalent drain-to-source resistance R_{ON} is negligible when they are enabled. R_{OFF} is supposed infinite when disabled.
7. The matrix filling is incremental by row or by column. When the bit X_i equals 0, whatever the input Y, all tri-state inverters in the concerned stage are disabled and, when X_i is high, cells are enabled with Y_j.

2.4 Analytical Expression of the Oscillation Period

Equation (2) can be rewritten by relying on the previous considerations, especially equations (5) and (6). It allows expressing the time-delay of a stage, τ_{Di}, as a function of $\mathcal{Y}$ and the delay introduced by a SE inverter τ_{Dm} (when the tuning matrix is completely disconnected):

$$\tau_{Di}[\mathcal{Y}] = \eta \frac{C_{se}(1+\beta Q)}{I_{se}(1+\beta X_i \mathcal{Y})} V_{DD} = \tau_{Dm} \frac{1+\beta Q}{1+\beta X_i \mathcal{Y}} \tag{7}$$

where:

$$\tau_{Dm} = \eta \frac{C_{se}}{I_{se}} V_{DD} \tag{8}$$

As a consequence, from (3) and the sixth hypothesis made in the previous subsection, the oscillation period, with respect to the bi-dimensional input command, becomes:

$$\begin{aligned} T_{OSC}[\mathcal{X},\mathcal{Y}] &= 2\{\mathcal{X}\tau_{Di}[\mathcal{Y}] + (N-\mathcal{X})\tau_{Di}[0]\} \\ &= T_{OSCm}(1+\beta Q)\left(1 - \frac{\mathcal{X}}{N}\frac{\beta\mathcal{Y}}{1+\beta\mathcal{Y}}\right) \end{aligned} \tag{9}$$

where, as for $\mathcal{Y}$, $\mathcal{X} = \sum_{i=1}^{N} X_i$ is a decimal value ranging from 0 to N and is associated to the vector X. Besides, the newly introduced parameter, T_{OSCm} in (9), stands for the oscillation period of the main chain (when the tuning matrix is totally disconnected). It is classically defined by (10):

$$T_{OSCm} = 2N\tau_{Dm} \tag{10}$$

Because (9) relates the tuned period to that of the classic RO, it provides valuable information and some insights must be extracted. Indeed, this equation demonstrates that the tuning matrix acts like a brake on the RO (main chain). When all tuning cells of the matrix are selected (i.e., $\mathcal{X} = N$ and $\mathcal{Y} = Q$), the oscillation period is minimum and equals that of the SE RO, with:

$$T_{OSCmin} = T_{OSC}[\mathcal{X} = N, \mathcal{Y} = Q] = T_{OSCm} \tag{11}$$

This is explained by the fact that the C_L surplus compared to C_{se} is compensated by the current supplied by all TS inverters.

In the reverse case, when the TS inverters are off, the controlled oscillator reaches its maximal output period:

$$T_{OSCmax} = T_{OSC}[\mathcal{X} = 0, \mathcal{Y} = 0] = T_{OSCm}(1+\beta Q) \tag{12}$$

Indeed, only the current supplied by the SE element, I_{se}, charges (discharges) C_L, which has a capacitance $(1+\beta Q)$ times greater than that introduced by the unique main inverter, C_{se}.

By the end, a compact expression for the nominal oscillation period can be derived as in the following equation :

$$T_{OSC}[\mathcal{X},\mathcal{Y}] = T_{OSCmax}(1 - \delta[\mathcal{X},\mathcal{Y}]) \tag{13}$$

with:

$$\delta[\mathcal{X},\mathcal{Y}] = \frac{\mathcal{X}}{N}\frac{\beta\mathcal{Y}}{1+\beta\mathcal{Y}} \tag{14}$$

However, due to the intrinsic noise of components, the nominal period is prone to drift [20]. Thus, the next section studies the period jitter. This is a step forward for a complete analytical and behavioral model of this DCO topology. Furthermore, the jitter analysis is one of the most significant contributions to the present work.

3 Period Jitter Analysis

We exclusively focus on the random jitter observed on a short time window, typically equivalent to one clock cycle [14]. It originates from the intrinsic noise of transistors composing the DCO. Noise implies uncertainties on the threshold crossing moment when a delay stage toggles [24, 25].

Only the white noise is concerned in this study. On the one hand, for short observation time, the 1/f noise has no effect. On the other hand, flicker noise is rejected by the PLL loop filter, where the DCO is generally implemented [26, 27].

Based primarily on the jitter analysis of the main chain (matrix disconnected), we then perform an analytical model of the DCO jitter, by quantifying the impact of the matrix with respect to its state.

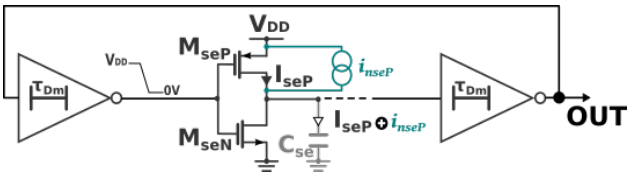


Figure 3: The current and noise charging the equivalent output capacitor, when a SE inverter toggles, in a three delay stage ring oscillator.

3.1 Jitter of the Main Chain

According to [28] and to assumption 2 made in the subsection 2.3, we can suppose that the thermal noise contribution of each transistor is ideally of the same amount. Moreover, we assume that all noise sources are uncorrelated to each other, as it is classically the case [20, 26, 28].

Focusing on the charge step, i.e. M_{seP} drives the current while M_{seN} is OFF, as depicted in Fig. 3, the capacitor C_{se} integrates both signal and noise into voltage over the time-window $[0; \tau_{Dm}]$. Hence, referring to (2), the threshold crossing dynamics are such that:

$$V_{DD} = \int_0^{\tau_{Dm}} \frac{I_{seP} + i_{nseP}}{\eta C_{se}} dt \tag{15}$$

where i_{nseP} is the thermal noise current due to M_{seP} operating in the saturaion region. i_{nseP} is associated to its single-sided Power Spectral Density (PSD) $\mathcal{S}_{i_{nseP}}$. Therefore, the mean time-delay, $\overline{\tau_{Dm}}$, is described by (8) and its variance, ${\sigma_{\tau_{Dm}}}^2$, is given by:

$${\sigma_{\tau_{Dm}}}^2 = \frac{1}{2} \frac{\mathcal{S}_{i_{nseP}}}{{I_{seP}}^2} \tau_{Dm} = {\kappa_m}^2 \tau_{Dm} \tag{16}$$

The complete derivation of this last result can be found in [28], where we define ${\kappa_m}^2$ as the current noise Normalized PSD (NPSD):

$$\kappa_m = \frac{1}{\sqrt{2}} \frac{\sqrt{\mathcal{S}_{i_{nseP}}}}{I_{seP}} \tag{17}$$

Equation (16) is meaningful. On the one hand, it demonstrates that the delay variance of a stage is directly proportional to its nominal value. On the other hand, it is also proportional to the current noise NPSD.

Considering the assumptions on noise characteristics, the variance of the oscillation period, ${\sigma_{T_{OSCm}}}^2$, is obtained by summing (16) for both rising and falling edges of the N main inverters. It yields:

$${\sigma_{T_{OSCm}}}^2 = 2N{\sigma_{\tau_{Dm}}}^2 = {\kappa_m}^2 T_{OSCm} \tag{18}$$

and the period jitter is the RMS value of (18).

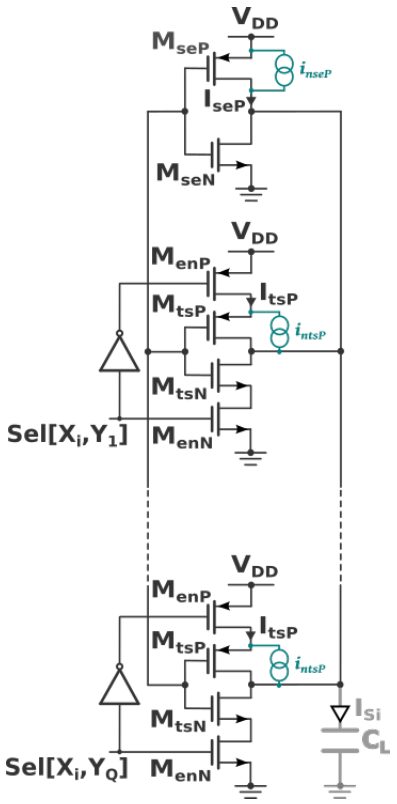


Figure 4: Currents and noises provided to C_L by a tuned stage.

3.2 Impact of the Tuning Matrix

Similarly to the previous case, the matrix noise contribution can be analyzed by relying on the Fig. 4. In addition to the noise sourced by M_{seP}, the noise sources, i_{ntsP}, provided by the enabled TS inverters have to be considered. The total noise current integrated by C_L is the direct sum of each of these uncorrelated sources. Its PSD can be formulated, for the i^{th} column and with respect to $\mathcal{Y}$, as follows:

$$\mathcal{S}_{i_{nSi}}[\mathcal{Y}] = \mathcal{S}_{i_{nseP}}(1 + \beta X_i \mathcal{Y}) \tag{19}$$

Moreover, based on (16), the variance of the column delay can be expressed through:

$$\sigma_{\tau_{Di}}{}^2[\mathcal{Y}] = \kappa'^2[\mathcal{Y}]\tau_{Di}[\mathcal{Y}] \tag{20}$$

where the NPSD, κ'^2, depends on $[\mathcal{Y}]$, such as :

$$\begin{aligned} \kappa'^2[\mathcal{Y}] = \frac{1}{2}\frac{\mathcal{S}_{i_{nSi}}[\mathcal{Y}]}{I_{Si}{}^2[\mathcal{Y}]} &= \frac{1}{2}\frac{\mathcal{S}_{i_{nseP}}}{I_{seP}{}^2}\frac{1}{1+\beta X_i \mathcal{Y}} \\ &= \kappa_m{}^2 \frac{1}{1+\beta X_i \mathcal{Y}} \end{aligned} \tag{21}$$

Finally, to inject equations (21) and (7) in (20) results in:

$$\begin{aligned} \sigma_{\tau_{Di}}{}^2[\mathcal{Y}] &= \frac{1}{2}\frac{\mathcal{S}_{i_{nseP}}}{I_{seP}{}^2}\tau_{Dm}\frac{1+\beta Q}{(1+\beta X_i \mathcal{Y})^2} \\ &= \sigma_{\tau_{Dm}}{}^2 \frac{1+\beta Q}{(1+\beta X_i \mathcal{Y})^2} \end{aligned} \tag{22}$$

Thereby, for the i^{th} column, if every TS inverter is disabled, i.e. the bit X_i equals 0, the variance of the stage delay is $(1+\beta Q)$ times greater than that introduced by the main inverter (matrix disconnected). As a consequence for the oscillation period, its variance is governed by:

$$\sigma_{T_{OSC}}{}^2[\mathcal{X},\mathcal{Y}] = 2\{\mathcal{X}\sigma_{\tau_{Di}}{}^2[\mathcal{Y}] + (N-\mathcal{X})\sigma_{\tau_{Di}}{}^2[0]\} \tag{23}$$

With (22), it becomes:

$$\begin{aligned}\sigma_{T_{OSC}}{}^2[\mathcal{X},\mathcal{Y}] &= 2\mathcal{X}\sigma_{\tau_{Dm}}{}^2\frac{1+\beta Q}{(1+\beta X_i\mathcal{Y})^2} + (N-\mathcal{X})\sigma_{\tau_{Dm}}{}^2(1+\beta Q) \\ &= \sigma_{T_{OSCm}}{}^2(1+\beta Q)\times\left\{1-\frac{\mathcal{X}}{N}\left(1-\frac{1}{(1+\beta\mathcal{Y})^2}\right)\right\}\end{aligned} \tag{24}$$

It is worth noting that the variance of the DCO period remains directly proportional to that of the RO (without the tuning matrix): $\sigma_{T_{OSCm}}{}^2$, previously described by (18). This original formulation allows highlighting specific features. First, when each element of the connected matrix is disabled ($\mathcal{X}=0$ and/or $\mathcal{Y}=0$), the variance calculation leads to (25):

$$\begin{aligned}\sigma_{T_{OSC}}{}^2[0,0] &= \sigma_{T_{OSCm}}{}^2(1+\beta Q) \\ &= \sigma_{T_{OSC}max}\end{aligned} \tag{25}$$

Indeed, in this case, the delay of a stage is $(1+\beta Q)$ times longer than that of the main inverter and, the noise is integrated during this time. Furthermore, activating TS inverters yields the decrease of the period uncertainty. In this sense, $\mathcal{X}=N$ and $\mathcal{Y}=Q$ is a remarkable configuration. We previously demonstrated that the DCO oscillates at the natural frequency of the RO and, with (24), we show that the period variance is:

$$\sigma_{T_{OSC}}{}^2[N,Q] = \frac{\sigma_{T_{OSCm}}{}^2}{(1+\beta Q)} \tag{26}$$

This last relation shows for equivalent oscillation periods, the period jitter exhibited by the DCO is attenuated by a factor $\sqrt{1+\beta Q}$ compared to that of the unique main chain.

At the end, a compact expression for $\sigma_{T_{OSC}}{}^2$ can be derived as in the following equation:

$$\sigma_{T_{OSC}}{}^2[\mathcal{X},\mathcal{Y}] = \sigma_{T_{OSCmax}}{}^2(1-\vartheta[\mathcal{X},\mathcal{Y}]) \tag{27}$$

where $\sigma_{T_{OSCmax}}{}^2$ is defined by (25) and $\vartheta[\mathcal{X},\mathcal{Y}]$ relates the jitter to the input command, such as:

$$\vartheta[\mathcal{X},\mathcal{Y}] = \frac{\mathcal{X}}{N}\left(1-\frac{1}{(1+\beta\mathcal{Y})^2}\right) \tag{28}$$

Later in this paper, Fig. 6 gives a graphical view of this novel jitter formulation for given specifications.

4 Design Guidelines

The analytical developments have shown that the DCO period and its dynamic are strongly dependent on those of the single RO, and more precisely, on the delay introduced by a main inverter, τ_{Dm}. A first definition was given in (8). It is now interesting to expose its technology dependence.

In accordance with [23], C_{se} can be defined as:

$$C_{se} = \frac{5}{2}LW_{seP}C_{ox}(1+\beta\gamma) \tag{29}$$

where L is the MOSFET channel length, W_{seP} is the PMOS (M_{seP}) gate width, C_{ox} is the device oxide capacitance and finally, γ is the applied ratio between M_{seP} and M_{seN} so as to equalize charging and discharging currents. We defined these currents by using the alpha-power law model in saturation regime [21, 29], such as:

$$I_{se} = K_\alpha\frac{W_{seP}}{L}(V_{DD}-V_{TH})^\alpha \tag{30}$$

where K_α, V_{TH} and α are technology dependent parameters. K_α is a drivability factor. V_{TH} is the threshold voltage. α ranges from 1, for deep submicron technology, to 2 for long channel length. This way, every fabrication process is covered. Finally, the current is defined for a gate voltage equals to V_{DD} [22, 30].

Then, τ_{Dm}, the delay introduced by a SE inverter, previously defined in (8), becomes:

$$\tau_{Dm} = L^2 \frac{5\eta C_{ox}(1+\gamma)V_{DD}}{2K_\alpha(V_{DD}-V_{TH})^\alpha} \tag{31}$$

From there, our model integrates all the necessary entries for circuit designing. So that, several design strategies can be derived. Here, we develop one of them for given period range, resolution and fabrication technology.

4.1 Sizing Procedure

We propose to figure out N, L, Q, β and W_{seP} in 4 steps.

4.1.1 Technology Influence

The minimal oscillation period is set by the specifications. From equations (10) and (11) with (31), we demonstrated that:

$$T_{OSCmin} = 2N\tau_{Dm} = NL^2 \frac{5\eta C_{ox}(1+\gamma)V_{DD}}{K_\alpha(V_{DD}-V_{TH})^\alpha} \tag{32}$$

Hence, by setting L at the minimal channel length allowed by the specified technology, the number of stages N can be deduced. A trade-off between L and N may be required.

4.1.2 Period Range

The oscillator output dynamic sets the product of parameters βQ. Indeed, from (11) and (12), we have:

$$\beta Q = \frac{T_{OSCmax}}{T_{OSCmin}} - 1 \tag{33}$$

The insights drawn from the analysis, in section 2, lead to think β as the parameter referring to the DCO period step; while Q finally defines the number of step, and consequently the number of TS cells, for the period sweeping from T_{OSCmax} to T_{OSCmin}.

4.1.3 DCO Resolution

The equation (13), expressing the period dependence to the command input, shows the non-linear relation between $\mathcal{Y}$ and T_{OSC} for this control scheme. The period step, when activating an additional TS inverter, is not constant and varies according to the matrix state. However, regardless of the control strategy set up by the designer, the maximal step is always reached when switching on a TS cell in a column previously inactive. Then, the maximal period decrement, ΔT_{max}, can be calculated as follows:

$$\Delta T_{max} = T_{OSCmax} - T_{OSC}[1,1] = \delta[1,1]T_{OSCmax} \tag{34}$$

which leads to:

$$\beta = \frac{N\Delta T_{max}}{T_{OSCmax} - N\Delta T_{max}} \tag{35}$$

By relying on the result of (33), Q is deduced and the tuning matrix is sized.

4.1.4 W_{seP}, Adjustment Variable

The MOS gate width does not have any influence on the nominal oscillation period nor on the tuning step, at the first order. Nevertheless, it is a key parameter. W_{seP} imposes the DCO power consumption and the jitter magnitude, due to intrinsic noise, exhibited by the structure.

By omitting leakage and short circuit currents, at its highest oscillation frequency, the circuit consumes a maximal electrical power which is defined by:

$$P_{max} = NC_L{V_{DD}}^2\frac{1}{T_{OSCmin}} = \frac{1}{2\eta}V_{DD}I_{se}(1+\beta Q) \tag{36}$$

and from (30), it appears that:

$$P_{max} \propto I_{se} \propto W_{seP} \tag{37}$$

Furthermore, with (16) and (24), we showed that:

$$\sigma_{T_{OSC}}[N,Q] \propto \sigma_{T_{OSCm}} \propto \frac{\sqrt{\mathcal{S}_{i_{nseP}}}}{I_{seP}} \propto \frac{1}{\sqrt{W_{seP}}} \tag{38}$$

To contrast (37) and (38) reveals the trade-off with regard to the choice of W_{seP}. Large transistors allow reducing the intrinsic jitter at the expense of an increase of the electrical power consumption. In practice, the maximal value of one of both parameters is set by the application requirements. The other one is then deduced.

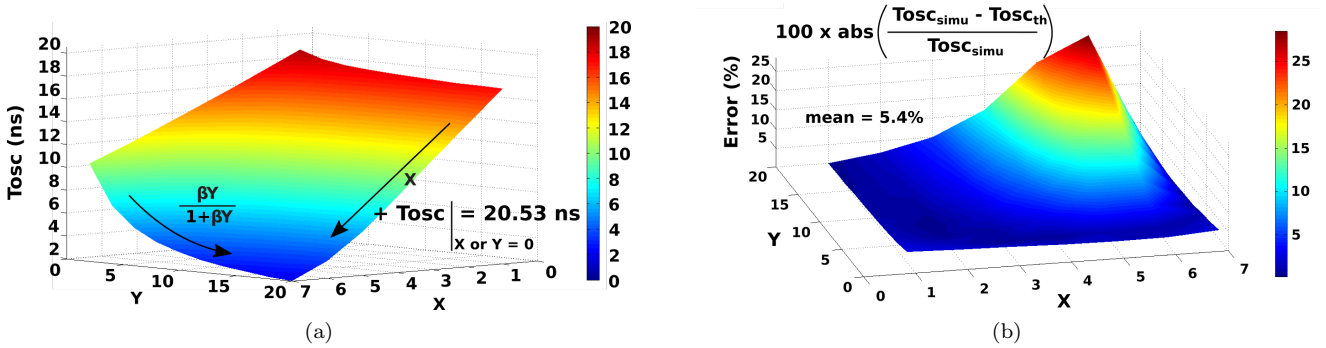


Figure 5: For W_{seP}=64 μm: (a) - Simulation result of the oscillation period as a function of the bi-dimensional command ; (b) - Absolute error between theory and simulation.

4.2 Applicaton to Circuit-S

These guidelines are experienced in designing a first DCO: *Circuit-S* (S for Simulation). For validation purpose, the latter is qualified through simulations in the next section.

Circuit-S is implemented in the STMicroelectronics CMOS 65nm process with HPA-LP MOSFETs (High-Perfomance Analog and Low-Power) provided by the Design-Kit. The device is powered by 1.2 V. It is intended to operate within the oscillation period range of T_{OSCmin} = 2 ns to T_{OSCmax} = 20 ns, with a maximal period step ΔT_{max} = 1 ns, at ambient temperature. Thereby:

1. We set the gate length L at 0.5 μm. Then, the number of stages $N = 7$ is deduced from (32) for T_{OSCmin} = 2 ns.
   We intentionally apply long channel length to MOSFETs. The reader can note that, in section 6, another circuit is designed with the minimal length of this technology node. Both circuits allow validating the model for extreme cases.

2. The ratio T_{OSCmax}/T_{OSCmin} implies that the product βQ equals 9.

3. β should be equal to 0.54, the reader can refer to (35). So as to ease the implementation of $M_{seP,N}$ and $M_{tsP,N}$, at the layout level, β is rounded to 0.5.
   Thence, Q should be equal to 18. We set it to 20 in order to get a safe margin ensuring the operating range.

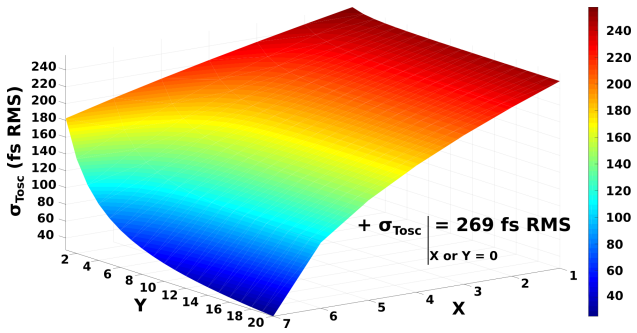


Figure 6: DCO period jitter predicted with equation (24).

4. To highlight the key role played by the reference gate-width, W_{seP}, on the DCO features, we vary it from 4 to 64 μm.

The calculated parameters are summarized in Table 1. The aspect ratios of $M_{seP,N}$ and $M_{tsP,N}$ were determined according to coefficients β and γ. Finally, the dimensions of enabling MOSFETs (i.e., $M_{enP,N}$) were computed for their effective drain-to-source resistance does not exceed a few dozen Ohms, and thereby, minimizing their impact.

Table 1: *Circuit-S* design parameters

Parameter	Value	Inverter	MOSFET	$W_P/W_N/L$ (μm)
Q	20	SE	$M_{seP,N}$	64/20/0.5
β	0.5	TS	$M_{tsP,N}$	32/10/0.5
N	7		$M_{enP,N}$	160/50/0.35
γ	3.2	E/D	not shown	0.18/0.06/0.06

Note that, according to [20], γ is calculated with a view to equalize both falling and rising edge of the generated wave in order to minimize the DCO sensitivity to 1/f noise.

5 Simulation Results for Circuit-S

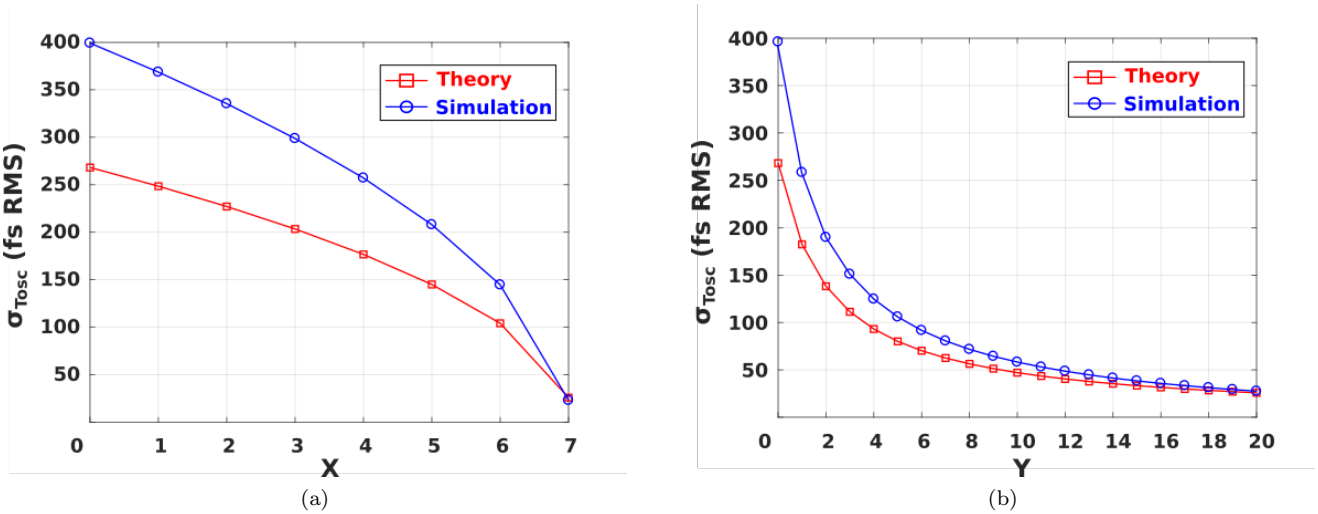
We intend to fulfill two goals in this section. The first one is to evaluate the analytical description built previously. Hence, the formulations of $T_{OSC}[\mathcal{X},\mathcal{Y}]$ and $\sigma_{T_{OSC}}[\mathcal{X},\mathcal{Y}]$ are verified. Then, the trade-off between the power consumption and the period uncertainty is highlighted. Again, the second goal is to provide further knowledges on the DCO behaviour. The simulations have enabled the mapping of the oscillation period as a function of the tuning matrix state. This result suggests remarkable properties regarding the DCO transfer characteristic according to the activation strategy of TS inverters. Therefore, this section ends with a focus on this last point.

All simulations were carried out with Eldo(-RF) - a SPICE-like electronic circuit simulator edited by Mentor Graphics - associated to the BSIM4 MOS transistor model, for Typical-Typical corner.

5.1 Nominal Oscillation Period

Fig. 5a shows the oscillation period as a function of the bi-dimensional command. This result is obtained with a SST (Steady-STate) analysis. The period ranges from 1.93 ns, when all tuning inverters are enabled, to 20.52 ns, for $\mathcal{X} = 0$ and $\mathcal{Y} = 0$. This figure demonstrates that equation (13) adequately describes the period according to both $\mathcal{X}$ and $\mathcal{Y}$.

Fig. 5b presents the relative error between the simulated and the theoretical curves (in absolute terms). A maximal error of 28% is obtained for the combination $\mathcal{X} = 6$ and $\mathcal{Y} = 20$, while the mean error equals 5.4% for a standard deviation of 6.8%. At first glance, the maximal error can seem high. However, the errors with usual equations applied for the RO period calculation can go up to 63% [31,32]. These deviations can be explained by three factors. In first place, the model of delay used in this work is already an approximation. As a comparison, [33] deals with more sophisticated and accurate models. However, they can not be used for hand calculations and/or rapid prototyping. We also suggested that C_L does not depend on the input code while simulations show a variation slightly less than 8%. Finally, we assumed that $M_{seN,P}$ and $M_{tsN,P}$



(a) (b)

Figure 7: For $W_{seP} = 64$ μm: a) - Jitter as a function of $\mathcal{X}$ for $\mathcal{Y} = Q = 20$; b) - Jitter as a function of $\mathcal{Y}$ for $\mathcal{X} = N = 7$.

operate in saturation regime during transitions. However, this hypothesis falls as $\mathcal{X}$ goes up when $\mathcal{Y}$ is close to Q, except for $\mathcal{X} = N$. To illustrate this last point, one can observe the specific case of $\mathcal{X} = 6$ and $\mathcal{Y} = 20$ where the error is maximal. The switching edges of the wave propagating through the ring become sharper as they cross the six fastest delay stages until they reach the last slowest column. The 7^{th} stage is only able to provide the minimal charging current to its output capacitance. Hence, the input transition is much faster than the output one. The major part of the current is provided by the MOSFETs when they operate in the triode region. This configuration is not taken into account in our model. The amplitude of this phenomenon is related to $\mathcal{Y}$ and it takes importance as $\mathcal{X}$ is increased. It disappears when $\mathcal{X} = N$, since every delay stage operates at the same speed.

Still, the mean error remains low. This demonstrates that our hypotheses enable accurate modelling even for hand calculations.

5.2 Period Jitter

Equation (24) expresses the DCO jitter as a function of $\sigma_{T_{OSCm}}$. As a prior step, we extracted the main chain jitter with the SSTNOISE tool implemented in Eldo-RF without the tuning matrix. Its value is 83.76 fs. As a result, the complete DCO structure can be predicted in association to the parameters summarized in Table 1 with respect to the input code. The theoretical characteristic is drawn in Fig. 6.

The prediction is then compared to simulations. In order to highlight the observed deviations, we present the results through the extreme cases. The predicted and simulated curves are plotted in Fig. 7a for $\mathcal{Y} = Q$ while $\mathcal{X}$ varies from 0 to N. This is equivalent to a matrix filling from the left to the right end. In Fig. 7b, $\mathcal{Y}$ ranges from 0 to Q while $\mathcal{X}$ remains equal to N. This is equivalent to a matrix filling from the top to the bottom. The maximal difference between the predicted and simulated results does not exceed 32% for both representations. It is obtained when all the tuning cells are disabled. The error decreases as the number of activated cells increases and is lower than 1% for $\mathcal{X} = N$ and $\mathcal{Y} = Q$. There are several origins of the underestimation of the period jitter described in our model. First, we previously noted the dispersion between the theoretical and simulated DCO period. It affects the jitter calculation. Moreover, we considered that the disabled inverters do not contribute to the noise integrated by the capacitive load C_L. Thus, the formulation of $\sigma_{T_{OSC}}$ in (23) is optimistic. However, the trends and the orders of magnitude are in line with the expectations.

5.3 Power-Jitter Trade-Off

The reduction of the period jitter is at the expense of an increase of the power supply consumption. The reverse is also true. This compromise depends on the reference gate-width, W_{seP}, which has no influence on the oscillation period.

In order to verify this last hypothesis, simulations were performed on the DCO for W_{seP} ranging from 4 to 64 μm, when

$\mathcal{X} = 7$ and $\mathcal{Y} = 20$. Simulation results are plotted in Fig. 8. Of course, one can note that the channel widths of M_{seN} and $M_{tsP,N}$ follow this variation according to coefficients β and γ.

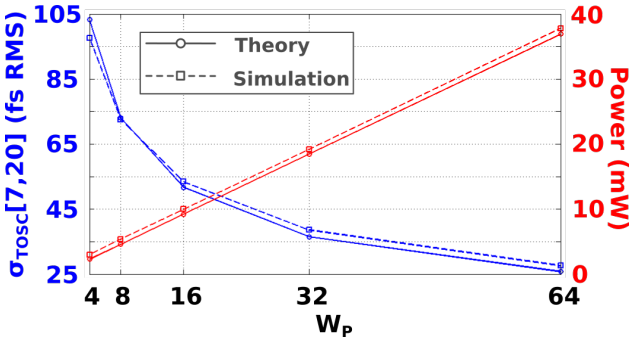


Figure 8: Illustration of the power-jitter trade-off related to W_{seP} for all tuning cells enabled.

Simulations demonstrate that the period changes less than 2.2% while the reference gate-width is multiplied up to sixteen times. Interestingly, they show that the power consumed by the controlled oscillator is directly proportional to W_{seP} while the period uncertainty (i.e. jitter) decreases as the inverse of its square-root in accordance with our expectations.

The minimal jitter value is obtained for $\mathcal{X} = 7$, $\mathcal{Y} = 20$ and $W_{seP} = 64$ μm, when the power consumption is maximal. This was cross-checked with equation (23) in [34]. This publication deals with the minimum achievable phase noise (and jitter) of an oscillator. The concerned equation was computed with our design parameters: $V_{DD} = V_{GS} = 1.2$ V, $V_{TH} = 206$ mV at $T = 25°C$ (from the Design-Kit documentation), at the oscillation frequency $f_0 = 520$ MHz ($T_{OSCmin} = 1.93$ ns) and $P_{min} = 38$ mW (see Fig. 8). By the end, the period jitter, computed with [34], is about 32 fs while our prediction with our equation (24) is 29 fs. Our model again underestimates the period uncertainty but the deviation is only of 10%.

5.4 Control Strategy

Aside from the good agreement between prediction and simulation, the results and, more specifically the 3D representation of T_{OSC} in Fig. 5a, emphasize valuable properties. Indeed, this mapping provides a global view of the oscillation period for any matrix state. To navigate within it by following a direction, or another one, implies different DCO responses. This is shown with Fig. 9. The latter illustrates two activation strategies of TS inverters equivalent to two different trajectories within the 3D mapping.

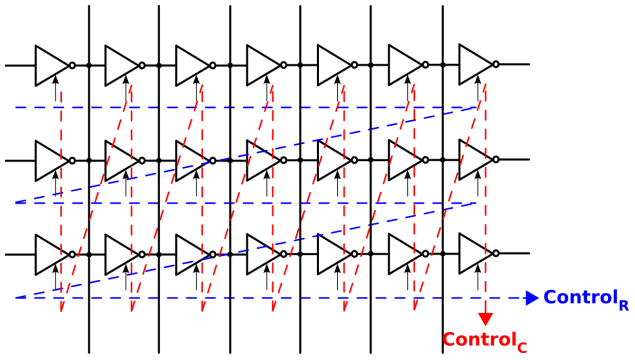


Figure 9: Activation paths of TS inverters following $Control_R$ and $Control_C$ strategies.

On the one hand, $Control_R$ consists of enabling the next TS cell just on the right, in the same row. When a row is fully active, the operation continues with the activation of the first TS inverter at the left end of the following row, and so on. It is equivalent to browse the map following the $\mathcal{X}$-axis from 0 to 7. When $\mathcal{X} = 7$ is reached, the operation is renewed with the immediately higher value of $\mathcal{Y}$. On the other hand, with $Control_C$, the next tuning cell which is enabled is below, in the same column. When a column is fully active, the next one is started. This path is equivalent to navigate through the map by following the $\mathcal{Y}$-axis from 0 to 20 and to increment $\mathcal{X}$ at the next iteration. The both control strategies lead to different

DCO transfer characteristic presented in Fig.10. It is worth noting that for implementing one of these tuning strategies, the simple AND operation of X and Y is not applicable and, an adjustment of the activation circuitry is required.

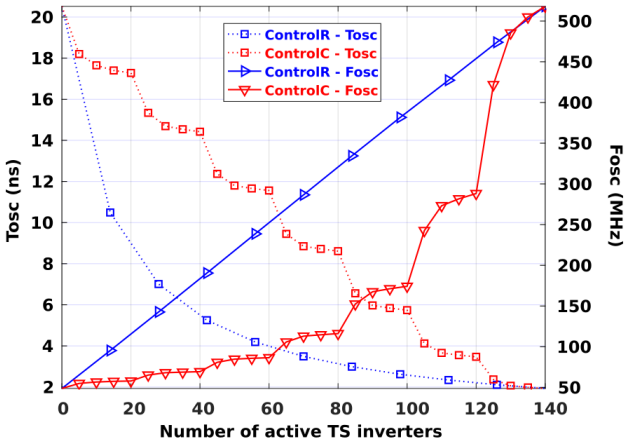


Figure 10: DCO Period and frequency responses, as a function of the number of active tuning cells, and for $Control_R$ and $Control_C$.

Regarding $Control_R$, the oscillation period is inversely proportional to the number of active tuning cells. Even more interesting is that the DCO output frequency grows linearly with the activation of TS inverters. It is especially suitable for designing an ADPLL [14].

$Control_C$ shows different properties. The frequency response does not show as much interest. However, the oscillation period has a quasi-linear decrease with the activation of the next columns. In addition, the modulation of the delay introduced by each stage, when turning-on TS inverters in a same column, is highlighted here. These features are particularly appropriate to All-Digital Delay-Locked Loops and are reported in [35].

Having said that, $Control_R$ is the most widely used strategy, see [9,14–16]. Therefore, the study continues with *Circuit-M* (M for Measurement) whose tuning strategy relies on $Control_R$.

6 Experimentations on Circuit-M

Circuit-M was manufactured with LVT-LP (Low-V_{TH} and Low-Power) MOSFETs provided by the STMicroelectronics 65nm Design-Kit. A die microphotograph of the fabricated chip is given in Fig. 11.

Circuit-M represents an interesting study case because the SE and TS inverters do not have the same channel-length. Therefore, the established model is revised at the beginning of this section. Moreover, in opposition to *Circuit-S*, SE inverters of this chip were implemented with the minimal channel-length allowed by the technological process. Thus, short-channel effects are included in experimental results.

One can note that the circuit was fully described in [16] as a DCO featuring a linear transfer characteristic for the output frequency versus the input code. Then, in this section, for convenience, we focus on the output frequency instead of the oscillation period. As an extra contribution to [16], we provide the theory demonstrating the published simulation results and the measurement results as a proof. Finally, the jitter is analyzed.

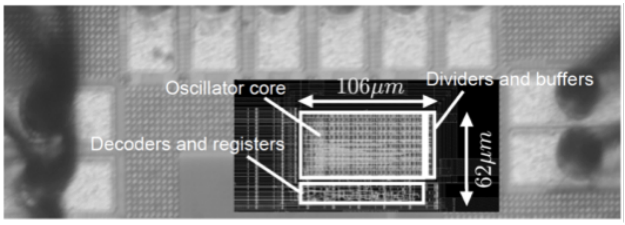


Figure 11: *Circuit-M* die microphotograph.

6.1 Brief Circuit Description

Circuit-M is a 10-bit DCO. The chip operates within the frequency range [1.1-2.8 GHz] at ambient temperature. Its core is built on the association of a 7-stages ring oscillator and a regular array of 266 switchable elements ($N = 7$ and $Q = 38$). In this matrix, 11 cells are included for trimming purpose in case of PVT (Process, Voltage, Temperature) variations and are activated with a dedicated control scheme. The 255 remaining TS inverters serve for the frequency coarse tuning and are individually enabled through the 8 most significant bits of the input word. In addition, both least significant bits allow the frequency fine tuning by enabling a single TS inverter placed on the 2^{nd}, the 4^{th} and the 6^{th} columns.

For the following calculations, the design parameters related to *Circuit-M* are summarized in Table 2 (from [16]), where SE, CT, FT and TR stand for Single-Ended, Coarse-Tuning, Fine-Tuning and TRimming inverters, respectively.

Table 2: *Circuit-M* design parameters

Parameter	Value	Cell Type	# of cells	MOSFET $W_P/W_N/L$ (μm)
V_{DD}	1.1 V	SE	7	26.4/18.72/0.06
# of bits	10	CT	255	2.4/1.6/0.12
N	7	FT	3	0.56/0.4/0.12
Q	38	TR	11	2.4/1.6/0.12

6.2 Revised Model

For the sake of simpicity, at least in the first round, we neglect the influence of the FT inverters for two reasons. Firstly, there are only 3 cells, in comparison, there are 266 CT and TR cells. Secondly, the gate area of a FT inverter represents slightly less than a quarter of that of a single CT or TR cell. As a consequence, their contribution to the total stage capacitance C_L can be neglected in comparison to those of other devices. Finally, by referring on the MOSFET aspect ratios summarized in Table 2, the reader can conclude that the current provided to C_L by a CT or TR inverter is five times greater than the one drawn with a FT inverter. Thus, it can be omitted for calculating the stage total current, I_{Si}.

These assumptions lead us to express C_L such as :

$$C_L = C_{se} + QC_3 = C_{se}(1 + Q\mathcal{R}_{GA}) \tag{39}$$

with $\mathcal{R}_{GA}$ as the ratio of gate-area between a TS inverter (CT or TR) and the SE one. This new parameter distinguishes (39) from (6). It equals :

$$\mathcal{R}_{GA} = \frac{L_3(W_{3P} + W_{3N})}{L_{se}(W_{seP} + W_{seN})} \tag{40}$$

And $\mathcal{Y}$ inverters are enabled for the i^{th} stage, C_L is (dis-)charged with I_{Si} described as in (41):

$$I_{Si}[\mathcal{Y}] = I_{se} + \mathcal{Y}I_3 = I_{se}(1 + \mathcal{Y}\widetilde{\beta}) \tag{41}$$

In this last equation, $\widetilde{\beta}$ relates the aspect ratio of a CT (or TR) inverter to that of a SE one. Its formulation is given in equation (42) where, as previously, we assume that charging and discharging current are equals.

$$\widetilde{\beta} = \frac{W_{3P}}{L_3}\frac{L_{se}}{W_{seP}} = \frac{W_{3N}}{L_3}\frac{L_{se}}{W_{seN}} \tag{42}$$

Having defined C_L and I_{Si} allows expressing the operating range, the frequency resolution and the expected jitter of *Circuit-M*.

6.2.1 Oscillation Frequency

The chip oscillates at its minimal frequency when all tuning and trimming inverters are off (i.e., $I_{Si}[0] = I_{se}$). Hence, we have:

$$\begin{aligned} F_{OSCmin,0} &= \frac{I_{se}}{2\eta N V_{DD} C_{se}} \frac{1}{1+Q\mathcal{R}_{GA}} \\ &= F_{OSCm} \frac{1}{1+Q\mathcal{R}_{GA}} \end{aligned} \tag{43}$$

and similarly to the previous study case, F_{OSCm} stands for the oscillation frequency of the main chain alone (matrix disconnected). The reader can observe the particular notation used for the indices of F_{OSC}, in the above equation, it takes into account the conditions: "0" for all TR inverters turned off.

At the other end, the maximal oscillation frequency is reached when all tri-state inverters are activated (i.e., $\mathcal{Y} = Q$ for each stage), it yields:

$$F_{OSCmax,11} = F_{OSCm} \frac{1+Q\widetilde{\beta}}{1+Q\mathcal{R}_{GA}} \tag{44}$$

Finally, the coarse frequency step, ΔF_C, is obtained by dividing the calculated range by the total number of TS cells. The calculation results in:

$$\Delta F_C = \frac{F_{OSCmax,11} - F_{OSCmin,0}}{NQ} = \frac{\widetilde{\beta}}{N} F_{OSCmin,0} \tag{45}$$

6.2.2 Period Variance

Expressing the period jitter as a function of the input code, for this control scheme, requires to include the modulo operator in analytical developments. It allows taking into account the progressive filling of a row before activating the TS inverters of the next one.

So as to obtain a fairly simple equation, we propose an alternative approach for quicker calculations by designers. It consists to compute the period jitter only for fully-enabled rows. It is equivalent to estimate the period jitter for each seven increments. In this way, the calculations are very similar to those presented for *Circuit-S* with X_i always equal to 1.

By relying on (22), the delay variance of a stage is:

$$\begin{aligned} {\sigma_{\tau_{Di}}}^2[\mathcal{Y}] &= \frac{1}{2} \frac{\mathcal{S}_{i_{nseP}}}{{I_{seP}}^2} \tau_{Dm} \frac{1+Q\mathcal{R}_{GA}}{(1+\widetilde{\beta}\mathcal{Y})^2} \\ &= {\sigma_{\tau_{Dm}}}^2 \frac{1+Q\mathcal{R}_{GA}}{(1+\widetilde{\beta}\mathcal{Y})^2} \end{aligned} \tag{46}$$

where ${\sigma_{\tau_{Dm}}}^2$ is still related to the delay variance of the SE inverter. Thence, the period variance is directly given by:

$$\begin{aligned} {\sigma_{T_{OSC}}}^2[\mathcal{Y}] &= 2N {\sigma_{\tau_{Dm}}}^2 \frac{1+Q\mathcal{R}_{GA}}{(1+\widetilde{\beta}\mathcal{Y})^2} \\ &= {\sigma_{T_{OSCm}}}^2 \frac{1+Q\mathcal{R}_{GA}}{(1+\widetilde{\beta}\mathcal{Y})^2} \end{aligned} \tag{47}$$

with ${\sigma_{T_{OSCm}}}^2$ as the period variance of the SE ring oscillator.

6.2.3 Expected Results

We simulated the RO (matrix disconnected). Its natural oscillation frequency F_{OSCm} equals 7.1 GHz with a period jitter, $\sigma_{T_{OSCm}}$, of 2.99 ps. In this way, from the dimensions summarized in Table 2 and the relations established within the previous two subsections, we predicted the frequency and jitter characteristics of *Circuit-M*. The numerical application is compared with the simulation results of the complete DCO structure in Table 3. Note that, ΔF_F stands for the fine frequency step. It is computed by dividing by 4 the value of ΔF_C, according to the MOSFET geometrical factors summarized in Table 2.

Table 3: Expected Performances of *Circuit-M*

	Parameter	Prediction	Simulation
Frequency (MHz)	$F_{OSCmin,0}$ ▼	459.09	611.89
	$F_{OSCmin,11}$ ▲	491.97	-
	$F_{OSCmax,0}$ ▼	1220.76	1258.19
	$F_{OSCmax,11}$ ▲	1252.06	-
	ΔF_C	2.98	2.53
	ΔF_F	0.74	0.63
Jitter (ps)	$\sigma_{T_{OSC}min,0}$	3.17	-
	$\sigma_{T_{OSC}max,11}$	8.32	-

▼ : TR cells are off
▲ : TR cells are on

6.3 Measurement Results

The modelling work presented throughout this paper is finally assessed by measurements on the fabricated chip, which are subsequently compared to the expectations.

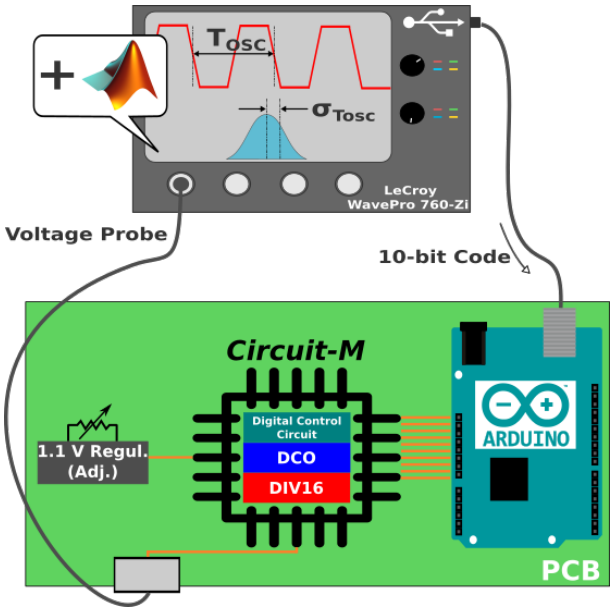


Figure 12: Experimental setup for the characterization of *Circuit-M*.

6.3.1 Setup

It is illustrated by Fig. 12. The designed DCO is embedded on a specific Printed Circuit Board (PCB). It includes an adjustable voltage regulator so as to power the controlled oscillator. The 10-bit input code is generated from a Matlab script which runs on the Digital Sampling Oscilloscope (DSO) Teledyne LeCroy WavePro 760Zi. The command is sent via the USB interface to the Arduino Nano microcontroller, operating as a serial-to-parallel data converter, in order to drive *Circuit-M*. The same DSO serves as the measuring instrument and probes the DCO output after a clock division by a factor of 16. The frequency division is required here to not exceed the frequency limitation of the I/O pads (i.e., 280 MHz in our case).

6.3.2 Frequency Characteristics

Fig. 13 shows the DCO transfer characteristic obtained by measurement, simulation and theory, when the typical supply voltage V_{DD} = 1.1 V is applied. The frequency measured at the PCB output is multiplied by 16 so as to reflect the DCO

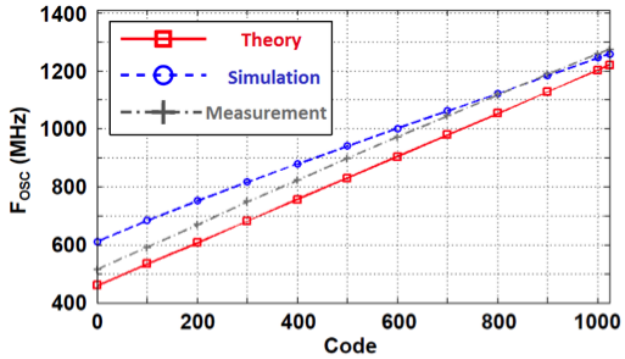


Figure 13: Comparison between the measured, the simulated (post-layout) and the theoretical DCO transfer characteristic, for $V_{DD} = 1.1$ V.

output. Note that the curve associated to the measurements is the average over 10 instances of *Circuit-M*. By taking the measurements as the reference, the discrepancy with theoretical calculations never exceeds 8.2%, with a quasi-constant shift of 50 MHz. We attribute this to process variations observed over the 10 chips. Furthermore, for $F_{OSCmax,0}$, it appears that the simulation result is more faithful to the reality of the chip than the theory. However, for $F_{OSCmin,0}$, the simulation shows a deviation of more than 22% compared to the measurement.

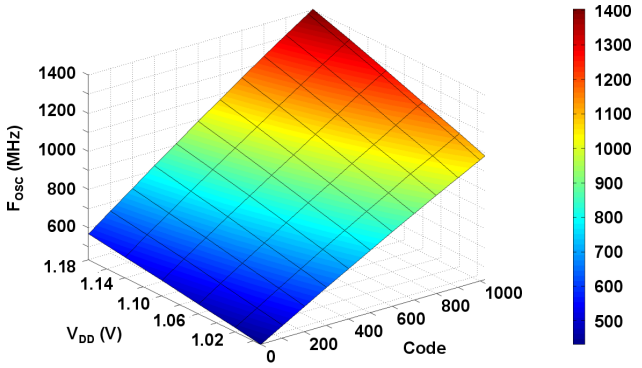


Figure 14: 3D graphic of *Circuit-M* oscillation frequency tuned by the input code and the supply voltage V_{DD}.

Fig. 14 plots the results of our experimental investigation concerning the DCO sensitivity to V_{DD}. Through the adjustable voltage regulator, the supply voltage is varied from 992 mV to 1.18 V. The illustration denotes the increase of the frequency range covered by the oscillator as V_{DD} is increased. The revised model demonstrated that F_{OSCmin}, F_{OSCmax}, ΔF_C, and thus ΔF_F, are proportional to F_{OSCm}. The natural oscillation frequency of the RO is described by the inverse of (11). Then, F_{OSCm} grows with V_{DD} and justifies the observed behaviour of the DCO frequency range.

6.3.3 Period Drift

This last feature was measured thanks to the jitter analysis tool equipping the DSO : the WPZi-JITKIT. It was done in accordance with the JEDEC standard JESD65B [36]. One million periods are acquired. The value of jitter is then stored after 10.000 computations on this set of periods. This experiment is repeated 10 times for various input codes. Finally, the average values and standard deviations are graphed in Fig. 15, in term of the input code and for $V_{DD} = 1.1$ V. The predicted jitter is superimposed on measurement results.

In a similar way to the study on *Circuit-S*, the Fig. 15 shows that our model underestimates the DCO jitter. In this case, the mean deviation between the measurement and the prediction is about 0.81 ps while the maximal gap is observed at 1.52ps for *Code* equal to 100.

Furthermore, it seems that our measurement protocol shows its limits for an input *Code* above 800 while the jitter is decreasing and close to its minimal value. This outcome was partially expected. First, the measurement tool introduces a jitter floor which is approximately 2 ps [37]. In addition, the experimental data include the jitter due to the on-chip buffers placed at

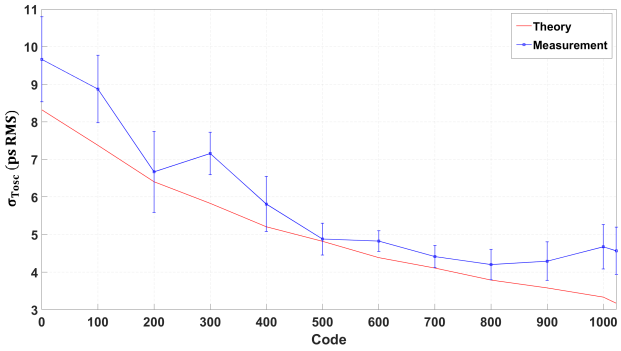


Figure 15: Measured and predicted jitter for *Circuit-M* with respect to the input code.

the DCO output, plus the asynchronous clock divider and pads contributions [38,39]. Unfortunately, at this stage, we are not able to quantify experimentally the impact of each of these components. Moreover, we suspect possible parasitic contributors related to the off-chip measurements.

Anyway, the trend between the jitter measurement and our (revised) model are in agreement and finally reinforce the validity of the proposed model.

7 Conclusion and Perspectives

This paper proposes a comprehensive analytical study of the tri-state inverter based DCO. This is achieved by expressing its oscillation period and the associated uncertainty, with respect to the input code, by relying on properties of a classic SE RO. These derivations yield the elaboration a design guide. Relating the design steps of the DCO to those of the well-known RO enables either a fast implementation from digital standard cells or fast optimization with a (full-)custom design for more stringent specifications. To this end, two circuits are presented and validate our assumptions: *Circuit-S* and *Circuit-M*, with simulations and measurements, respectively. Both are designed with the STMicroelectronics CMOS 65nm process.

Circuit-S showed the developed model is accurate enough to predict the oscillation period with a mean relative error of 5.4% compared to electrical simulations. Furthermore, the period jitter can be predicted with a maximal discrepancy of 32% compared to simulations. The jitter formulation as a function of the input code is one of our contributions to the state-of-the-art. At our best knowledge, this is the first initiative to equate the period uncertainty according to the DCO state.

The measurements performed with *Circuit-M* support our analysis and results. Contrary to *Circuit-S*, this chip is built from MOSFETs sized at the minimal channel length. Hence, *Circuit-M* is subject to short-channel effects. As a reminder, the transistors of *Circuit-S* are almost eight times longer than those of *Circuit-M*. For the latter, the measurements demonstrate that our assumptions and model remain valid. A maximal gap of 8.2% between the predicted oscillation frequency and the measured one and a mean deviation of 0.81 ps between the predicted and measured jitter are observed.

In perspective to this work, we plan to address two main points. First, the jitter measured with *Circuit-M* should be studied with more details to quantify the contribution due to each part (out of the DCO itself), even if the trend is well-respected. It could require the fabrication of a new test-chip. Finally, we intend to integrate the proposed design procedure within an automatic design tool. This work is actually in progress.

Acknowledgment

This work was supported by French National Agency of Research under HERODOTOS project (grant number ANR- 10-SEGI-014-01). The Authors thank the CMP (Circuits Multi Projet) team for valuable support in silicon implementation of the circuit.

The authors also would like to thank Dr. F. Kölbl for his help on the text.

References

[1] R.B. Staszweski, "State-of-the-Art and Future Directions of High-Performance All-Digital Frequency Synthesis in Nanometer CMOS", IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 58, no. 7, pp. 1497-1510, 2011.

[2] A. Rylyakov, J. Tierno, D. Turker, J.O. Plouchart, H. Ainspan, and D. Friedman, "A Modular All-Digital PLL Architecture Enabling Both 1-to-2GHz And 24-to-32GHz Operation In 65nm CMOS", IEEE International Solid-State Circuits Conference (ISSCC), pp. 516-632, 2008.

[3] V. Kratyuk, P. Hanumolu, U.K. Moon, and K. Mayaram, "A Design Procedure for All-Digital Phase-Locked Loop Based on a Charge-Pump Phase-Locked Loop Analogy", IEEE Transaction on Circuits And Systems - II, vol. 54, no. 3, pp. 247-251, 2007.

[4] Y.H. Liu, J. Van Den Heuvel, T. Kuramochi, B. Busze, P. Mateman, V.K. Chillara, B. Wang, R. B. Staszewski, and K. Philips, "An Ultra-Low Power 1.7-2.7 GHz Fractional-N Sub-Sampling Digital Frequency Synthesizer and Modulator for IoT Applications in 40 nm CMOS", IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 64, no. 5, pp. 1094-1105, 2017.

[5] M. Shakir, M. Abdulaziz, P. Lu and P. Andreani, "A Mixed Mode Design Flow for Multi GHz ADPLLs", IEEE Nordic Circuits And Systems Conference (NORCAS) : NORCHIP, pp. 1-4, 2011.

[6] I. L. Syllaios and P. T. Balsara, "Linear Time-Variant Modeling and Analysis of All-Digital Phase-Locked Loops", IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 59, no. 11, pp. 2495-2506, 2012.

[7] J. Prinzie, J. Christiansen, P. Moreira, M. Steyaert and P. Leroux, "Comparison of a 65 nm CMOS Ring- and LC-Oscillator Based PLL in Terms of TID and SEU Sensitivity", IEEE Transactions on Nuclear Science, vol. 64, no. 1, pp. 245-252, 2017.

[8] E. Hegazi, J. Rael, Jacob, and A. Abidi, "Designers Guide to High Purity Oscillators", Springer, 2005.

[9] T. Olsson, and P. Nilsson, "A Digitally Controlled PLL for SoC Applications", IEEE Journal of Solid-State Circuits, vol. 39, no. 5, pp. 751-760, 2004.

[10] T.Y. Hsu, C.C. Wang and C.Y. Lee, "Design and analysis of a portable high-speed clock generator", IEEE Transactions on Circuits and Systems II, vol. 48, no. 4, pp. 367-375, 2001.

[11] C.C. Chung and C.Y. Lee, "An all-digital phase-locked loop for high-speed clock generation", IEEE Journal of Solid-State Circuits, vol. 38, no. 2, pp. 347-351, 2003.

[12] J. Cortadella, M. Lupon, A. Moreno, A. Roca and S. S. Sapatnekar, "Ring Oscillator Clocks and Margins", IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC), pp. 19-26, 2016.

[13] T. Seong, Y. Lee, S. Yoo and J. Choi, "A 242dB FOM and 75dBc-reference-spur ring-DCO-based all-digital PLL using a fast phase-error correction technique and a low-power optimal-threshold TDC", IEEE International Solid - State Circuits Conference (ISSCC), pp. 396-398, 2018.

[14] J. Tierno, A. Rylyakov, and D. Friedman, "A Wide Power Supply Range, Wide Tuning Range, All Static CMOS All Digital PLL In 65n SOI", IEEE Journal of Solid-State Circuits, vol. 43, no. 1, pp. 42-51, 2008.

[15] B.G. Jeon, Y. Moon, and T.W. Ahn, "A Study on 11 MHz-1537 MHz DCO Using Tri-State Inverter for DAB Application", IEEE Technical Conference, pp. 1-5, 2009.

[16] E. Zianbetov, F. Anceau, M. Javidan, D. Galayko, E. Colinet, and J. Juillard, "A Digitally Controlled Oscillator in a 65-nm CMOS Process for SoC Clock Generation", IEEE International Symposium on Circuits And Systems (ISCAS), pp. 2845-2848, 2011.

[17] M. Terosiet, S. Feruglio, D. Galayko, and P. Garda, "An Analytical Model Of The Oscillation Period For Tri-State Inverter Based DCO", IEEE International Conference on Microelectronics (ICM), pp. 1-5, 2011.

[18] D. Lee, K. Kim, Y. Min, J. Park and S. Kim, "A Jitter and Power Analysis on DCO", in IEEE Transactions on Circuits and Systems II, vol. 58, no. 9, pp. 560-564, 2011.

[19] J.A. McNeill and D. Ricketts, "The Designer's Guide to Jitter in Ring Oscillators", Springer, 2009.

[20] A. Hajimiri, S. Limotyrakis and T.H. Lee, "Jitter and Phase Noise in Ring Oscillators", IEEE Journal of Solid-State Circuits, vol. 34, no. 6, pp. 790-804, 1999.

[21] M. Alioto and G. Palumbo, "Impact of Supply Voltage Variations on Full Adder Delay: Analysis and Comparison", IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 14, no. 12, pp. 1322-1335, 2006.

[22] E. Morifuji, T. Yoshida, H. Tsuno, Y. Kikuchi, S. Matsuda, S. Yamada, T. Noguchi and M. Kakumu, "New Guideline of Vdd and Vth Scaling for 65nm Technology and Beyond", IEEE Symposium on VLSI technology, Digest of technical paper, pp. 164-165, 2004.

[23] R.J. Baker, "CMOS Circuit Design, Layout, and Simulation", John Wiley and Sons, 2005.

[24] B. Leung, "Design and Analysis of Saturated Ring Oscillators Based on the Random Mid-Point Voltage Concept", IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 21, no. 8, pp. 1554-1557, 2013.

[25] S. Robson, B. Leung and G. Gong, "Truly Random Number Generator Based on a Ring Oscillator Utilizing Last Passage Time", IEEE Transactions on Circuits and Systems II, vol. 61, no. 12, pp. 937-941, Dec. 2014.

[26] J. A. McNeill, "Jitter in Ring Oscillators", IEEE Journal of Solid-State Circuits, vol. 32, no. 6, pp. 870-879, 1997.

[27] D.C. Lee, "Analysis of Jitter in Phase-Locked Loops", IEEE Transactions on Circuits and Systems II, vol. 49, no. 11, pp. 704-711, 2002.

[28] A. Abidi, "Phase Noise and Jitter in CMOS Ring Oscillators", IEEE Journal of Solid-State Circuits, vol. 41, no. 8, pp. 1803-1816, 2006.

[29] T. Sakurai, and A. Newton, "Alpha-Power Law MOSFET Model and Its Applications to CMOS Inverter Delay and Other Formulas", IEEE Journal of Solid-State Circuits, vol. 25, no. 2, pp. 584-594, 1990.

[30] J. Rabaey, "Low Power Design Essentials", Springer, 2009.

[31] S. Docking, and M. Sachdev, "A Method to Derive an Equation for the Oscillation Frequency of a Ring Oscillator", IEEE Transaction on Circuits And Systems - I, vol. 50, no. 2, pp. 259-264, 2003.

[32] M. Alioto, and G. Palumbo, "Oscillation Frequency in CML and ESCL Ring Oscillators", IEEE Transaction on Circuits And Systems - I, vol. vol. 48, no. 2, pp. 210-214, 2001.

[33] B. Leung, "A Switching-Based Phase Noise Model for CMOS Ring Oscillators Based on Multiple Thresholds Crossing", IEEE Transactions on Circuits and Systems I, vol. 57, no. 11, pp. 2858-2869, 2010.

[34] R. Navid, T.H. Lee and R.W. Dutton, "Minimum achievable phase noise of RC oscillators", in IEEE Journal of Solid-State Circuits, vol. 40, no. 3, pp. 630-637, 2005.

[35] B.I. Abdulrazzaq, I. A. Halin, S. Kawahito, R.M. Sidek, S. Shafie and N.A. Md. Yunus, "A review on high-resolution CMOS delay lines: towards sub-picosecond jitter performance", SpringerPlus, vol. 5, no. 1, pp. 1-32, 2016.

[36] A. Sridhar and G. Ayala, "Time-Domain Jitter Measurement Considerations for Low-Noise Oscillators", Texas Instruments, Application Report, 2015. [online]. Available : http://www.ti.com/lit/an/snaa285/snaa285.pdf

[37] Teledyne LeCroy, Inc., "WavePro 7 Zi-A Series, 1.5 - 6 GHz", 2017. [online]. Available: http://cdn.teledynelecroy.com/files/pdf/wavepro_7_zi-a_datasheet.pdf.

[38] S. Levantino, L. Romano, S. Pellerano, C. Samori and A.L. Lacaita, "Phase Noise in Digital Frequency Dividers", IEEE Journal of Solid-State Circuits, vol. 39, no. 5, pp. 775-784, 2004.

[39] A.M. Fahim, "Jitter analysis of digital frequency dividers in communication systems", IEEE International Frequency Control Symposium and Exposition, pp. 169-173, 2004.