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Radiation Hardening Efficiency of Gate Sizing and Transistor Stacking based on Standard Cells

Y. Q. Aguiar[a,*], F. Wrobel[a], S. Guagliardo[a], J-L. Autran[b], P. Leroux[c], F. Saigné[a], A. D. Touboul[a] and V. Pouget[a]

[a] Institut d'Electronique et des Systèmes, *University of Montpellier, Montpellier, France*
[b] Institut Materiaux Microelectronique Nanoscience de Provence, *Aix-Marseille University, Marseille, France*
[c] Advanced Integrated Sensing Lab, *KU Leuven University, Leuven, Belgium*

Abstract

Soft error mitigation schemes inherently lead to penalties in terms of area usage, power consumption and/or performance metrics. This work provides a radiation hardening efficiency analysis of two possible selective node hardening based on standard cells: Gate Sizing and Transistor Stacking. The impact on the Single-Event Transient cross-section, layout area and leakage current is discussed. The results indicate that both techniques provide the same area overhead and high efficiency for low particle linear energy transfer. Further, although transistor stacking exhibits lower static power consumption, gate sizing still presents the best trade-off between area, performance and reliability.

1. Introduction

Advances on transistor technology allowed the design of ever increasing complex integrated circuits in the past years. Along with the great achievements on reduction of power consumption and increase in performance, new challenges are faced when considering deeply-scaled technologies. Pronounced process variability, aging and radiation effects are recurrent design challenges with growing importance [1-5]. Integrated circuits are increasingly susceptible to single energetic particle hits and it may experience destructive or non-destructive effects. Single-Event Latchup (SEL) occurs when a particle strike triggers the parasitic transistor in the PNPN structure inherently present in the CMOS circuits and it can be a destructive effect [6]. When the energetic particle hits a sensitive region of transistors from a sequential logic element and it deposits enough charge to upset the circuit, a Single-Event Upset (SEU) is observed as a bit flip. Also, combinational logic circuits are susceptible to Single-Event Transient (SET) effects which appear as parasitic transient currents generated from the particle interaction into the drain electrodes of transistors in the off-state. This is not an exhaustive list of effects known as Singe-Event Effects (SEE) [7]. Radiation Hardening by Design (RHBD) techniques have been developed to cope with radiation effects on electronic circuits at different levels of abstraction ranging from circuit layout to system and software design [8-13]. These techniques can provide mitigations from fault masking to detection and recovery of the system. However, traditional RHBD techniques rely on hardware, time or information redundancy, implying an increase in area, power and delay. Additionally, at advanced technology nodes, the charge sharing effect induced by closely spaced transistor nodes reduces the efficiency of well-known hardening techniques as the dual interlocked storage cell (DICE) designs and error-correcting codes (ECCs) [5]. Circuit designers need to find the best trade-off between performance and reliability when considering RHBD techniques [12]. Accordingly, the goal of this work is to assess the radiation robustness efficiency provided by gate sizing and transistor stacking based on standard cells. A layout-based prediction methodology is used to calculate the SET cross-section and to measure the transient pulse width through Monte Carlo simulations.

This paper is organized as follows. A review on radiation hardening by design techniques, especially gate sizing and transistor stacking, is discussed in Section 2. The layout-based SEE prediction methodology is presented in Section 3. Section 4 presents the results of the power consumption, layout area and radiation analysis on the RHBD designs. Section 5 summarizes this work.

* Corresponding author. aguiar@ies.univ-montp2.fr

2. Radiation Hardening based on Standard Cells

Radiation hardness of electronics systems can be enhanced through modifications on fabrication process or by design. Besides the higher cost, Radiation Hardening by Process (RHBP) techniques are available for older transistor technologies leading to higher power consumption and lower performance compared to current commercially available technology nodes. On the other hand, RHBD techniques can profit from the improvements on power, performance and reduced area acquired by state-of-the-art commercially available CMOS technology process [14]. One well established RHBD layout technique to reduce the leakage current induced by total ionizing dose effects is to use edgeless transistors, also known as Enclosed Layout Transistors (ELT) [15, 16]. Triple Modular Redundancy (TMR) approach is another well-known and widely used fault tolerant technique that provides robustness to SET and SEU [17].

Radiation robustness can also be obtained through reliability-aware logic and physical synthesis in semi-custom designs based on standard-cell methodology [18-21]. In other words, it is possible to harden a circuit by selectively using logic gates that minimize the SET generation or propagation in the most vulnerable nodes of a complex VLSI design. In [18], three selective node hardening techniques were evaluated in the logic synthesis of different ISCAS85 benchmark circuits. It was shown that hardening techniques can be very effective when applied at standard cell based VLSI designs. During physical synthesis, hardening strategies can be explored in the cell placement to avoid charge sharing effects or to promote pulse quenching effects in electrically related combinational circuits [19-21]. Du et al. [20] demonstrated that, as feature size shrinks, cell placement has a stronger impact on the soft error vulnerability of complex VLSI due to the multi-node collection process. Accordingly, it is imperative to study selective node hardening strategies suitable to be integrated into standard cell based design methodologies. In this work, the usage of gate sizing and transistor stacking is explored using NAND and NOR gates from a standard-cell library.

2.1. Gate Sizing

The feature sizes of transistors, i.e. the length (L) and the width (W) of the device channel, directly influence the performance of the circuits. Transistor or gate sizing is widely used to improve delay/power trade-offs in different applications [22, 23]. By changing the W/L ratios of transistors, the nodal capacitance and drive strength of the circuit are affected, leading to changes in the power consumption and propagation delay. As radiation-induced transient currents are dependent on the drive strength and nodal capacitance of the circuit, gate sizing has also been used to improve the radiation robustness of VLSI circuits [24]. However, besides increasing the capacitance and restoring current, upsizing transistors increases the sensitive area and it can possibly worsen the reliability of the circuit by increasing the particle incidence probability. In standard cell libraries, the cells are available with different drive strengths, starting from the minimum sized implementation denoted by X1, and increasing discretely to drive strength 2 (X2), drive strength 4 (X4) and so on. Due to the high regularity of circuit layout of standard cells and drive strengths, the gate sizing using standard-cell methodology is a discrete process. In [25], inverter, NAND and NOR logic gates from a 90 nm RHBD cell library were characterized under heavy ion and high energy protons irradiations. Different drive strengths available in the cell library were evaluated. Results show that upsizing the cells was only efficient on reducing the SET cross-section for the inverter and NOR logic gates. In the case of the NAND2_X2 cell, the larger sensitive area dominates the SET sensitivity over the increased nodal capacitance and restoring current [25]. On the other hand, FinFET-based circuits using NAND and NOR gates have shown similar SET sensitivity in [26]. The symmetric sizing of the PFET and NFET transistors, provided by the strain engineering and width quantization, has led to a symmetrical collection drain area and restoring current and hence a similar soft error susceptibility for both circuits.

2.2. Transistor Stacking

Another alternative to gate sizing is to use transistor stacking to increase the nodal capacitance [18]. Stacking devices is a well-known RHBD technique used for SEU immunity in SOI designs [27-28]. Due to the SOI structure, the shallow trench isolation (STI) and buried oxide (BOX) prevents charge sharing between the stacked transistors improving the overall soft error susceptibility drastically [27]. Accordingly, a single particle strike must deposit sufficient charge in both stacked devices for an SEU/SET to be observed. Unlike SOI technology, bulk devices experience charge sharing but it still benefits from the increased nodal capacitance provided by the stacked devices. Additionally, transistor stacking provides less leakage current than a same sized single transistor as shown in [29]. Also, in [18], transistor stacking outperformed

gate sizing in terms of power consumption while maintaining similar area efficiency. Although the power saving compared to gate sizing, connecting transistors in series in the stacking technique increases the effective (dis)charging resistance leading to increase in delay. Taking into account the layout effects on the deposition and charge collection process, this work aims to investigate the radiation robustness efficiency of gate sizing and transistor stacking hardening technique using a layout-based SEE prediction methodology. Aiming at low power reliable applications, the analysis focuses on the trade-off between power consumption and radiation effects. And, more importantly, the input dependence of each technique is provided and it can be used to improve the radiation reliability of hardened standard cell libraries while reducing its area, power and performance overhead.

3. Methodology

To accurately analyze the SET sensitivity of digital circuits, it is highly recommended to adopt a multi-scale and multi-physics approach taking into consideration all aspects from the particle interaction physics to the circuit layout design [30]. Further, to evaluate the effectiveness of RHBD techniques in deeply-scaled technologies, it is imperative to address emerging effects such as bipolar amplification and charge sharing effect [31]. Therefore, a layout-based SEE prediction is adopted using the MC-Oracle prediction tool [32]. The standard cells analyzed in this work are issued from the 45 nm OpenCell Library from NanGate [33] and its simplified cell layout design is shown in Fig. 1. Only the metal1, active diffusion and poly layers are shown for clarity.

MC-Oracle is a predictive tool based on Monte Carlo simulations to estimate the SEE sensitivity of electronics components based on the physics of particle interaction within the devices. The ionization mechanism is modeled using tables of range and electronics stopping power pre-calculated with SRIM [32]. The diffusion-collection model is used as the charge collection process [34-36]. Considering a particle hit into the component, the ionizing track is numerically divided into small fragments in which the generated charges diffused to the collecting drain areas. The transient current is obtained from the integration of the collected charge along the ionizing track for each elemental section of the drain area [36]. The collecting areas are directly extracted from the GDS (Graphical Design System) format file of the circuit. For every particle event, energy deposition and charge collection are calculated for each collecting area, i.e. each drain region of the circuit design. Accordingly, multiple node charge collection is considered and the SPICE parameters to describe each resulting transient current in circuit-level simulations are stored in an SET database.

Considering a given Linear Energy Transfer (LET), a high number of particles is simulated to reach the minimum of 100 observed events. The confidence is the root square of the number of events, accordingly, with a minimum of 100 events, it is obtained 10% confidence. To calculate the SET cross-section and pulse width, an injection campaign is performed using SPICE simulations with the post-layout parasitic extraction netlist of the circuits and the SET database. The analysis is performed for each input signal of the circuit separately and an arithmetic mean is calculated for the circuit SET cross-section and pulse width. Besides different sensitive nodes, different input signals provide different restoring current and consequently different radiation robustness [31]. All circuits drive a fan-out 1 (FO1), i.e. an inverter was coupled to its output signal in which the SET measurement is carried out.

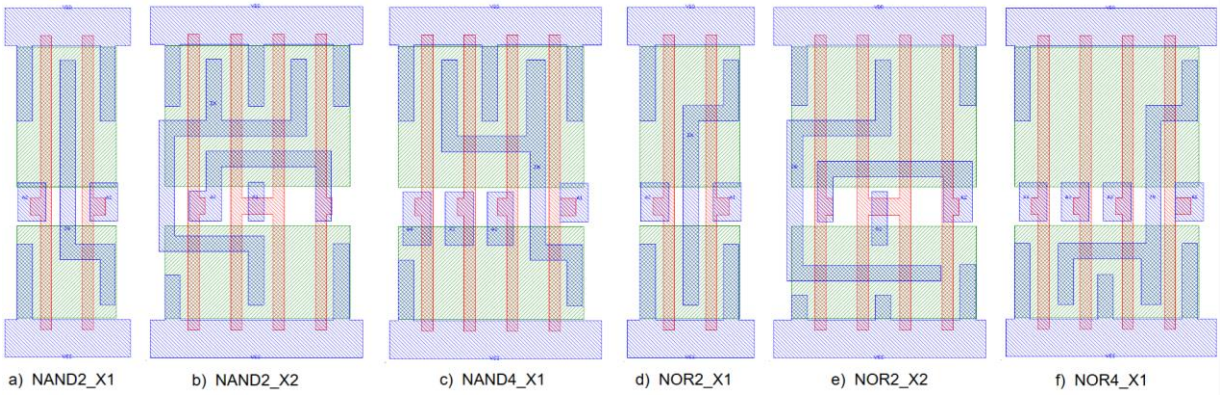

Fig. 1. Simplified cell layout design of logic gates from the 45-nm bulk CMOS [33] containing metal1, active diffusion and poly layers.

4. Results and Discussion

The radiation robustness of a circuit design is influenced by a variety of physical and electrical factors. Increasing the nodal capacitance and restoring current improves the overall robustness, however layout and drain area should also be taken into consideration to evaluate the effectiveness of RHBD techniques. Table 1 presents the layout and drain area information for the NAND and NOR gates considering the minimum sized (called as original design), gate sizing and transistor stacking. It is important to notice that both NAND and NOR gates provide the same layout design area. This is also observed when considering gate sizing and transistor stacking approaches due to the cell design regularity characteristic of a standard cell library implementation. Thus, in terms of area overhead, these hardening techniques provide the same increase of 66.7% for the analysed layout design of NAND and NOR gates. However, despite the same layout design area, a different sensitive collecting area is obtained for each technique. Considering the total area of the drain junctions in the layout, i.e. the sensitive collecting area, the two techniques present an area increase. For both circuits, transistor stacking showed the greatest increase in drain area, 107.5% and 110.9% for NAND and NOR, respectively. Originally, the NOR gate presents approximately 11.6% greater drain area than the NAND gate. When applying the hardening techniques this difference reduces to 8.5% for gate sizing, and increases to 13.5% for transistor stacking.

Besides the increase in area, adopting RHBD techniques generally implies an increase in power consumption. Due to the increase in leakage current in advanced technology nodes, the static power consumption is considered in this work. Fig. 2 presents the static power consumption for the NAND and NOR gate considering both RHBD techniques. For both standard cells, gate sizing showed the largest

Table 1
Layout and drain area of the original design, and applying gate sizing and transistor stacking techniques[a]

		Original (μm^2)	Gate Sizing (μm^2)	Transistor Stacking (μm^2)
Layout	NAND	0.895	1.492 (66.7%)	1.492 (66.7%)
	NOR	0.895	1.492 (66.7%)	1.492 (66.7%)
Drain	NAND	0.190	0.351 (84.6%)	0.394 (107.5%)
	NOR	0.212	0.381 (79.6%)	0.447 (110.9%)

[a]Area increase is expressed in percentage.

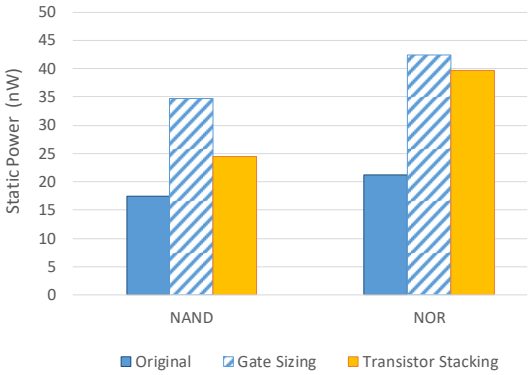

Fig. 2. Static power consumption estimation for original, gate sizing and transistor stacking implementations of the NAND and NOR gates.

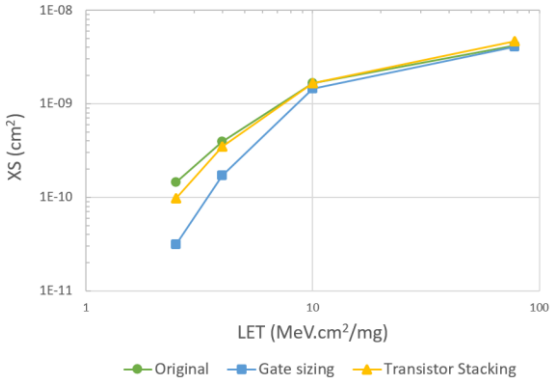

Fig. 3. Average of the SET cross-section for each input signal the NAND logic gate: minimum sized (Original), using Gate Sizing; and Transistor Stacking.

increase in power consumption, a factor of 2. Due to the leakage current reduction provided by the transistor stacking effect, both circuits have shown lower power consumption when compared to the gate sizing technique. The NMOS transistors in the pull-down network provide higher leakage current than the PMOS transistors. When adopting transistor stacking using standard cells, the stacked devices for the NAND and NOR gate are the NMOS and PMOS transistors, respectively. This explains the greater reduction observed on the static power reduction of the NAND gate, as it contains stacked NMOS devices.

Fig. 3 provides the log-log representation of the SET cross-section for the NAND gate. The cross-section was calculated for each input vector of the gates and the arithmetic mean for each particle LET is shown. For 2.5 MeV.cm^2/mg, gate sizing provided the greatest reduction on the SET cross-section, approximately 78.4%, while a reduction of about 33% is expected by transistor stacking approach. The radiation robustness efficiency of both techniques reduces as the particle LET increases. For 78 MeV.cm^2/mg, the gate sizing technique still provides

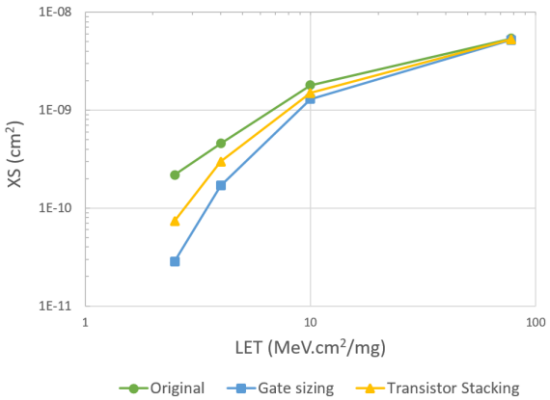

Fig. 4. Average of the SET cross-section for each input signal the NOR logic gate: minimum sized (Original), using Gate Sizing; and Transistor Stacking.

a reduction on the overall SET cross-section, solely 3% of reduction. On the other hand, the transistor stacking technique increased the SET sensitivity of the circuit to about 11.7%. This increase in cross-section is related to the increase in layout area and drain regions when adopting these RHBD techniques. For higher particle LET, the dominant effect on the circuit reliability is the charge collection efficiency enhanced by the larger transistors. A similar trend is also observed for the SET cross-section curve of the NOR gate shown in Fig. 4. However, both techniques exhibited a higher efficiency when compared to the NAND gate. For instance, the transistor stacking provided an SET cross-section reduction of approximately 66.3% at 2.5 MeV.cm^2/mg, twice the reduction observed for the NAND gate. The SET cross-section for each input signal for the NAND and NOR gate under 78 MeV.cm^2/mg can be seen in Fig. 5 and Fig. 6, respectively. The input signal (1, 1) is the most sensitive for the NAND gate, while for the NOR gate this is the input (0, 0). Notice that for the most sensitive input combination, both techniques provide a higher cross-section than the original design, especially the transistor stacking. In the transistor stacked NAND (NOR) design, all radiation sensitive transistors are PMOS (NMOS) devices. Consequently, the 4-stacked NMOS transistors in the NAND pull-down network are providing the restoring current to counteract the parasitic SET pulse. However, transistors in series provide less current drive due to the increased effective resistance, leading to performance degradation and also larger SET pulse width and increased cross-section. Fig. 7 provides the SET pulse width measurements for each technique applied on the NAND gate. The original and gate sized designs present similar pulse width mean and maximum, however, the transistor stacking design can have a maximum SET pulse width more than 2x larger than the original design due to the reduced drive

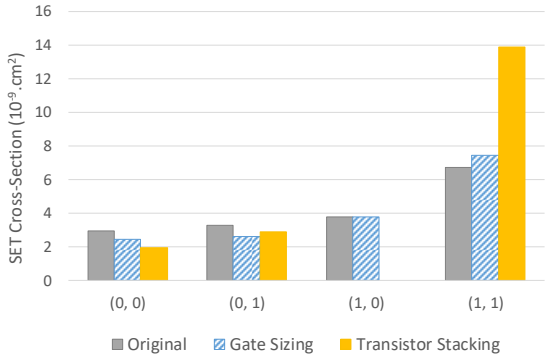

Fig. 5. SET Cross-Section for each input signal combination of the NAND gate under 78 MeV.cm^2/mg.

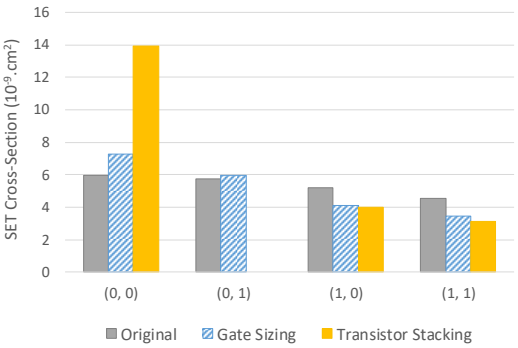

Fig. 6. SET Cross-Section for each input signal combination of the NOR gate under 78 MeV.cm^2/mg.

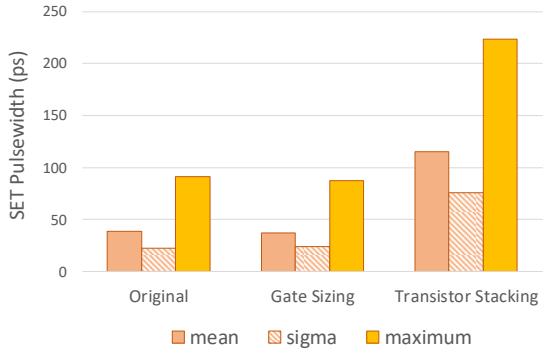

Fig. 7. SET pulse width measurements for the NAND gate under 78 MeV.cm^2/mg.

strength of the stacked devices.

On the other hand, for the NAND input signal (0, 0), a lower sensitivity is obtained due to the increased capacitance in the off-state NMOS transistors. The same behaviour can be observed in the NOR (1, 1) result shown in Fig. 6.

5. Conclusion

This work has evaluated the radiation efficiency of gate sizing and transistor stacking using standard cells. Besides the area and leakage current increase,

both techniques provide a reduction on the overall SET cross-section for low particle LET. The NOR gate shows the greatest improvements on the SET cross-section even though transistor stacking can increase the maximum SET pulse width to 2x wider than the original design. Gate sizing shows the best trade-off between area, power and reliability. However, the hardening efficiency of transistor stacking is strongly dependent on the input signal of the gate. Thus, according to the application, this technique can outperform gate sizing.

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