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Development of SiC reliability study tool

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ABSTRACT

Understanding the failure mechanisms is essential to ensure reliability for a new technology of semiconductors. Amongst various existing tools dedicated to silicon-based devices, there is no consensual method for silicon carbide (SiC) devices. This semiconductor offers very interesting properties for power electronics in comparison with Si, but these failures are different and need to be studied. This paper will compare different methods applied to failures, focusing on lock-in thermography and micro-Raman analysis. Three devices will be evaluated, a vertical diode, a lateral diode and a MESFET. A methodology will finally be recommended as a valuable and robust solution for failures mechanisms further studies.

1. Introduction

Nowadays, reliability is fundamental to establish a new market tendency with SiC technology. Indeed this semiconductor allows a better efficiency in comparison with silicon and can be applied for example in most of electrical vehicle due to its high temperature capability. This technology can greatly improve our electrical energy management and failure mechanism study is required to propose devices with higher performances and better robustness [1]. In this study, we will discuss about several characterization methods for failures on SiC devices: SEM, FIB, active infrared thermography, micro-Raman spectroscopy, OBIC, and Photon Emission. Each has some pro and cons and permits to observe different phenomena as it will be described in the article. The proposed study approach is valid for all kind of device without packaging but we will focus in this article on a vertical diode, a lateral diode and a MESFET in order to test several configurations. We will highlight several failure mechanisms created after electrostatic discharge (ESD) stress or after overvoltage stress. A standard characterization method is proposed at the end.

First, we will present the three devices, and the failures observed after two different stresses. Then we will use different tools to investigate the phenomena observed in these examples. Finally, we will point out the role of each tool and its limitations in order to propose a more efficient and relevant SiC failure study in the future.

2. Three SiC devices: MESFET, lateral diode, vertical diode

Vertical diodes were made by Dr. Lazar at the Ampere Laboratory as part of the ISMART project. The aim was to create a thermal and fast neutron sensor [2]. Compared to a vertical PiN power diode, a doped layer of Boron (^{10}B) used for radiation measurement in the anode metallization, was added at the interface between the Nickel-Titan-Aluminum layer and SiC P^+ (Fig. 1). A leakage current of 10 pA for a voltage of −5 V was measured. In forward bias, the threshold voltage was around 2.8 V and the internal resistance approximately equaled to R_{on}=1000Ω (Fig. 5). All the diodes on the wafer presented the same static characteristics, regardless their size.

MESFETs and lateral Schottky diodes (Fig. 2) are contained on the same wafer, originated from the CNM Laboratory and were designed for an easy adaptation to drive power transistor. MESFETs characteristics were ranging from 0 to 15 V with respectively 0 to 20 mA. They can also operate in static mode until 150 V [3]. During electrostatic discharges (HBM-ESD), failure was observed at voltages from about

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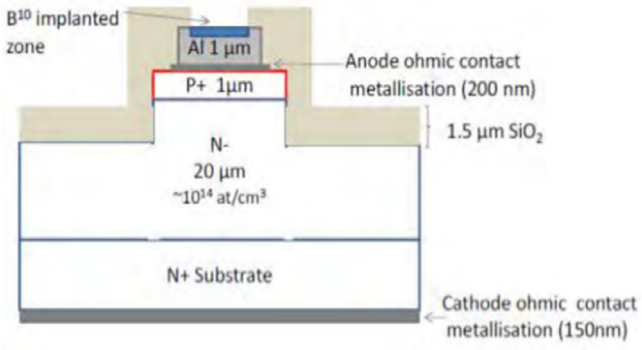

Fig. 1. Transversal section of vertical SiC diode.

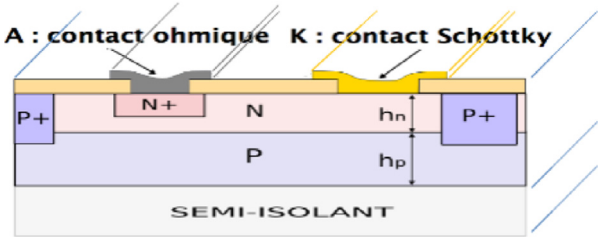

Fig. 2. Transversal section of lateral Schottky diode.

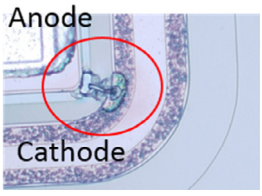

Fig. 3. Failure visualization after ESD stress on lateral diode.

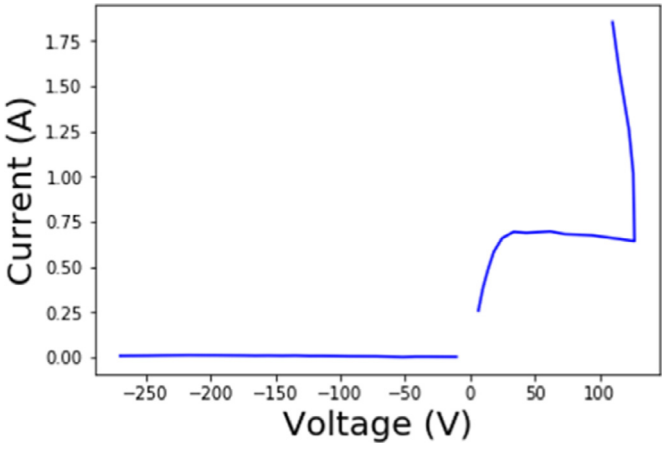

Fig. 4. I-V after HBM-ESD stress on SiC lateral diode.

50 V. The lateral diodes supported up to 200 V in static mode when submitted to HBM-ESD failure at −140 V. They have a threshold voltage of 0.6 V, an internal resistance R_{on}=30Ω and a high leakage current with milliamps.

3. Definition of destructive events

Two destructive stresses were performed in this article. First, the MESFET and the lateral diode were evaluated against electrostatic discharge (ESD). Human Body Model (HBM) corresponds to a 150 pF capacitor discharge was applied. In this test method, the amplitude of the stress was increased until failure observation. An electric arc was thereafter visible at microscopic scale between cathode and anode electrodes, using an optical microscope (Fig. 3). I-V measurement showed abnormal current increase (Fig. 4). According to the failure visualization, this current discharges through the defect appeared as a dielectric breakdown.

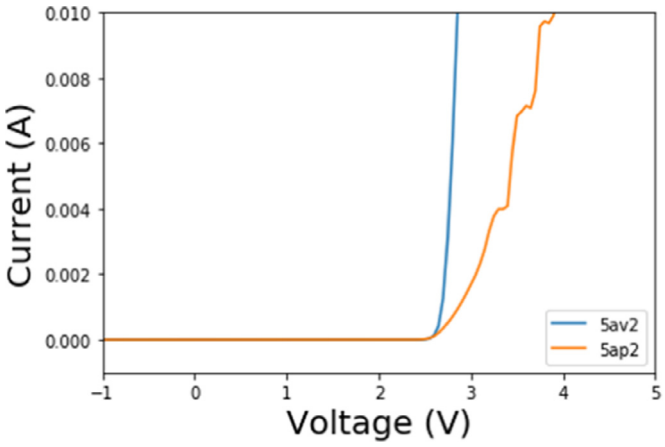

Fig. 5. I-V for SiC vertical diode before failure (5av2) and after (5ap2).

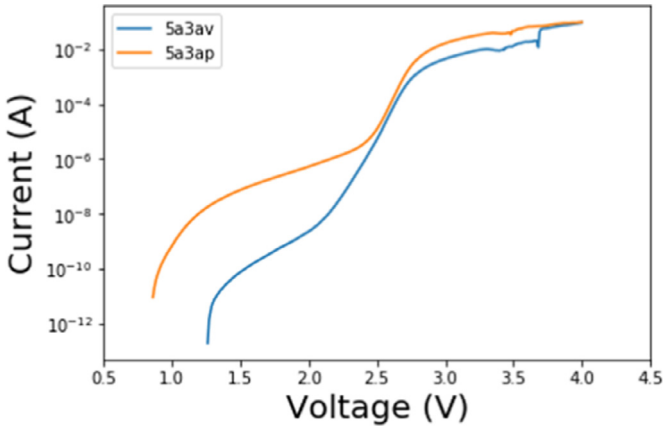

Fig. 6. I-V in semilogy for SiC vertical diode before failure (5av2) and after (5ap2).

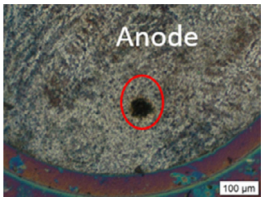

Fig. 7. Optical Microscopy after high voltage failure.

Fig. 8. Optical microscopy after high voltage failure on the corner of the device.

The second stress performed in this study was related to static voltage rise on the vertical diode. After reaching 30 V a failure was revealed: the current increases linearly as represented in blue in Figs. 5 and 6, while those before failure were shown in yellow in the same figures. To take advantage of covering a surface without metallization, the tip was placed on the edge of the device, as depicted in Figs. 8 and 9. As the failure occurred, the diode no longer emitted photons and its current level decreased drastically. When the voltage was increased again, the current increases was slower, indicating that R_{on} was modified (see Figs. 5 and 6).

Voltage rise was also applied in reverse mode on three diodes. Up to 200 V, no failure were observed (Fig. 9) although some devices presented significant current increase, with particularly higher leakage current. One hypothesis to explain this observation could be that impact ionization -due to strong field- may have increased the probability of electrons crossing the space charge barrier. The electric field

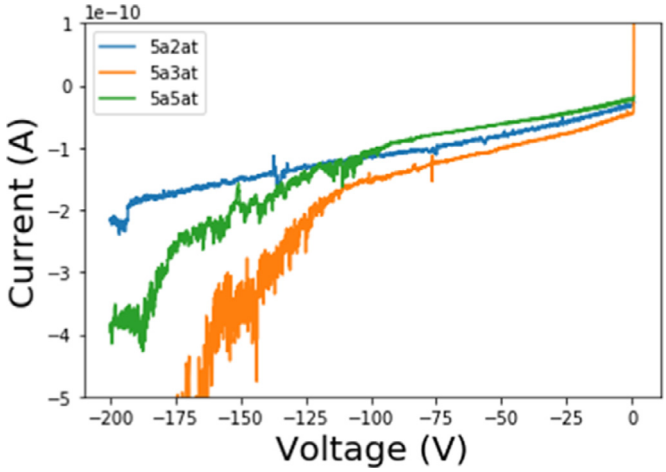

Fig. 9. I-V for three vertical diodes.

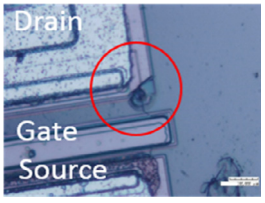

Fig. 10. Failure at the MESFET corner after HBM-ESD stress.

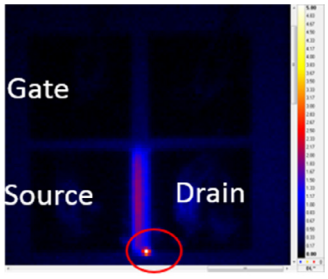

Fig. 11. Amplitude image with lock-in thermography after HBM-ESD stress on SiC MESFET.

applied could thus have been insufficient to create a crack in the dielectric, while in a transistor -composed of a succession of doping- a destructive parasitic transistor is triggered.

4. Lock-in thermography after ESD stress

A deep analysis was performed to understand the MESFET-failure origin after ESD. Thanks to SEM observation (Fig. 10), it was shown in [4] that a too strong electric field can break the SiO_2 layer [5]. However, other tools have to be used to complete the analysis.

Even if the defect is visible on the surface, lock-in thermography -carried out at the CNM laboratory- could help to better and deeper understand failure mechanisms. After appropriate treatment, this infra-red measurement provides useful amplitude and phase representations of the excited electrons during device polarization [6]. In this study, 1 V sinusoidal signal at a frequency of 100 Hz was applied between MESFET Drain and Source.

Thereby failures have been located at the gate corner. Indeed failures were identified in *x*-axis and *y*-axis with the amplitude image (Fig. 11) and in *z*-axis with the phase image, where the corner position depicted deeper failure characteristics (Fig. 12). This representation is consistent with the SEM representation. Taking together, these results strongly suggest the creation of deep hot spots at the corner of the MESFET as failure origin. The resolution of this method is of about ten micrometers, which is unfortunately not convenient for 100 µm-size devices. However, it helps defining interesting hypotheses to understand failure mechanism, (i) heating may have caused a hole in the semiconductor by sublimation, or (ii) metal layer may have melt at the component surface, modifying the contact resistance, and slightly digging the SiC surface.

5. FIB-EDX results

Another method to study SiC-defects consists in using Focus ion Beam (FIB). In a previous study [7], short circuits were submitted to high temperatures until failure. Thanks to FIB analysis, the authors identified failure origin as gate metallization failure. Indeed, a

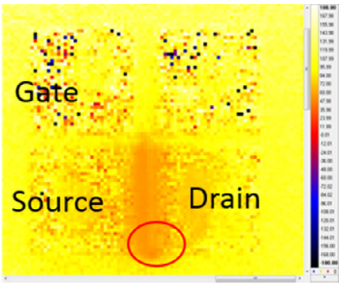

Fig. 12. Phase image with lock-in thermography after HBM-ESD stress on SiC MESFET.

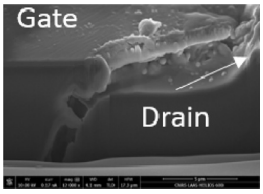

Fig. 13. SEM image after FIB on a failure in SiC MESFET after ESD [7].

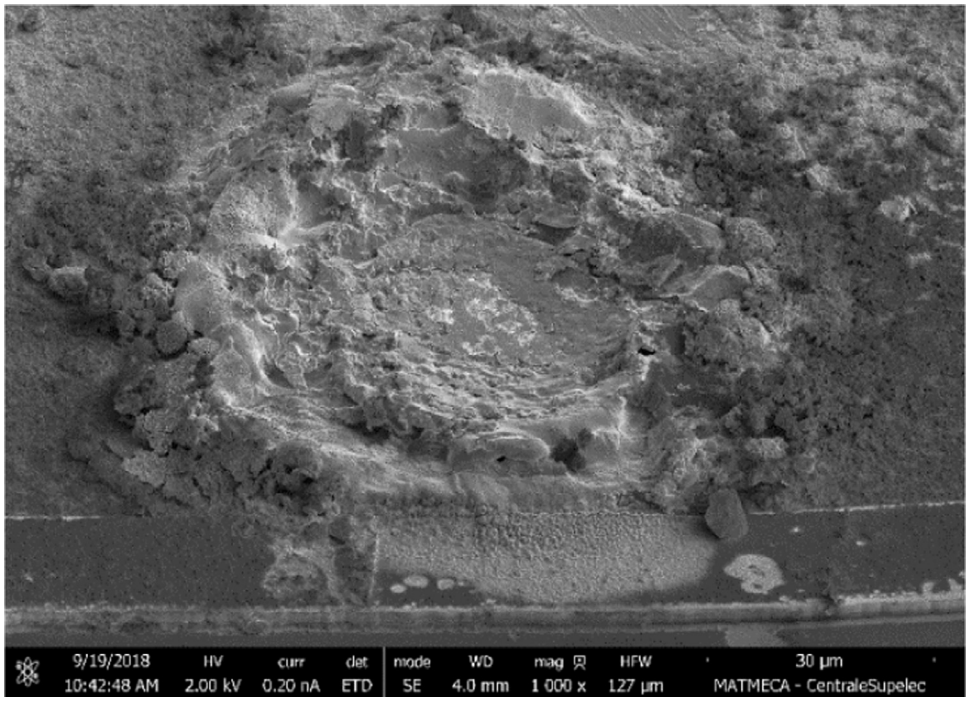

Fig. 14. SEM Image after FIB on a failure after high voltage applied on SiC vertical diode.

voltage drop, an increase in grid current, as well as a crack in the FIB image were observed, while the infrared image indicated overall luminescence under the MOSFET gate.

In one of our previous study, the FIB analysis on MESFET device also clearly revealed the presence of a hole (Fig. 13). This defect undoubtedly appeared after the activation of a parasitic transistor, causing SiC sublimation, during ESD [3].

In this study, both FIB and Energy Dispersive X-ray (EDX) analyses were performed on vertical diode. Results suggested a melting of the metallization at the interface (Figs. 14 and 15). Comparing EDX response before and after stress, Aluminum level decreased significantly, whereas Silicon level increased and Nickel and Titan stayed stables (Figs. 16 and 17). This result can be explained by the lower melting temperature of Aluminum in comparison with Nickel and Titan. In addition, the FIB cut (Fig. 14) showed that the defect remained on the surface and that SiC was not attacked (Fig. 15), explaining its relative proportion increase. As a result, internal resistance decrease -previously described in section 3 - may only be due to the local modification of the metallization.

Thanks to FIB, failure mechanisms were highlighted for both vertical diode and MESFET devices. Whereas surface-level failure was identified on vertical diode, MESFET presented a completely different defect structure, occurring as a hole in the semiconductor.

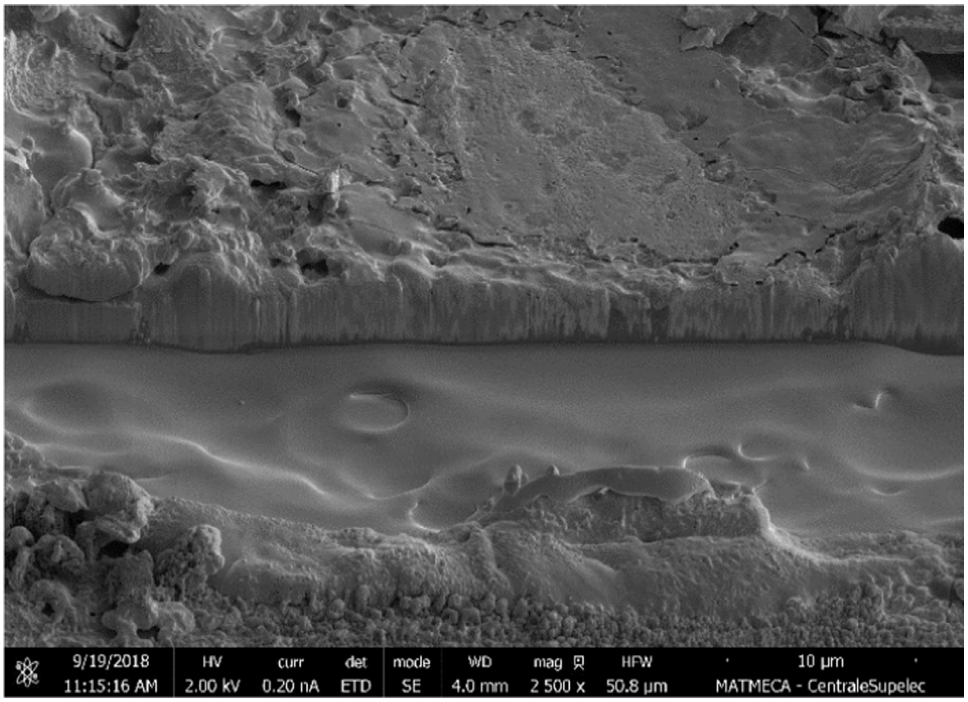

Fig. 15. Zoom on failure in SiC vertical diode.

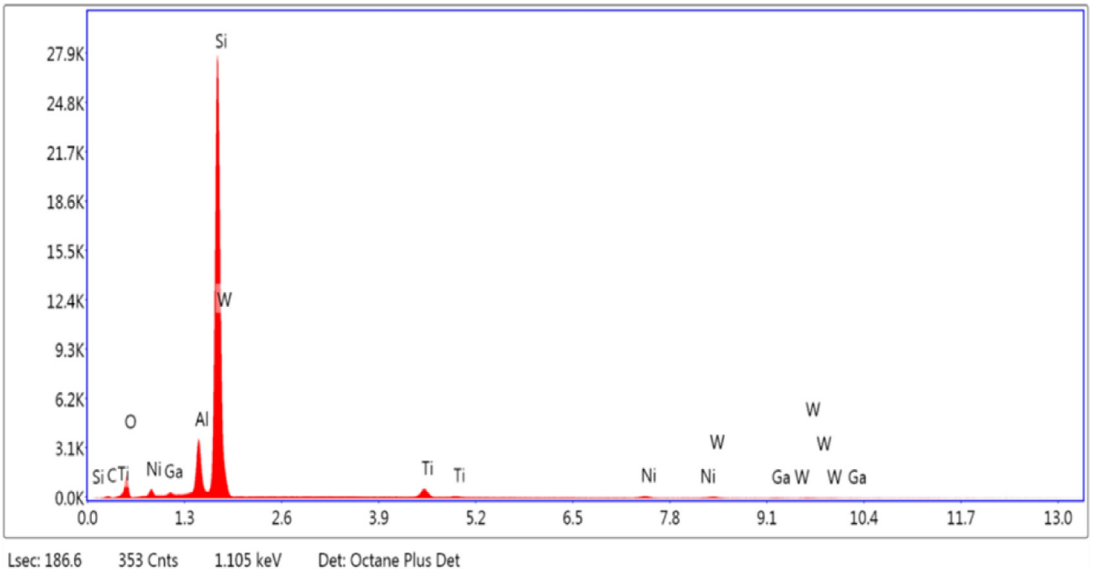

Fig. 16. Micro-Raman mapping of the Si integrated intensity.

6. Micro-Raman analysis

Different tools such as the Optical Microscope (OM), the Photo-Emission Microscope (PEM), or the Scanning Electron Microscope (SEM) are usually used to locate defect in surface. For example, Schottky SiC diodes with internal defects -micrometer comets- were observed with optical microscope and SEM in [7], whereas 100nm-size micropipes were identified with a specific Micro-Raman analysis [8].

In this study, after identification of the vertical diode failure, we applied micro-Raman spectroscopy analysis -with a CLSM setup (Confocal Laser Scanning Microscope)- to identify SiC crystalline structure at the defect level. This analysis indicated the presence of a metallic alloy residue on the diode surface. A migration of silicon atoms was also observed at the defect position (Figs. 18 and 19), suggesting atoms rupture and carbon atoms gathering in the observed metal alloy. In [9], SiC carbon atoms disappeared by combustion, leaving amorphous silicon and polysilicon on SiC surface device. Same results were obtained with Raman analysis performed in this study (Figs. 18 and 19). And the conclusions were the same for ESD failure and static failure. One strong explanation for this defect could be the presence of a strong electric field as well as a local high temperature, both concentrated at the contact between the tip and SiC.

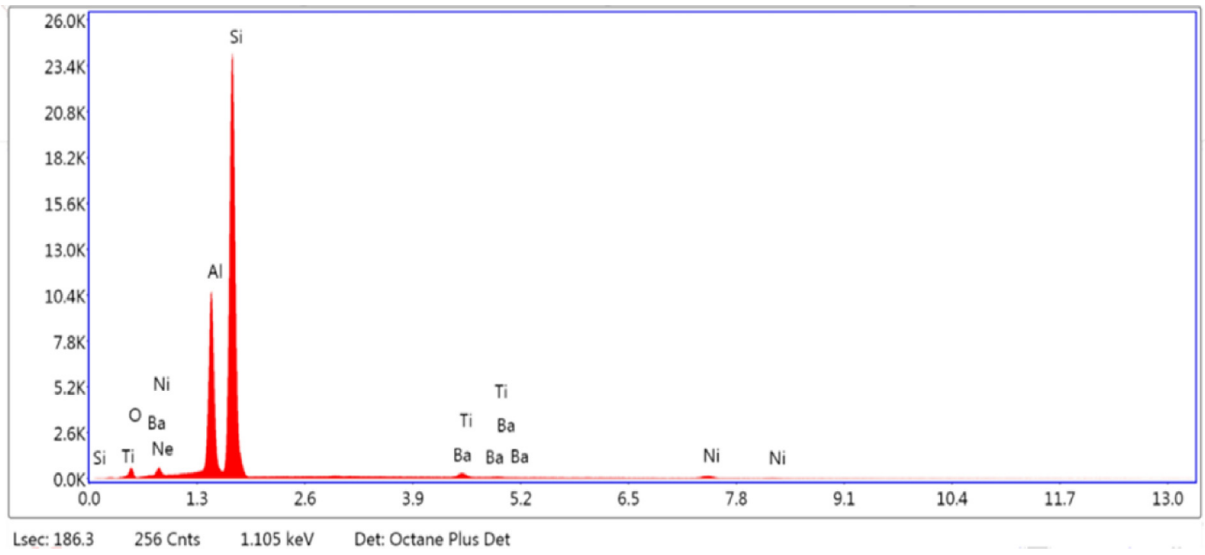

Fig. 17. EDX of SiC vertical diode before failure.

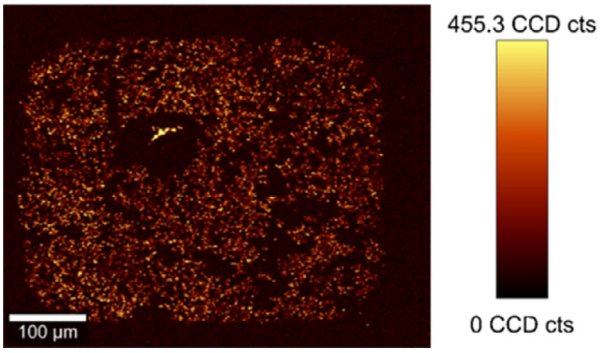

Fig. 18. EDX of Sic vertical diode after failure.

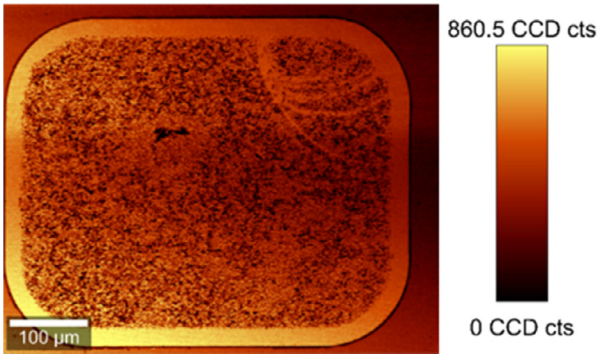

Fig. 19. Micro-Raman mapping of the Sic integrated intensity.

All together these methods help determining the mechanisms leading to failure for vertical and lateral SiC diodes as well as for MESFET component. The next paragraph will focus on the pro and cons of each method and finally propose an improved methodology to study such component failure mechanisms.

7. Limits of each tool

This paragraph will discuss the different tools and their limits to determine a failure on a SiC devices. First, it's worth mentioning that failures on SiC devices are often related to packaging [10] or dielectrics [3]. It would be necessary to search for more efficient packaging, insuring both reliability and performances SiC technology, that is to say, with higher sustained temperatures and lower switching losses.

Concerning the failure, a visual analysis with an optical microscope or SEM often provides the first information. In [11] for example, authors presented SEM images of the devices after Unsynchronized Inductive Switching (UIS) destructive stress, where failures can be clearly identified. Others tools are sometimes used to detect the failure, as Optical Beam Induced Current (OBIC). This method measures

-in a short time- the photo-current emitted by the component and thus allows defect location [12]. However, it is not possible to observe a deep failure with this method. A surface defect is therefore localizable with this tool, but its study is rather difficult.

Lock-in thermography provides a representation of hot spots with a ten micrometers resolution. It can then be difficult to work on nanometric devices. But as SiC components are often intended for power, their size is usually ranging from ten to several hundred micrometers, making this tool as particularly appropriate for SiC devices study. A second problem could be link to device polarization. It is necessary to connect device to a PCB linked to the alimentation with bonding wires. This process limits the use of lock-in thermography for isolated devices, and is therefore not adapted for component integrated on a wafer. Nevertheless, this method sometimes detects not previously visible defects [13].

Another technique recently used for failure detection is Photon Emission (PE) and Spectral Photon Emission (SPE). For example in [14], after an ESD stress, a current variation was observed during Ids-Vds measurements. Unfortunately, the Ids-Vgs and Cgs-Vgs measurements doesn't reveal any difference between the failed and the reference devices. The MOSFET is then prepared for the microscope without adding any damage, which means that the semiconductor must be accessible without metallization [15]. The measurement procedure consists of 3 acquisitions: the reference image, the image of the emissions and the superposition. The result is the presence of hot spots on the source side. A spectral analysis can then be performed even if the addition of different defects complicates the interpretation of failure mechanisms. The authors observed a difference in the spectrum after failure, interpreted as a degradation of the gate oxide [14].

To go further, micro-Raman analysis should be used. It helps to determine the nature of atoms and thus to understand the migration of dopants and atoms, or the creation of alloys. However and as for PE, the analysis needs a non-metallic and flat surface -due to the confocal configuration-. It often requires a chemical step to remove metal or other disturbing coating to correctly visualize the defect, because this analysis consists in studying the light scattered through the sample. This process can be difficult to implement, especially on commercial components.

Finally, one effective method after fault localization is the coupling of the FIB with SEM images [16–19]. During the analysis, ions will attack the semiconductor at atomic scale. A problem currently observed with SiC failure is the sublimation at high temperatures [3]. These holes are sometimes detectable with FIB. Unfortunately sometimes the FIB will fulfill these holes by trying to push back the layers of atoms. The second problem with the FIB is that it is a destructive analysis that condemns the device. However for the study of failure mechanisms, this is probably not a problem, especially since these tools are combined with TCAD Sentaurus simulations, which avoids excessive expenditure.

8. Conclusion

Failure mechanisms is crucial for new semiconductors, especially to entirely understand the limits and to overcome the industrialization obstacles. SiC is a semiconductor with different properties and behaviors than silicon, then, different tools for failure mechanism study are required. This work summarizes the mains different tools usually used, with their pros and cons. A focus on lock-in thermography and on micro-Raman analysis is presented but the use of standard static measurements, assisted by TCAD Sentaurus simulation as well as SEM and FIB images, seems to be the most relevant approach to fully understand the three main phenomena that can occur in SiC devices: dielectric cracking, melting of the metallization and triggering of a parasitic transistor.

Acknowledgments

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Credit Author Statement

Tanguy Phulpin: Measurements, Analysis, Writing. **Alexandre Jaffre**: Microraman characterization. **José Alvarez**: Microraman characterization. **Mihai Lazar**: SiC diode conception, Reviewing.

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