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***Abstract* — This paper describes the I-V characteristics obtained from a 4H-SiC current limiting device. Some specific aspects of the specific on-resistance are discussed in simulation with the DESSIS ISE software. The device behaviors place it in the field of the best Implanted Channel MOSFET (IC-MOSFET) obtained in the literature. The best on–resistance measured is 13 mΩcm² and the saturation current density reaches 900 Acm⁻².**

***Index Terms* — 4H-SiC, MOSFET, Current Limiting Device, Simulation, I-V Characteristics, Low Specific On-Resistance, Forward Current Density, Serial Protection.**

I. Introduction

Since april 2001, SiC devices are commercially available. These new devices are Schottky diodes proposed by Microsemi and Infineon Technologies AG. The available grading are 300 V/ 10 A and 600 V/ 4-12 A for PFC applications and DC/AC converter. SiC technologies should be able to produce high quality of power rectifier, but there is no SiC power switches commercially available yet. In the high frequencies field, the current trend seems to be the MESFET which could be placed between the silicon and the GaAs ones [1].

For power applications, the main researches turn towards the power MOSFET, JFET and the thyristor GTO structures. The main problems encountered in thyristor technologies are the low current gain obtained (β=20) comparing with the silicon ones, du to the low minority carrier lifetime measured (best of 5 µs measured for low injection level and low doping concentration [2][3]). Another problem is the low efficiency (30 %) of the peripheral breakdown protection used in thyristor technologies [4], which leads to an increase of the P-base epi-layer thickness and then, leads to a lower current gain of the NPN bipolar transistor.

Some SiC unipolar structures present higher electric characteristics than the last evolution of the silicon power Mosfet (alias *CoolMos*™ [5] or *super-junction MOSFET*). Nevertheless, in SiC technologies, the SiO_2/SiC interface presents a high density of trap and the oxide layer itself owns a large quantity of fixed charge. Those parasitic charges reduce the electron mobility in the inversion layer. This low mobility value would be also the consequence of the crystalline orientation SiC surface chosen for the SiO_2 growth. A lot of research team are working on better technological conditions for making SiC power MOSFET with lowest specific on-resistance (surface studies, SiO_2 growth conditions, post-implantation annealing process). To avoid insulator/SiC problems, the current trends turn towards JFET or Accu-MOSFET. Such devices, shown in the literature, exhibit the best electrical characteristics obtained in SiC technologies : low specific on-resistance and high current density ability (Accu-MOSFET : 16 mΩcm² / 1600 V [6] ; JFET : 10 mΩcm² / 600 V and 14 mΩcm² / 1800 V [7]).

Nevertheless, the technological steps used for the built of these devices require complex (expensive) process (deep implantation, epitaxial growth inside, deep plasma etching and a lot of mask levels) and there is no sign of a next commercially SiC power switch.

In this paper, another unipolar device structure is shown and an evaluation of the electrical static characteristics of prototypes is given. The physical properties of SiC allow the development of new devices for applications not covered by the silicon technologies. The function (serial circuit protection) requires to limit a short-circuit overcurrent during a time long enough to allow the opening of the power line (a 230 V / 50 Hz network) by a circuit breaker under reliable conditions. The design of such a device [8] is proposed here with a special view on its specific on-resistance studied in simulation with the DESSIS® ISE software [9], and in experimental measurements. This device has to work under high junction temperature and the thermal aspect will not be discussed here, but they are given elsewhere [10]. A current limiting device must have the lowest resistance as possible for the normal use, the End User requirements specify a value close to 10 mΩcm², high current saturation density and simple technological process.

II. Device structure, simulation and process

A. Device structure and specific on-resistance

1) Device structure, IC-MOSFET (Implanted Channel MOSFET) :

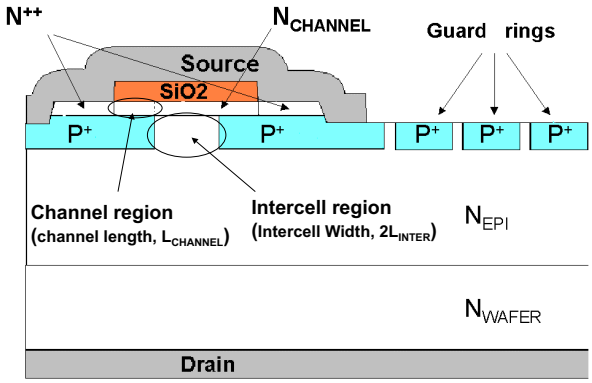

Fig. 1 : Structure of the current limiting device (a peripheral cell). The IC-MOSFET is shown with its guard rings protection, the implanted N channel and the P^+ implanted layer. The channel and intercell regions are noted on the schema.

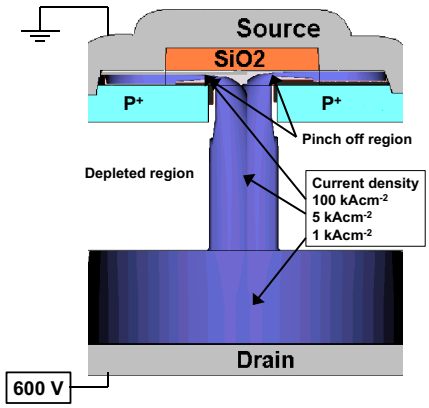

Fig. 2 : Simulation view of current density inside the device in the saturation phase. The N epilayer is depleted entirely and the current is pinched off at the end of the channel.

The design of the current limiting device is based on a Power Mosfet (like a N channel VDMOSFET in silicon technology) in which a N channel is implanted and the source and gate contacts are connected (V_{GS}=0 V) (figure 1).

As the Power Mosfet structure, the anti-parallel built-in diode doesn't allow a bi-directionnal capability. The current limitation only appears in case of positive drain-to-source bias voltage (figure 2). For low V_{DS}, the device acts as a resistance, R_{ON} ; and if V_{DS} increases over V_{DSSAT}, the resistance reaches highest value (ideally ∞) and the current stays equal to the current saturation value. The pinch-off effect is localized at the end of the N channel region.

2) Specific on-resistance :

This component has to be ranging for 600 V / 50 A and its on-resistance should be lowest as possible. For a fixed efficiency of the peripheral protection (evaluated by simulation using DESSIS® ISE), the thickness of the drift-layer can be estimate. In this case, the desired breakdown voltage is 600 V and the peripheral protection efficiency is about 50 %. The protection used is chosen in order to minimize the number of photolithographic mask, and we take a guard rings protection made in the same way that the P^+ layer. By the way, the peripheral protection used is composed by three P^+ guard rings of 10 µm width and of 3 µm width between each other's. The N epitaxial layer of 4×10^{15} cm^{-3} / 7 µm is chosen and a breakdown voltage of 720 V is simulated with the guard rings protection. A breakdown voltage of 630 V is experimentally obtained from a pin test-diode protected as well, comparing to the 730 V of the simulated one.

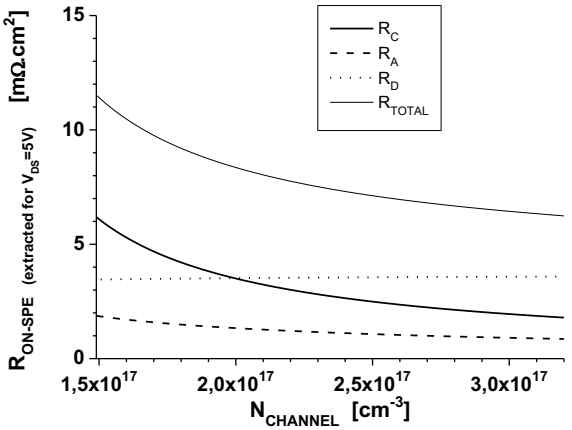

Fig. 3 : Simulation of the variation of the partial specifics on-resistances of the device versus the channel doping level ($N_{CHANNEL}$). The channel length is 4 µm and its junction depth ($N_{CHANNEL}/P^+$) is 0.3 µm

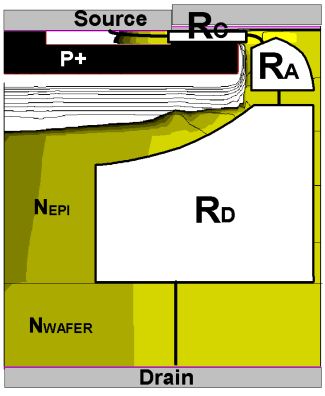

Fig. 4 : Description of the different parts of the total on-resistance inside the simulated device. The channel resistance, R_C, the access resistance, R_A and the drift resistance R_D are noted.

The entire on-resistance, R_{TOTAL}, is the addition of the channel resistance, R_C, access resistance, R_A, and drift resistance, R_D (Fig. 3, Fig. 4).

The on-resistance depends on the channel parameter (doping level : $N_{CHANNEL}$, junction depth : $X_{JCHANNEL}$, and length : $L_{CHANNEL}$) and on the drift layer doping level and thickness. The access resistance value, R_A, is linked to the intercell width ($2\times L_{INTER}$) through the parasitic JFET effect induced by a smaller intercell width (below 2 µm). On figure 3, the total on-resistance is represented versus the doping level of the channel, $N_{CHANNEL}$. For $X_{JCHANNEL}$=0,3 µm and $L_{CHANNEL}$=4 µm, the channel resistance decreases when the doping level increases. Up to 2×10^{15} cm^{-3}, the channel resistance, R_C, (figure 4) become lower than the drift one and contribute for 40 % to the total resistance (in the simulation, we take $n=N_D$. In case of incomplete ionization of the donor, electron density, n, is closed to $0,8\times N_D$ at 300 K, that means a change of 20 % up for the total resistance value).

On figure 5, the total specific resistance is plotted versus the channel parameter. The goal, for the total resistance value, is 10 $m\Omega cm^2$ and it can be achieve with a channel doping level up to 2.5×10^{17} cm^{-2}, a channel length of 4 µm and a channel junction depth of 0.2-0.25 µm. The choice of these technological values leads to a current saturation density of 1000 Acm^{-2} (this is the upper bound that we take, deducted from simulation results). In this way, the experimental result should be less sensible with the channel variation and a value of 12 $m\Omega cm^2$ could be obtained.

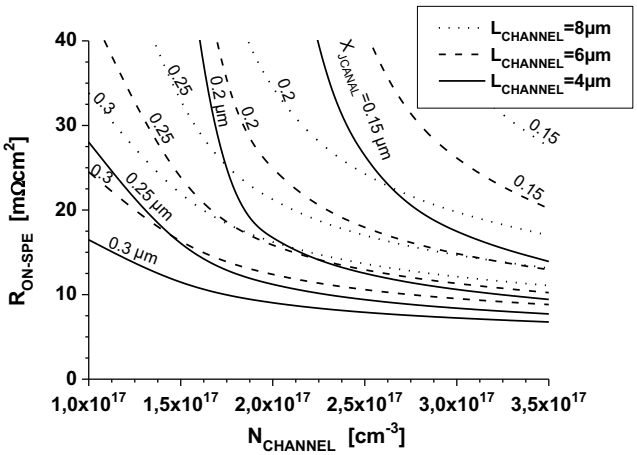

Fig. 5 : Simulation mapping of specific on-resistance versus the channel technological parameters.

B. *Technological data*

The 4H-SiC wafer used for the fabrication was purchased from CREE Research. It is composed by a N^{++} grown substrate (ρ=20 mΩcm / 430 µm) and a N type epitaxial layer (4.1×10^{15} cm^{-3} / 7 µm). The process used requires 5+1 mask levels (The first level only used for placing the devices on the wafer, with the alignment crosses). The P^+ buried layers are made by ionic implantation of aluminum. The channel region is implanted over the P^+ buried layer (nitrogen). A dry oxide of 50 nm is grown after a post-implantation annealing stage at 1700 °C / 30 mn [11]. The source contact is ensured by a high dose nitrogen implantation and a nickel layer. A plasma etching step is used to allow a connection with the buried P^+ layer and the source contact (bulk-to-source short-circuit in microelectronic technologies).

The table 1 summarizes the technological data used for the current limiting device.

Table. 1

Process steps	Technological data
P^+ implantation (Al)	500 keV / 10^{14} cm^{-2}
Nchannel implantation (N)	30-180 keV / 1.1×10^{13} cm^{-2}
Ncontact implantation (N)	30-100 keV / 10^{15} cm^{-2}
Epilayer (N)	4×10^{15} cm^{-3} / 7 µm
Substrate (N^+)	ρ=20 mΩcm

The values given on table 1 lead to a N channel with a doping level of 2-2.5×10^{17} cm^{-3} and a junction depth of 0.2-0.25 µm.

For the mask design, a multicell structure is defined with a hexagonal perimeter that allow to optimize the conduction perimeter versus the active area and simplify the geometrical adaptation with a circular periphery (figure 6). Different devices with different channel length (4,5 and 6 µm) and intercell length (4,6 and 8 µm) were realized. the conduction perimeter is kept constant and equal to 2880 µm. When using the implantation simulator developed by E. Morvan [12] for describing the doping profiles and using the finite element simulator DESSIS® ISE, the projected electrical behavior shows an on-resistance of 12 $m\Omega cm^2$, a current saturation density of 1050 Acm^{-2} and a saturation voltage close to 15 V.

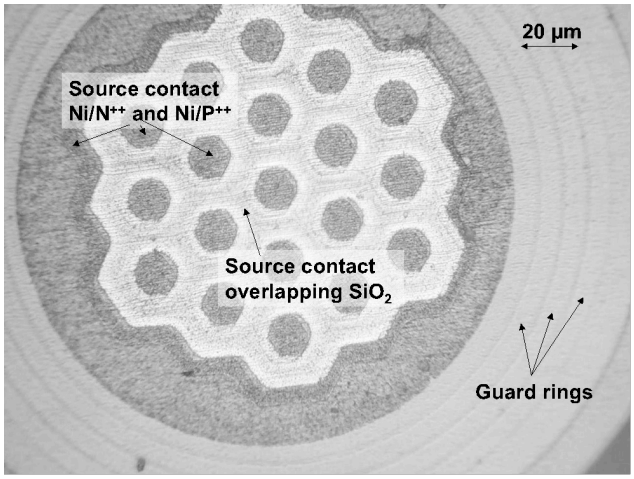

Fig. 6 : Photography (optical microscope) of a current limiting device. The guard ring protection is shown. The dark hexagons are the source contact part that reach the SiC N^{++} surface, the white parts (between the dark hexagons) are the source contact that overlay the oxide layer.

III. I-V CHARACTERISTICS.

The electrical characterization are made with a curve tracer tektronix 370. The devices are tested with probe on the entire wafer. The results are shown on figure 7 and figure 8. The simulated I-V characteristic (using technological projected data) is pointed on the graph for comparing with the real I-V curve. We find a good match between the simulation curve and the real curve in the case of a step-by-step measurement. It supposes that the projected technological data have been done and that the SiO_2/SiC charge density (interface+inside SiO_2) is low, may be ten time smaller than the channel dose ($\approx 5\times10^{12}$ cm^{-2}) and close to $\approx 10^{11}$ cm^{-2}. A saturation current density of 900 Acm^{-2} and a specific on-resistance of 13 $m\Omega cm^2$ are measured. This value are closed to the simulated one : 1050 Acm^{-2} and 12 $m\Omega cm^2$ that means the good electrical conductivity of the compensated channel comparing with the simulation ($\mu_{nchannel\text{-}simul}$=450 $cm^2V^{-1}s^{-1}$).

By comparing the measurement using the step-by-step method and the screen caption method, an illustration of the self-heating in the device is given. The step-by-step measurement means that the couple (I,V) is kept during the applied voltage rises. With the step-by-step method, each point is taken at a constant junction temperature and this temperature increases with the losses (and voltage) in the device. In the case of the screen caption curves, the ended voltage is applied and, after the I-V curve is saved. With the screen caption method, the junction temperature inside the device is roughly the same for each point of the curve.

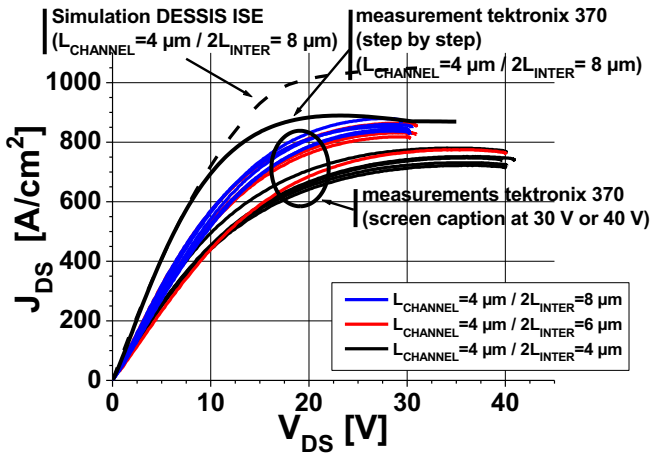

Fig. 7 : Experimental and simulated I-V characteristics of current limiting device with 4 µm for the channel length value. The saturation voltage is 15 V. The current density is calculated considering the entire source contact area.

The effect of the channel length is remarkable : the saturation current decreases as the channel length increases. Using a MOSFET like or JFET like analytical model, the saturation current should vary as $1/L_{CHANNEL}$ but there is not enough $L_{CHANNEL}$ values (two values) to fit correctly the experimental curve. The intercell width has to be lower as possible to optimize the active area. Nevertheless, its bottom value is closed to 4 µm, below that the resistance rises a lot. With DESSIS® ISE simulations, the critical value for the intercell length is found to be 3 µm, below it the parasitic vertical JFET effect increases drastically the on-resistance.

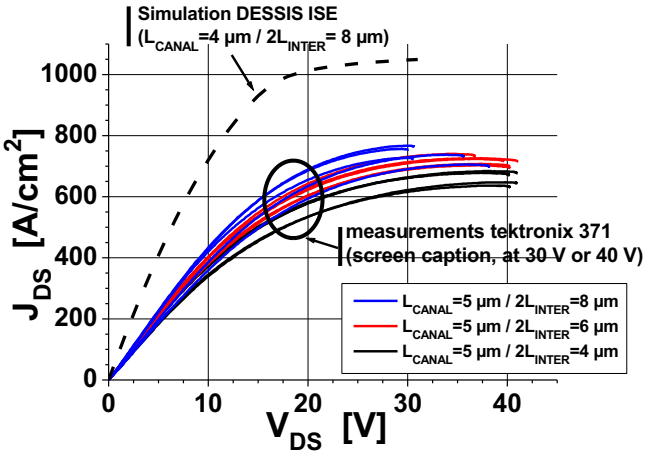

Fig. 8 : Experimental and simulated I-V characteristics of current limiting device with 5 µm for the channel length value. The saturation voltage is 15 V. The current density is calculated considering the entire source contact area.

On the fig. 9, the specific on-resistance is plotted versus the intercell width for two channel length values (4 and 5 µm). When the intercell width changes, only the access resistance change and this variation can be estimated roughly using a linear interpolation with a slope of 0.5 $m\Omega cm^2/\mu m$. While keeping constant the intercell width, it is possible to evaluate the resistance shift (linear approximation) versus the channel length value (only two points). We obtained 7 $m\Omega cm^2/\mu m$ for $dR_{ON}/dL_{CHANNEL}$.

This variation (7 $m\Omega cm^2/\mu m$) is not only due to the channel resistance variation. In fact, the source contact area decreases with an increase of the channel length : the add up $L_{CHANNEL}$ with L_{SOURCE} is kept constant in the layout. For a constant specific contact resistance value, the contact resistance (Ω) increases with the channel length as $\propto 1/\left(1-\alpha L_{CHANNEL}^2\right)$.

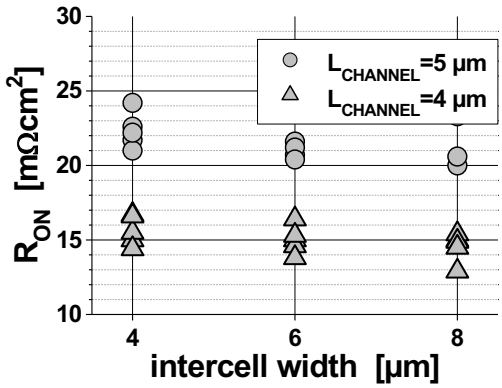

Fig. 9 : Specific on-resistances measured plotted versus the intercell width (extracted at V_{DS}=1 V) for several current limiting prototypes with different technological characteristics (channel length, $L_{CHANNEL}$ and intercell width, $2\times L_{INTER}$).

The variation of the specific on-resistance versus the channel length obtained on figure 9 is due mainly to the reduction of the active contact area and not only to the channel resistance increase. This one should vary less than 7 $m\Omega cm^2/\mu m$, as is it observed in simulation because the total on-resistance is low and the channel electron mobility seems to be as predicted in the simulated devices.

For the device with a channel length of 6 µm, the on-resistance rises to 100 $m\Omega cm^2$ due to the smallest source contact area.

IV. Conclusion

With comparing to the other devices (figure 10), already published, it seems that the IC-MOSFET belongs to the best unipolar devices built in SiC technologies. The technological steps used are common in silicon technologies (until post-implantation annealing) and only 5+1 mask levels are needed (adding a gate control should only require two levels more). The electrical characteristics experimentally obtained show a specific on-resistance of **13 mΩcm²** and a current saturation density of **900 Acm⁻²**. The I-V curves obtained are very closed to the simulated ones (DESSIS® ISE software) and are very uniform over the wafer : more than 90 % of the device are working with a spreading of electrical characteristics of 20 %.

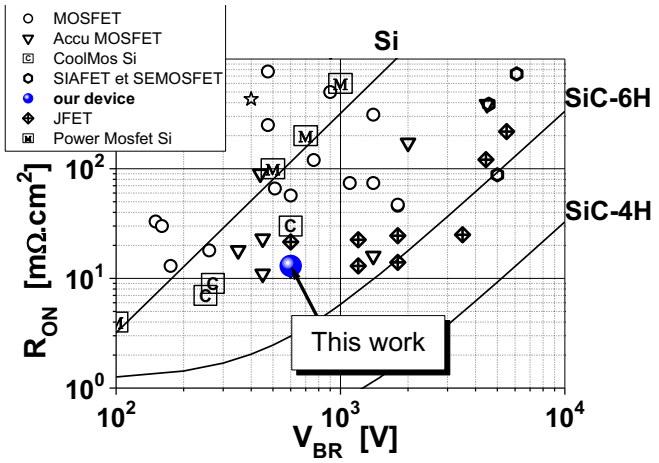

Fig. 10 : State of the art of the unipolar SiC devices (power switches) ordered by specific on-resistance versus breakdown voltage (year 2001). Only few 4H-SiC devices reach the 6H-SiC theoretical limit. The highest breakdown voltage obtained is 6.1 kV (4H-SiC SIAFET from Kansai [13]) and the best trade V_{BR}/R_{ON} is obtained with a 3.5 kV / 25 mΩcm² (4H-SiC JFET from SiCED [14])

Acknowledgments

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