SymBIST: Symmetry-based Analog/Mixed-Signal BIST

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I. Introduction

The large number of Integrated Circuits (ICs) deployed in modern safety- and mission-critical applications has created an increasing interest to avoid IC malfunctions in the field and reduce the test escapes down to sub-ppm levels. Regarding Analog and Mixed-Signal (A/M-S) ICs, many case studies have shown that the standard specification tests performed on Automated Test Equipment (ATE) offer no guarantee to meet this quality requirement [1]. To this end, performing defect-oriented Built-In Self-Test (BIST) on top of the standard specification tests and proving high defect coverage can address safety concerns. The premise of BIST in this context is that it can detect latent defects and defects that will be triggered in the context of system operation in the field provoked by environmental stress.

In this paper, we present a defect-oriented BIST strategy for A/M-S ICs, called symmetry-based BIST or *SymBIST*. We demonstrate how *SymBIST* can be successfully applied to a 65nm 10-bit Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC) IP by ST Microelectronics.

Existing works on ADC BIST focus on functional BIST [2]–[6]. The main reason for the lack of defect-oriented ADC BIST solutions is the long ADC simulation time, typically in the order of hours, which prohibits a defect simulation campaign. Thanks to the fast test time accomplished by *SymBIST*, and by using the recent mixed-signal defect simulator Tessent®DefectSim by Mentor®, A Siemens Business [7], we were able to run very fast in a automated workflow defect simulation for hundreds of defects and compute defect coverage for the entire IP.

II. *SymBIST* principle

The proposed *SymBIST* paradigm exploits existing symmetries into an A/M-S design and builds invariant properties that should hold true only in defect-free operation.

The underlying observation is that symmetries are inherent to virtually all A/M-S designs. Inherent symmetries exist thanks to fully-differential (FD) signal processing, complementary signal processing, and replication of identical blocks. For example, for node pairs carrying FD or complementary signals we can build an invariance in the form of $V_1 + V_2 = \alpha$, where V_1 and V_2 are the nodes' voltages and α is a constant, i.e., in the case of FD signals $\alpha = 2V\text{cm}$, where $V\text{cm}$ is the common mode voltage [8]. Symmetries can also be created artificially with reconfiguration using switches, duplication of blocks, or pseudo-duplication of blocks.

These invariances can be checked with a window comparator circuit implementing a comparison window $[-\delta, \delta]$, $\delta > 0$, to account for process, voltage, and temperature variations. If the invariant signal slides outside the window, then this points to defect detection.

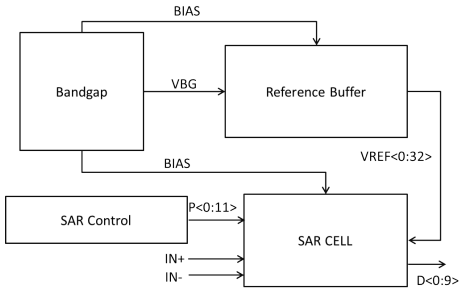

Fig. 1: Top-level architecture of SAR ADC.

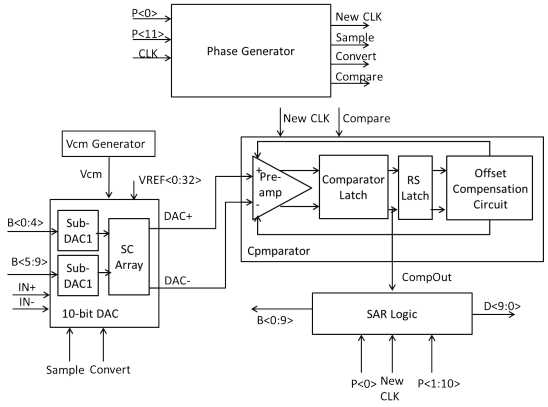

Fig. 2: SARCELL block-level architecture.

III. *SymBIST* applied to SAR ADC IP

The top-level of the SAR ADC IP architecture is illustrated in Fig. 1. The circuit accepts a FD analog input ΔIN=IN$^+$-IN$^-$. The SAR algorithm is implemented into the main SAR CELL block whose block-level architecture is shown in Fig. 2.

Looking into the architecture of the SAR ADC IP, we identified 6 invariances that hold true for any FD input ΔIN and at every conversion cycle and cover the entire A/M-S part of the SAR ADC IP. The same test stimulus is used for checking all of these invariances. In particular, the FD input ΔIN stays constant at a DC value which can be set arbitrarily and a 5-bit digital counter is used that generates all possible 2^5 bit combinations at the inputs B$< 0 : 4 >$ and B$< 5 : 9 >$ of the two sub-DACs composing the 10-bit DAC. The rationale for this dynamic part of the test stimulus is that it excites all A/M-S sub-blocks. If the 6 invariances are checked sequentially, the test is completed very fast in $6 * 2^5 \cdot (1/f_{clk}) = 1.23\mu$sec, where $f_{clk} = 156$MHz is the sampling clock frequency. This time equals about 16x the time to convert one analog input sample. A simple window comparator is designed for checking

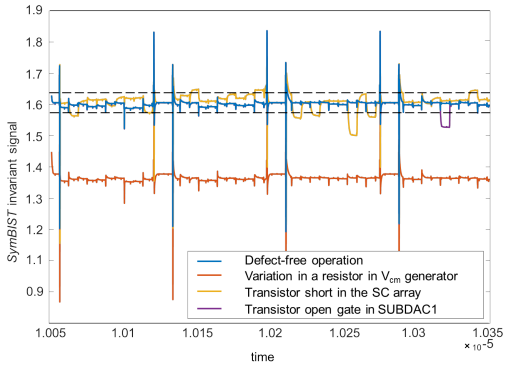

Fig. 3: Defect detection by checking an invariance signal.

Blocks	# defects	# defects simulated	defect simulation time (sec)	L-W defect coverage for k=5
BandGap	104	104	2035	94.22%
Reference Buffer	160	55	10620	1%
SUBDAC1	1260	112	2674	80.58%±6.68%
SUBDAC2	1260	112	2474	84.22%±5.89%
SC Array	44	44	1286	97.7%
V_{cm} Generator	6	6	310	30.88%
Preamplifier	24	24	700	94.12%
Comparator Latch	38	38	752	87.79%
RS Latch	40	40	983	68.09%
Offset Compensation circuit	20	20	1400	15.15%
Complete A/M-S part of SAR ADC IP	2956	101	6660	86.96%±3.67%

TABLE I: L-W defect coverage results.

an invariance composed of voltage followers and an operational amplifier. Overall, the BIST infrastructure is totally transparent to the IP incurring no performance penalties and is estimated to incur a very low and justifiable area overhead below 5%. Furthermore, the BIST can be interfaced with a standard digital test access mechanism based on two external pins which is the minimum.

IV. Results

Defects are assigned a relative likelihood of occurrence as explained in [7]. For this reason, we report the Likelihood-Weighted (L-W) defect coverage computed by the Tessent®DefectSim tool [7]. To reduce defect simulation time, we use the stop-on-detection and Likelihood-Weighted Random Sampling (LWRS) options [7]. When the LWRS option is used, the 95% confidence interval of the L-W defect coverage is also reported [7]. We rely on a standard defect model based on short- and open-circuits and 50% variation in passive components.

Fig. 3 shows in blue the invariant signal that corresponds to the sum of the differential inputs DAC+ and DAC- of the comparator. This signal should be around 1.6V in defect-free operation. In this simulation, the stop-on-detection was disabled. The two dashed horizontal lines correspond to the comparison window which has limits at $\delta = 5\sigma$ such that yield loss is negligible. The instantaneous glitches are due to the switching operation, either due to changes in the input digital test stimulus or due to the sampling and conversion operations. A clocked comparator is used to check the invariance with the checks performed when the node voltages are settled, thus no defect detection is flagged when the glitches exceed the range. The yellow, red, and purple curves in Fig. 3 show the same invariant signal in the presence of a defect in three different blocks. As it can be seen from Fig. 3, while the defect in V_{cm} generator is detectable during the entire test duration, the defects within the sub-DAC1 and SC array are detectable during specific conversion periods.

Table I shows for the various individual sub-blocks of the SAR ADC IP and for its complete A/M-S part the total number of defects, the number of defects simulated, the total defect simulation time, and the L-W defect coverage values achieved using *SymBIST*. For the entire A/M-S part of the IP, the defect coverage is $86.96\% \pm 3.67\%$. As a comparison, for two considerably smaller industrial A/M-S IPs, namely a bandgap and a power-on-reset circuit, the reported defect coverage values are 74% and 51%, respectively [7].

The low defect coverage for some sub-blocks can be explained by the non-detection of defects with very high likelihood of occurrence. In fact, the absolute defect coverage is considerably higher.

The defect simulation times are proportional to the number of defects simulated, as well to the detection time stamps since the stop-on-detection option is used. For defects that are not detected the test ends up being exhaustive.

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