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Localized VLS Epitaxy Process as a P-type Doping Alternative Technique for 4H-SiC P/N Junctions

S. Sejil[1,2], M. Lazar[2], D. Carole[1], C. Brylinski[1],
D. Planson[2], G. Ferro[1], C. Raynaud[2]
E-mail: selsabil.sejil@etu.univ-lyon1.fr

[1)] Laboratoire des Multimatériaux et Interfaces, Université de Lyon 1, 69622 Villeurbanne, France
[2)] Laboratoire AMPERE, INSA Lyon, Ecole Centrale de Lyon, CNRS, 69621 Villeurbanne, France

At present, the most popular technique for the localized P-type doping of 4H-SiC is Al ion implantation. The main drawbacks related to ion implantation are the limited activation of the Al as acceptors and the high amount of residual crystal damages, even after annealing at very high temperature [1]. In the last few years, Vapor-Liquid-Solid (VLS) selective epitaxy has been investigated as an alternative solution for the localized p-type doping of 4H-SiC [2]. One interesting result obtained with this new method has been the reduction of the resistivity of ohmic contacts on p-type 4H-SiC, for which specific resistance value as low as 1.3×10^{-6} $\Omega.cm^2$ after annealing, and ohmicity before contact annealing, have been demonstrated [3]. In the present work, we have optimized the experimental conditions of the VLS epitaxial growth, in order to obtain 4H-SiC P/N junctions. For the VLS process, the liquid phase is an AlSi melt and C_3H_8 gas is the carbon precursor.

In a previous attempt [3], only samples annealed at 1700°C after the VLS epitaxy have led to electrical behavior typical for P/N junctions, with direct bias threshold voltage V_{th} ~ 3V. Without such post-VLS annealing, a Schottky-like behavior was unexpectedly evidenced with V_{th} values in the range 1 - 2 V. In the present work, the VLS epitaxy process has been optimized, in order to get true P/N junctions without the need of high temperature annealing after the VLS process.

The VLS growth studies were performed on 6 µm thick N^- epitaxial layer, deposited on commercial 4H-SiC N^+ substrates with (0001-Si) surface (8° off). At first, 1 µm deep bowls with circular shapes have been etched into the substrate by Inductively Coupled Plasma (ICP) using SF_6 gas and a photoresist mask. Then, each bowl was locally covered by an Al-Si layers stack (~1.1 µm Si + ~1.5 µm Al) deposited by e-beam evaporation. This stack was then patterned using a combination of plasma and wet etching processes. The melting of this Al-Si stack provides the materials for the liquid phase of the VLS process (figure 1). The main parameters for the VLS growth process are: sample temperature of 1100°C, propane flow of 1 sccm, and VLS run duration of 15 min. After the VLS sequence, residual Al-Si alloy was wet-etched using alternates of acid and basic solutions.
One of the main parameters which was found to strongly influence the VLS growth process is the nature of the carrier gas, either H_2 or Ar. As shown on Fig.2a, a regular step-bunching morphology has been obtained under H_2, which suggests good epitaxial growth conditions. Under Ar, the morphology exhibits a rather disturbed step-bunching with the frequent presence of holes and pits (Fig.2b).
The deposit was found to be thinner (~ 50 nm) under H_2 compared to that under Ar (~ 900 nm).

Current-voltage plots have been performed on diodes made on both types of samples. On the back face of the N^+ substrate, classical Ni-based ohmic contacts, annealed at 900°C, were made.
Ohmic contact on the VLS P^{++} zone of the diode has been directly taken with a metal tip [3].
In direct bias, for samples with VLS growth under Ar, threshold voltage V_{th} < 3 V was observed again, while, for the samples with VLS growth under hydrogen, V_{th} ~ 3 V is reproducibly obtained (figure 3), which is the expected value for a true PN junction. After further optimization of the VLS growth process under H_2 carrier gas, thicker p-type 4H-SiC layers have been obtained, up to 500 nm, while preserving the regular step-bunching surface morphology, similar to that presented on Fig. 2a.
In conclusion, a process allowing localized epitaxy of P^+ 4H-SiC at 1100°C is now available for the fabrication of 4H-SiC PN junctions and peripheral protection.

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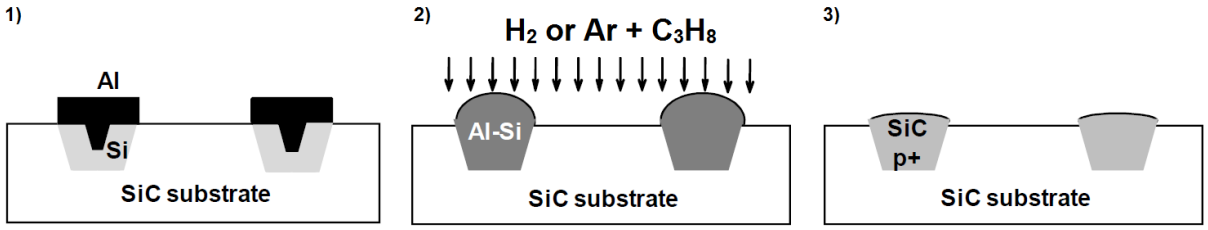

Figure 1: Schematic description of the localized VLS epitaxy process: 1) deposition of Al-Si stack inside the trenches / bowls formed by ICP in SiC, 2) melting of Al-Si and addition of propane for the VLS growth, 3) selective formation of P^+-type SiC

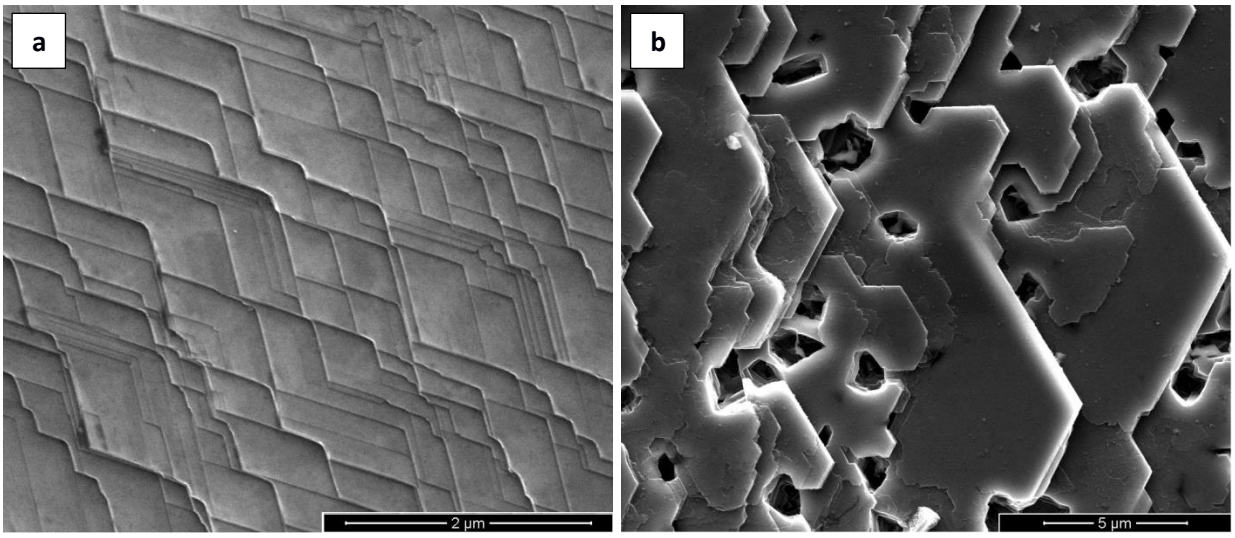

Figure 2 : Surface morphology after etching the remaining alloy on samples grown by VLS : under H_2 carrier gas (a - left), and under Ar carrier gas (b - right)

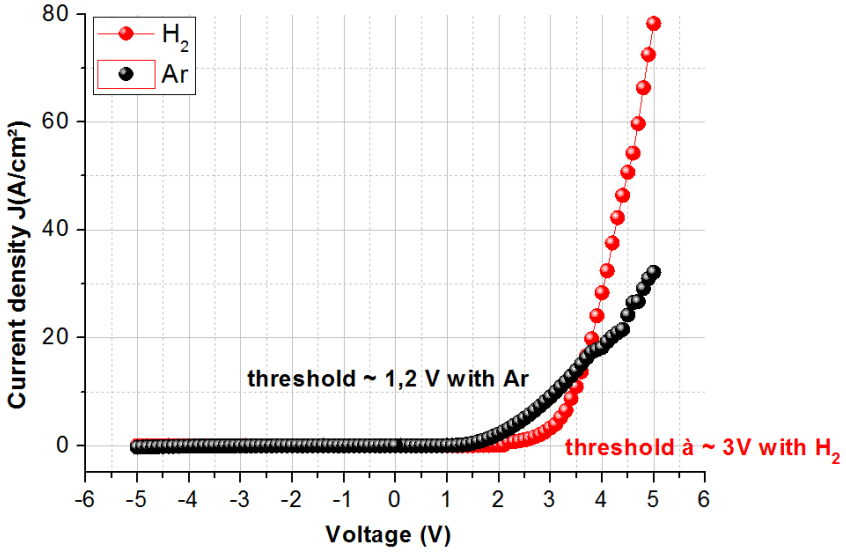

Figure 3 : Current-voltage characteristics in forward bias for P/N junctions in which P^+ material was grown by VLS : Ar carrier gas (●) vs H_2 carrier gas (●)