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Free GaAs surfaces studied using a back-gated undoped GaAs/Al_xGa_{1-x}As heterostructure

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We study the free GaAs surface by using a back-gated undoped GaAs/Al_xGa_{1-x}As heterostructure. This structure is suitable in investigating the free GaAs surface since a two-dimensional electron gas is induced by the back-gate bias in the undoped heterostructure. We compare the channel depth dependence of the transport characteristics with two different models of the free GaAs. The “midgap pinning model” assumes a constant surface Fermi level and an alternative approach called the “frozen surface model” assumes a constant surface charge density. The experimental results indicate that the frozen surface model appropriately describes free GaAs surfaces at low temperatures although the midgap pinning model is widely accepted. This is because charges cannot be transferred to the free GaAs surface at low temperatures.

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I. INTRODUCTION

A back-gated undoped heterostructure,¹⁻³ in which a two-dimensional electron gas (2DEG) is induced through the field effect, is ideal for achieving high mobility since it is free from remote-impurity scattering due to modulation doping. The advantage of the back-gated undoped structure over the front-gated undoped structure,⁴⁻⁶ is that it is easier to fabricate and there is less gate leakage because the ohmic contacts and gate are formed on the opposite sides of the sample. In addition, a back-gated undoped structure is suitable for studying the GaAs surface. This device has a free undoped GaAs surface since carriers are induced by the back gate. Therefore, the transport characteristics and operation of the device directly reflect the condition of the free GaAs surface. It is very important for us to understand and control the surface states of semiconductors for such devices as Schottky barrier diodes, metal semiconductor field effect transistors (MESFET), and metal insulator semiconductor field effect transistors (MISFET). The performance of these devices is greatly influenced by the metal-semiconductor or insulator-semiconductor interfaces. The “midgap pinning model” (MPM)⁷⁻¹⁹ is widely accepted as the GaAs surface model. The surface Fermi level is fixed at the midgap due to the large density of the surface states. However, this model implicitly assumes that charges can be transferred to the surface and a system always maintains thermal equilibrium. In conventional experimental methods for determining the surface Fermi level such as by using the current-voltage (I-V) and/or capacitance-voltage (C-V) characteristics of the Schottky contact, or x-ray photoelectron spectroscopy (XPS), it is clear that charges are easily transferred to the surface. In Schottky contacts, charges are transferred from the metal gate, and in XPS, charges are generated by photoexcitation. It is also reasonable to assume that, at room temperature, charges move by thermionic emission and a system is in equilibrium. However, it is not obvious if thermal equilibrium is also achieved for free GaAs surfaces at low tem-

peratures. In this situation, the transfer of charges to the surface seems to be rather difficult. Recently, many types of low-dimensional systems have been fabricated based on GaAs/Al_xGa_{1-x}As heterostructures. Conventional methods for the formation of fine patterns use surface Schottky gate and/or surface etching. Thus, they have a free semiconductor surface as well as a surface covered with metal. When modeling the electrostatics of these devices, we need to know the surface condition of free semiconductor surface to determine the boundary conditions. In addition, we usually operate these devices at low temperatures to enable us to see weak quantum-mechanical effects. Therefore, it is very important to study the free surface of (Al)GaAs at low temperatures.

An alternative surface model called the “frozen surface model” (FSM)²⁰⁻²⁴ has been proposed and investigated for the free surface of (Al)GaAs. This model assumes a constant surface charge density for the free semiconductor surface. Because the surface charge density is directly related to the surface electric field, it is equivalent to assuming a constant surface electric field. The difference between MPM and FSM lies in the difference in the given boundary condition. In the MPM, the constant potential is given and in the FSM, the differential of the potential, namely the electric field, is given. Laux and co-workers²⁰ theoretically calculated the energy level of the quantum wire formed by a split surface-gate structure on a GaAs/Al_xGa_{1-x}As heterostructure based on the FSM. They assumed a constant surface charge at the free GaAs surface between the gates. Davies, Larkin, and co-workers²¹⁻²³ also theoretically calculated the electrostatic potential formed by the patterned surface gate. They compared their results for split-gate surface superlattices with experimental results.²⁵ They analyzed the second harmonics of the commensurability oscillation of the magneto resistance. Although they support the FSM, the difference between the two models is small and the effect of the strain caused by the gate metal deposition is large. Recently, Ali and co-workers²⁴ measured the depletion capacitance of a finger-shape split type surface-gate fabricated on a

FIG. 1. A schematic cross-section of the undoped GaAs/Al_xGa_{1-x}As heterostructure. The whole structure is undoped except for the *n*-GaAs used as a back-gate. For some devices, the central region is chemically etched to vary the channel depth. 2DEG is induced at the GaAs/Al_xGa_{1-x}As interface by applying a positive bias to the back gate.

GaAs/Al_xGa_{1-x}As heterostructure. They compared experimentally determined threshold voltages with the calculated value using both the MPM and the FSM. They concluded that the FSM accurately describes their data and the pinning model predicts very different values.

In this paper, we study the surface state of free GaAs by using the back-gated undoped GaAs/Al_xGa_{1-x}As heterostructure shown in Fig. 1. The whole device surface is a free GaAs surface since 2DEG is induced only by the back gate. Therefore, the transport characteristics well reflect the condition of the free GaAs surface. The threshold voltage of the back-gate bias is directly related to the surface charge density since no structures are formed on the surface. We analyze experimental results based on a simple capacitance model and assuming both the MPM and FSM for the free GaAs surface. Our devices are based on a high-quality undoped GaAs/Al_xGa_{1-x}As heterostructure as shown in Fig. 2. The highest mobility reaches the 5×10^6 (cm²/Vs) and the carrier density has a linear relationship with the back-gate bias. Therefore, we can analyze the system on the assump-

FIG. 2. 2DEG mobility as a function of carrier density. The highest mobility reaches 5×10^6 (cm²/Vs). The inset shows the relation between the carrier density and the back-gate bias voltage. The linear relation indicates that the undoped layers act as a good insulator. This result is obtained from device D3 at 1.5 K.

tion that the undoped layers act as a good impurity-free insulator and that there is no parallel conduction at the surface. After summarizing the experiments in Sec. II, we discuss the low-temperature characteristics of devices with deep channels in Sec. III. We analyze the operation using two different models (MPM and FSM) for the free GaAs surface and we show that the FSM is an appropriate model for a free GaAs surface with no charge transfer. In Sec. IV, based on the FSM, we discuss the effect of the charge transfer from the 2DEG to the surface. We explain the increase in the threshold voltage by considering the increase in the surface charge density. Tunneling plays a significant role in the charge transfer for shallow channels. At higher temperatures the charges are transferred by thermionic emission.

II. EXPERIMENTS

We grow the starting layer structure for the back-gated system shown in Fig. 1 by molecular beam epitaxy (MBE). We successively grow a 1- μ m-thick Si-doped *n*-type GaAs buffer layer, an AlAs (2 nm)/GaAs (2 nm) superlattice barrier layer, a 20-nm-thick Al_{0.33}Ga_{0.67}As barrier layer, and a GaAs channel layer on an *n*-type (100) substrate. All the layers are undoped except for the *n*-type GaAs layer that we use as the back gate. For the sample, we use for a temperature-dependence measurement, we replace the barrier layer with an AlAs (2.5 nm)/Al_{0.33}Ga_{0.67}As (5 nm) superlattice. The AlAs/Al_xGa_{1-x}As barrier layer reduces the back-gate leakage-current that increases with increasing the temperature. However, the mobility decreases because of the increase in the interface roughness. After MBE growth, the wafer is taken out to the atmosphere and we form a field-effect transistor (FET) with a Hall bar shape by using a conventional photolithographic technique. We provide no special surface treatment during the processing. The Hall bar structure is defined by mesa etching along the [011] direction. We deposit Au-Ge-Ni electrodes both on the surface and the back in a vacuum evaporator and anneal them to form the ohmic contacts and the back gate. We undertake the annealing procedure in a hydrogen atmosphere at a temperature of around 400°C. After forming the ohmic contacts, we cover the electrode regions with photoresist and chemically etch the central region of the Hall bar by using an H₂SO₄-H₂O₂-H₂O system to vary the channel depth. To observe the channel depth dependence, we prepare several samples with different channel depths starting from two wafers whose GaAs channel layers have different thicknesses as summarized in Table I. We also examine the difference in barrier layer thickness.

We evaluate the transport characteristics by measuring the Hall effect in a ⁴He cryostat system. We obtain the carrier density and mobility as a function of the back-gate bias voltage. We use a low-magnetic field of 0.1 T for the Hall voltage measurement. The applied drain-source voltage is sufficiently small compared with the back-gate bias, therefore, we are able to consider the potential of the drain and source as a ground.

TABLE I. Structure of the devices used in the experiment and the measured threshold voltage. We use six different wafers (*A–F*). *A1–A3* are made by chemically etching from wafer *A* and *B1, B2* are etched from wafer *B*. *D–D3* indicate the variation of the surface state of the different part of the same wafer. The threshold voltages for *B2* increases by repeating the measurement. Two values correspond to first (second) scan of the back-gate bias voltage.

Sample	Channel depth d_1 (nm)	Barrier thickness d_2 (nm)	Threshold voltage V_{bth} (V)
<i>A</i>	250	420	0.66
<i>A1</i>	205	420	0.79
<i>A2</i>	160	420	0.76
<i>A3</i>	110	420	0.68
<i>B</i>	100	420	0.60
<i>B1</i>	70	420	1.20
<i>B2</i>	54	420	1.93 (2.35)
<i>C</i>	250	620	0.91
<i>D</i>	150	620	0.81
<i>D1</i>	150	620	0.66
<i>D2</i>	150	620	0.65
<i>D3</i>	150	620	0.56
<i>E</i>	500	820	0.56
<i>F</i>	220	375	0.67

III. LOW TEMPERATURE CHARACTERISTICS

A. Experimental results

We first cool the devices from room temperature to the lowest temperature of 1.5 K without operating them. Then we operate the devices by applying a back-gate bias and measure the Hall effect. Figure 3 shows the measured carrier densities at various channel depths (sample *A–A3, B–B2*) as a function of the back-gate bias voltage. For all samples, the

FIG. 3. Carrier densities (sample *A–A3, B–B2*) as a function of the back-gate bias voltage for various channel depths. The barrier layer is the same in each case (420 nm). The carrier density (n) is proportional to the back-gate bias voltage (V_b) and the slope ($\partial n / \partial V_b$) is identical. Channel depths are $\oplus$: 250 nm; $\odot$: 205 nm; $\triangle$: 160 nm; $\square$: 110 nm; ∇ : 100 nm; $\circ$: 70 nm; and $\otimes$: 54 nm (first and second). The threshold voltages for deep channels (>100 nm) are almost constant at various channel depths. At the 70-nm deep channel, the threshold increases slightly and at the 54-nm deep channel, it increases when the measurement is repeated.

carrier density (n) is proportional to the back-gate bias voltage (V_b) and the slope ($\partial n / \partial V_b$) is about $1.3 \times 10^{11} \text{ cm}^{-2}/\text{V}$. This value is identical to the value determined from the barrier layer capacitance. This linear relationship between the carrier density and the back-gate bias indicates that the barrier layer acts as a good insulator. Based on the experimental results, we construct a model for the operation of this device. We use a simple capacitance model consisting of three electrodes; the back-gate, the 2DEG at the interface, and the surface. We consider the operations before and after the threshold separately.

After the threshold, the operation is simple and clear. As shown in Fig. 3, the carrier density is proportional to the back-gate bias (V_b) and the slope is the capacitance of the barrier layer. Therefore, the carrier density (n) is expressed as

$$n = \frac{\epsilon_2}{d_2 e} (V_b - V_{bth}), \quad (1)$$

where V_{bth} is the threshold of the back-gate bias voltage, and ϵ_2 and d_2 are the average dielectric constant and the thickness of the barrier layer, respectively. Once a 2DEG is formed at the GaAs/ $\text{Al}_x\text{Ga}_{1-x}\text{As}$ interface, the back-gate bias is applied only between the 2DEG and the back-gate.

We next discuss the mechanism that determines the threshold voltage (V_{bth}). Threshold voltages estimated from the experimental results are plotted as a function of the channel depth in Fig. 4. We directly estimate the surface charge density at the threshold (Q_{sth}) shown in the inset of Fig. 4 from the measured threshold voltage as expressed by,

$$Q_{sth} = \frac{\epsilon_2}{d_2 e} V_{bth}. \quad (2)$$

FIG. 4. Estimated threshold voltage (sample A-A3,B-B2) plotted as a function of the channel depth. For deep channels (> 100 nm), the thresholds are almost the same. The threshold voltage rapidly increases when the channel depth is less than 100 nm. The inset shows the surface charge density calculated from the threshold voltage as a function of the channel depth. The measured surface charge densities are much lower than those expected from the surface pinning model.

Since there are no charges at the interface at the threshold, the electric field both in barrier and channel layers are determined only by the threshold voltage. Therefore, we determine Q_{sth} solely from the thickness of the barrier layer and V_{bth} . It is independent of the surface model. It should be noted that the threshold voltages (V_{bth}) and the surface charge density at the threshold (Q_{sth}) for deep channels (> 100 nm) are almost the same. For the sample with the 70-nm-deep channel, the threshold voltage becomes higher. For the 54-nm-deep channel, the threshold voltage increases when the back-gate bias scan is repeated during the experiment. In this section, our discussion is concentrated on the threshold for deep channels. The model must explain the constant nature of the threshold. To determine the threshold voltage theoretically, we need an appropriate model for the surface condition of the free GaAs. We consider two different models for the GaAs surface and compare the results with experimental data. In the widely accepted midgap pinning model, the surface Fermi level is constant and it is fixed at the middle of the bandgap. In the frozen surface model, surface charge density, namely the surface electric field, is constant.

B. Midgap pinning model

We consider the system that is shown schematically in Fig. 5(a). From the charge neutrality and the Gauss theorem, the system is described as

$$\frac{V_b + \Phi_i}{d_2} = \frac{Q_b}{\epsilon_2}, \quad (3)$$

$$\frac{\Phi_s - \Phi_i}{d_1} = \frac{Q_s}{\epsilon_1}, \quad (4)$$

$$Q_b = Q_s + en, \quad (5)$$

FIG. 5. Schematic band diagram for the operation of a back-gated undoped GaAs/Al_xGa_{1-x}As heterostructure assuming the MPM. Note that the surface Fermi level (Φ_s) is constant and fixed at the midgap. (a) Before the threshold (thin solid line), bias is applied between the surface and the back gate. The potential at the interface Φ_i decreases with increasing bias voltage. The threshold voltage (V_{bth}) is defined as the point where Φ_i reaches the Fermi level (E_f) (thick solid line). After the threshold (thin dashed line), bias is applied between the 2DEG and the back gate thus, the carrier density increases linearly with increasing back-gate bias voltage. (b) The threshold voltage (V_{bth}) increases with decreasing channel depth since Φ_s is constant. (Compare thick and thin solid lines.)

where Q_b and Q_s are the charge densities at the surface and the back gate, n is the carrier density of the 2DEG, Φ_i and Φ_s are the potential at the interface, and the surface Fermi level measured from the conduction band edge, d_1 , ϵ_1 , and d_2 , ϵ_2 are the thickness and dielectric constant of the channel and the barrier layer, respectively. V_b is defined in the reverse direction so as to represent directly the back-gate bias voltage. This definition is convenient in terms of comparing the model with the experimental data. Note that in the MPM, the surface Fermi level Φ_s is constant. Throughout our discussion, we set the zero point of the potential (ground) at the source ohmic contact. From Eqs. (3)–(5), we obtain the following relations by eliminating Q_b and Q_s ,

$$en - \left(\frac{\epsilon_2}{d_2} + \frac{\epsilon_1}{d_1} \right) \Phi_i = \frac{\epsilon_2}{d_2} V_b - \frac{\epsilon_1}{d_1} \Phi_s. \quad (6)$$

Before the threshold, charges corresponding to the applied bias accumulate only at the surface and the back gate and there are no charges at the interface. The back-gate bias is applied between the surface and the back gate. Putting $n = 0$ in Eq. (6), the potential at the interface and the surface charge density are expressed as

$$\Phi_i = \frac{d_2}{(\epsilon_2/\epsilon_1)d_1 + d_2} \Phi_s - \frac{d_1}{d_1 + (\epsilon_1/\epsilon_2)d_2} V_b, \quad (7)$$

$$Q_s = \frac{\epsilon_2 \epsilon_1}{\epsilon_2 d_1 + \epsilon_1 d_2} (V_b + \Phi_s). \quad (8)$$

As the back-gate bias is increased, Φ_i decreases and Q_s increases.

At the threshold voltage, the potential at the interface reaches the Fermi level (E_f) and the 2DEG starts to be formed. We neglect the energy level of the 2DEG confined at the hetero interface since it is sufficiently small compared with the back-gate bias. Therefore, putting $\Phi_i = 0$, in Eqs. (7) and (8), the threshold voltage (V_{bth}) and the surface charge density at the threshold (Q_{sth}) are described as

$$V_{bth} = \frac{d_2}{d_1} \frac{\epsilon_1}{\epsilon_2} \Phi_s, \quad (9)$$

$$Q_{sth} = \frac{\epsilon_1}{d_1} \Phi_s = \frac{\epsilon_2}{d_2} V_{bth}. \quad (10)$$

After the threshold, Φ_i is kept at zero and the bias is applied between the 2DEG and the back gate. From Eqs. (6) and (7), the carrier density and surface charge density are expressed as

$$n = \frac{\epsilon_2}{d_2 e} V_b - \frac{\epsilon_1}{d_1 e} \Phi_s = \frac{\epsilon_2}{d_2 e} (V_b - V_{bth}), \quad (11)$$

$$Q_s = Q_{sth} = \frac{\epsilon_1}{d_1} \Phi_s. \quad (12)$$

The carrier density is proportional to the back-gate bias and its slope is determined by the capacitance of the barrier layer. The surface charge density is constant.

The threshold voltages calculated with Eq. (9) are plotted in Fig. 6 as a function of the channel depth together with the measured data. Many values have been reported for the pinning position of the surface Fermi level.⁷⁻¹⁹ They range from about 0.5 to 1.2 V below the conduction band edge, depending on such factors as the semiconductor carrier type, the surface orientation, the surface-gate metal, and the surface treatment. In the calculation, we assume that the surface Fermi level (Φ_s) is pinned at 0.96 V below the conduction band edge.¹⁹ This value is obtained from the experiment for the free GaAs surface using the contactless capacitance method. The following analysis is not significantly influenced by the variation of the pinning position of the surface Fermi level. Since the surface Fermi level (Φ_s) is constant, the threshold voltage increases with decreasing channel depth as shown in Fig. 5(b) for the same barrier layer thickness. When we compare the calculated results with the experimental data shown in Fig. 6, the former depend strongly on the channel depth and are much larger than the latter. This discrepancy indicates that the MPM is not appropriate for the free surface of GaAs at low temperatures.

C. Frozen surface model

To explain the above discrepancy, we consider an alternative condition for the free GaAs surface. The constant na-

FIG. 6. Measured (filled symbols), calculated with the MPM (open symbols) and the FSM (cross symbols) are plotted as a function of channel depth. Different marks correspond to different barrier layer structures. To see the validity of the model, values corresponding to different barrier thicknesses are plotted in the same graph. The surface Fermi level at a state of equilibrium is assumed to be 0.96 V below the conduction band edge. For a deep channel (> 100 nm), the measured data are well explained by the FSM. When the channel depth is less than 100 nm, the threshold voltage increases rapidly and moves closer to the value expected from the MPM.

ture of the threshold voltage indicates that the surface electric field, and therefore the surface charge density, is constant at the threshold. Accordingly, we assume that the surface charge density is constant for the free GaAs surface. This assumption means that the system is not in a state of thermal equilibrium when under an applied bias because charges cannot be transferred to the surface. The surface Fermi level is not defined in this situation. In addition, we need the surface charge density accumulated at thermal equilibrium to obtain the finite threshold voltage. It is valid to assume that the surface charge density is determined by the surface Fermi level in a state of equilibrium (Φ_{s0}) determined only by the n -type back gate and the surface at room temperature. Therefore, putting $V_b = 0$ in Eq. (8), Q_s is given by

$$\Phi_{s0} = \left(\frac{d_2}{\epsilon_2} + \frac{d_1}{\epsilon_1} \right) Q_s. \quad (13)$$

We start the analysis with Eqs. (3), (4), and (13). A schematic band diagram is shown in Fig. 7. Note that surface charge density (Q_s) is constant and the surface potential is floating. Equation (5) is not used since Φ_s is not defined in this model. From Eqs. (3) and (4), we obtain

$$en - \frac{\epsilon_2}{d_2} \Phi_i = \frac{\epsilon_2}{d_2} V_b - Q_s. \quad (14)$$

Before the threshold, a back-gate bias is applied between the source (fixed to the ground) and the back gate. Thus, the potential at the interface is expressed as

$$\Phi_i = \frac{d_2}{\epsilon_2} Q_s - V_b, \quad (15)$$

FIG. 7. Schematic band diagram for the operation of the back-gated undoped GaAs/Al_xGa_{1-x}As heterostructure assuming the FSM. Note that the surface charge density (Q_s) is constant. Thus, the surface potential is floating and the system is not in a state of thermal equilibrium. (a) Before the threshold (thin solid line), bias is applied between the source and the back gate. The potential at the interface Φ_i decreases with increasing bias while keeping the electric-field constant. The threshold voltage (V_{bth}) is defined as the point where Φ_i reaches the same level as the source (ground) (thick solid line). After the threshold (thin dashed line), bias is applied between the 2DEG and the back gate and the carrier density increases linearly with increasing back-gate bias voltage. (b) The channel depth dependence of the threshold is much weaker and almost constant. (Compare thick and thin solid lines.)

since no charges are accumulated at the interface. Under the ohmic contacts, charges corresponding to the applied bias may be accumulated somewhere around the ohmic contacts and the n -type back gate. However, in the central region of the device, charge densities Q_b and Q_s retain their initial values. Accordingly, the potential of the whole layer becomes lower while maintaining the initial electric field as shown in Fig. 7(a).

At the threshold voltage, the potential of the interface (Φ_i) reaches the same level as the source (ground) and 2DEG starts to form. When we put $\Phi_i = 0$ in Eq. (15) and use the relation in Eq. (13), the threshold voltage is given by

$$V_{bth} = \frac{d_2}{\epsilon_2} Q_s \quad (16)$$

$$= \frac{d_2}{d_2 + (\epsilon_2/\epsilon_1)d_1} \Phi_{s0}. \quad (17)$$

The threshold voltage is determined only by the surface charge density, which is given by the surface Fermi level in a state of equilibrium (Φ_{s0}). We also plot the threshold voltage calculated using Eq. (17) in Fig. 6. The assumed surface Fermi level at equilibrium (Φ_{s0}) is the same as that used in the MPM (0.96 V below the conduction band edge) because we consider the Fermi level to be pinned at the midgap at room temperature where the system is at equilibrium. As expressed in Eq. (17), the threshold value depends on the

FIG. 8. Schematic band diagram of the increase in the threshold voltage. Note that the system is nonequilibrium in FSM. When the channel depth is less than 100 nm, charge transfer from the 2DEG to the surface becomes significant. The system moves closer to thermal equilibrium (thick solid line) due to the charge transfer. The surface charge density increases and the surface electric field becomes stronger. Therefore, the threshold voltage becomes higher.

channel depth even in FSM. However, its dependence is much weaker than that in the MPM. As seen in Fig. 6, the experimental results agree well with the calculated values.

After the threshold, the operation is the same as that in the MPM. Φ_i is kept at zero and the carrier density n is expressed as

$$n = \frac{\epsilon_2}{d_2 e} \left(V_b - \frac{d_2}{(\epsilon_2/\epsilon_1)d_1 + d_2} \Phi_{s0} \right) = \frac{\epsilon_2}{d_2 e} (V_b - V_{bth}). \quad (18)$$

It is clear that the appropriate model for the free GaAs surface is the FSM rather than the widely accepted MPM.

IV. CHARGE TRANSFER TO THE SURFACE

For deep channels at a low temperature, device characteristics are well explained by the FSM. Therefore, we use the FSM as a basis for discussing the threshold increase for shallow channels. Since the system is substantially nonequilibrium in the FSM, we have to consider the increase in the surface charge density caused by the charge transfer from the 2DEG to the surface. With increasing surface charge density, the threshold voltage increases as expected from Eq. (16). We observe an increase in the threshold for devices with a channel depth of less than 100 nm. This is because of the tunneling of the electrons from the 2DEG to the surface since the tunneling effect becomes significant with the shallow channels. After the formation of the 2DEG at the interface, electrons are transferred to the surface by this tunneling and they are trapped by the deep levels at the surface because the system is not at a state of thermal equilibrium as shown in Fig. 8. The increase in the surface charge density causes an increase in the surface electric field. This makes the potential barrier higher and the tunnel probability less. Repeating this process, the system becomes stable when the tunneling probability becomes effectively zero. Through this process the threshold voltage moves higher and the system moves closer to thermal equilibrium. For a 54-nm channel depth, this process continues in of the order of minutes as seen in Fig. 3. The threshold voltage increases when the measurement is repeated. For the deep channels, the tunneling probability is so small that charge transfer to the surface is negligible within the usual measurement time. The threshold voltage is nearly constant.

FIG. 9. Carrier densities as a function of the back-gate bias voltage at various temperatures (sample *F*). From 1.5 to 100 K (open circles), the threshold voltage is the same. When the temperature is increased to 120 K (open triangles), the threshold starts to shift due to the charge transfer to the surface by thermionic emission. When the device is operated for one and a half hours, the threshold voltage increases further. After this, the temperature is set at 1.5 K (filled circles) again. The threshold voltage is the same as that of the second scan at 120 K.

We measure the temperature dependence to examine the validity of this charge transfer. It is reasonable to assume that electrons are transferred by thermionic emission at higher temperatures. In this experiment we use a device with a 250-nm channel depth (sample *F*). To reduce the leakage current between the back gate and the ohmic contacts at higher temperatures, we change the structure of the barrier layer to an $\text{AlAs}/\text{Al}_x\text{Ga}_{1-x}\text{As}$ superlattice. The thickness of the barrier layer is 375 nm. First, the device is directly cooled to 1.5 K without being operated. At 1.5 K, we operate the device and perform the Hall measurement. After the measurement, we reset the back-gate bias to 0 V and increase the temperature to 20 K. We perform the same measurement repeatedly by increasing the temperature to 120 K. Figure 9 shows the measured temperature dependence of the relationship between the carrier density and the back-gate bias. From 1.5 to 100 K (open circles), the characteristics are identical. The estimated threshold voltage is constant at 0.67 V. The surface charge density estimated by the Eq. (16) is $1.3 \times 10^{11} \text{ cm}^{-2}$. When we increase the temperature to 120 K (open triangles), the threshold voltage starts to increase. At the first scan, the threshold voltage increases to 0.71 V. The surface charge density corresponding to this threshold value

increases to $1.4 \times 10^{11} \text{ cm}^{-2}$. To observe the dynamic change of the threshold, we set the back-gate bias at 1.1 V and we keep this condition for one and a half hours, after the first scan. We then perform the same measurement again. At the second scan, the threshold increases further to 0.77 V and the surface charge density increases to $1.5 \times 10^{11} \text{ cm}^{-2}$. To confirm that this threshold shift is caused by the increase in the surface charge density due to the thermionic emission of electrons from the 2DEG to the surface, we perform the measurement at 1.5 K again. We reset the back-gate bias to 0 V and cool the sample to 1.5 K. At the second scan at 1.5 K (filled circles), we observe no change in the threshold voltage. The measured threshold voltage is the same as that obtained with the second scan at 120 K as seen in Fig. 9. Therefore, it is clear that at a low temperature, the thermionic emission is sufficiently small and the surface charge density is effectively constant.

V. CONCLUSION

We studied the free GaAs surface by using a back-gated undoped $\text{GaAs}/\text{Al}_x\text{Ga}_{1-x}\text{As}$ heterostructure. We measured the channel depth dependence of the transport characteristics. The measured threshold voltage was almost the same for various channel depths. We analyzed experimental results based on the MPM and FSM for a free GaAs surface. We showed that the frozen surface model is the appropriate model for a free GaAs surface at low temperatures. This is because charges cannot be transferred to the surface at low temperatures. The surface charge density is constant, thus contradicting the widely accepted midgap pinning model. By considering the increase in the surface charge density caused by tunneling from the 2DEG to the surface, we can explain the increase in the threshold voltage seen for devices with shallow channels. At higher temperatures, charges are transferred by thermionic emission. Therefore, the FSM is an appropriate model for free GaAs surfaces at low temperatures. This characteristic is promising as regards applying the back-gated undoped $\text{GaAs}/\text{Al}_x\text{Ga}_{1-x}\text{As}$ heterostructure to fine pattern devices since it means a shallow 2DEG can be formed.

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