A Vector Modulation Strategy for Open-End Winding Conversion Systems

Frederico F. V. Matos*, Herbert O. Ramos*, Caio E. Oliveira*, Victor F. Mendes*

Marcos A. S. Mendes* and Thierry Meynard†

*Graduate Program in Electrical Engineering

Federal University of Minas Gerais, Brazil

Email: fredmatos@ufmg.br †Institut National

Polytechnique de Toulouse

University of Toulouse, France

Abstract—With the increasing demand for industrial processes for power rating, quality and faster dynamics, multilevel converters and structures have been developed and became popular. Among them, the open-end winding topology is an advantageous structure for its lower device count and switching redundancy.

This paper presents a vector modulation technique for one of these systems, which employs a pair of two-level converters, being equivalent to a traditional three-level system. The strategy uses the nearest space vectors to the reference in order ensure a good power quality on the output. Its main features are the balance of commutations among devices, its constant switching rate and the higher frequency current ripple.

The characteristics of the fixed switching patterns to obtain the best quality on the output are presented along with simulation results that demonstrate the accomplishment of the strategy goals.

Index Terms—Open-End Winding, Modulation Techniques, Space Vector Modulation, Power Conversion.

I. INTRODUCTION

Over the last decades, several multilevel converter topologies were developed in order to achieve superior power, energy quality or dynamics than the traditional two level structure. Among them, the neutral point clamped (NPC), flying capacitor (FC) and cascaded H-bridge (CHB) achieved higher acceptance and became widely known [1].

The open-end winding (OEW) drive system is a connection scheme that uses two power converters to achieve a higher number of voltage levels in the electrical machine than the converters are individually capable of. It was first presented by Guggenbach and Stemmler in 1993 [2]. Fig. 1 shows a system that employs two-level converters in an open winding configuration, corresponding to a three-level drive.

The main advantages of this structure are the lower device count compared to traditional Δ/Y systems, the amount redundant switching states, and the absence of the capacitor voltage balance problems present in NPC or FC converters. However, in order to avoid the circulation of common-mode currents, the dc-links must be isolated in the grid side [2].

OEW structures have been reported for several applications, such as electrical and hybrid vehicles [3], aerospace [4], water pumping solar systems [5], [6] and wind power [7], [8], to name a few. Also, the combination of power converters

Fig. 1. Open end winding drive.

with different number of levels [9], [10] and type (fullycontrolled, semi-controlled or uncontrolled) [11], [12] have been proposed.

As for the modulation, several techniques were developed specifically for OEW systems, as the sub-hexagon strategies in [13]–[15] and the carrier based in [16]–[18]. These techniques, however, propose an alternating role between converters: one is clamped while the other is effectively switched.

In this work, a vector modulation technique is presented where all switches are switched constantly and the voltage reference nearest space vectors are used in order to achieve the best performance with respect to harmonic distortion. These characteristics are particularly interesting for high power, high voltage devices.

II. MODULATION TECHNIQUE

Fig. 2 presents the voltage space vectors produced in the machine windings by the system from Fig. 1. There are 19 distinct space vectors (including the null vector), with $2^6 = 64$ different switching states.

The space vector modulation technique consists of applying the vectors located closest to the reference voltage space

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Fig. 2. Voltage space vectors for the three-level power converter.

vector in such a manner that their linear combination over one switching period corresponds to the reference vector. The nearest vectors depend on the magnitude and angle of the reference and can be found by dividing the hexagon of space vectors produced by the system into triangular regions, as shown in Fig. 2.

Six sections are named from A to F, depending on the angle of the reference vector, and each section is divided in triangular subsections from 1 to 4. When the reference voltage is inside one specific region, the vertexes of that region correspond to the nearest voltage space vectors i.e., when in region A4, vectors V_3 , V_4 and V_5 are the closest vectors.

Fig. 2 also shows that for every region there are three time variables, t_a , t_b and t_c , each associated to one of the triangle vertexes. When each vertex is applied for its corresponding time, their linear combination in one switching period corresponds to the reference voltage. They are obtained by solving the system of equations

$$\mathbf{V}_a t_a + \mathbf{V}_b t_b + \mathbf{V}_c t_c = \mathbf{V}_{ref} T_s \quad (1)$$

$$t_a + t_b + t_c = T_s$$

where T_s is the switching period, $\mathbf{V}_{ref} = V^* e^{j\theta}$ is the reference vector and V_a , V_b and V_c are the vectors associated to t_a , t_b and t_c , depending on the region. For region A4, as an example, $V_5 = 2V_{dc}e^{j60^\circ}$ corresponds to t_a , V_3 to t_b , and V_4 to t_c . The solutions of (1) for each subsection were presented by [19] and are comprised in Table I. In the resulting

expressions, the modulation index is $k = V^*/(V_{dc}\sqrt{3})$ and the angle is $\theta' = \theta \pmod{60^\circ}$.

A. Switching Patterns

While the time variables calculation is not related to the converter topology itself but to the number of levels; the next step in the modulation technique is intimately related to the structure. It is the selection of which switching states are to

Fig. 3. Possible vector transitions for region A2.

be used in order to apply the corresponding vectors, and on what sequence.

To facilitate the representation of the switching states, we will use decimal numbers that, converted to a 6-bit binary number, represent the switches S1 to S6, from the least to the most significant bit. To exemplify: vector 19 corresponds to the switching state 010011, which means that switches S1, S2 and S5 are closed.

Fig. 3 presents the switching states for vectors V1, V2 and V3, that define region A2. The arrows linking each state correspond to possible direct transitions, where only one switch is commutated.

In order to identify the best possible switching patterns (or sequences) regarding power quality and loss distribution among devices, some conditions were determined: • The patterns should have the highest number of states as possible, in order to reduce the current ripple;

- The switching frequency should be the same for all six converter legs, in other words during a switching period each device can commutate two times only;
- The resulting voltage waveform must be symmetrical: there are switching patterns that produce waveforms with full symmetry around half the switching period, and the resulting voltages are centered around one quarter. That results in higher frequency current ripple;
- The starting (and ending) switching states of the patterns for each region are chosen in order to reduce the commutation number when the reference moves to a neighbor region. As an example, regions A1, A2, A3 and F4 share the vector V1, so we'll choose the same V1 state (01 for example) to begin these regions patterns. The same is valid for B1, B2, B3 and A4 with vector V4, and so on.

Taking those constraints into account, we could identify a considerable number of distinct switching patterns for each one of the regions. Fig. 4 presents one of these patterns, for

TABLE I EQUATIONS FOR
VECTOR APPLICATION TIME PERIODS.

Subsection	t_a	t_b	t_c
1	$2kT_s \text{sen} \left(\frac{\pi}{3} - \hat{\theta} \right)$	$T_s \left[1 - 2k \text{sen} \left(\hat{\theta} + \frac{\pi}{3} \right) \right]$	$2kT_s \text{sen} \left(\hat{\theta} \right)$
2	$2T_s \left[1 - k \text{sen} \left(\hat{\theta} + \frac{\pi}{3} \right) \right]$	$2kT_s \text{sen} \left(\hat{\theta} \right)$	$T_s \left[2k \text{sen} \left(\frac{\pi}{3} - \hat{\theta} \right) - 1 \right]$
3	$T_s \left[1 - 2k \text{sen} \left(\hat{\theta} \right) \right]$	$T_s \left[2k \text{sen} \left(\hat{\theta} + \frac{\pi}{3} \right) - 1 \right]$	$T_s \left[2k \text{sen} \left(\hat{\theta} - \frac{\pi}{3} \right) + 1 \right]$
4	$T_s \left[2k \text{sen} \left(\hat{\theta} \right) - 1 \right]$	$2kT_s \text{sen} \left(\frac{\pi}{3} - \hat{\theta} \right)$	$2T_s \left[1 - k \text{sen} \left(\hat{\theta} + \frac{\pi}{3} \right) \right]$

Fig. 4. Switching pattern for region A2.

region A2, and its corresponding command pulses over one switching period.

One can notice that the pattern is composed of 13 switching states, which corresponds to the maximum number of commutations per switching period. The resulting voltage space vector sequence shows a repetition by half the switching period, and a symmetry by one quarter this time. Application times t_a , t_b and t_c are divided along the repeating vectors in order to equalize the output, reducing ripple.

Finally, one pattern was selected for each region, forming a table which is presented in Appendix A.

III. DIGITAL IMPLEMENTATION

Although this vector modulation principle has not a straightforward implementation such as the methods based on reference-carrier comparison, a digital implementation is achievable through the use of a lookup table.

The inputs of the modulation algorithm are the previously

defined modulation depth $k = V^*/(V_{dc}\sqrt{3})$ and the space vector angle θ of the voltage reference. The first step is to localize which is the region where it is situated: while the section is directly given by the reference angle, subsection can be found by using equations

$$\text{Subsection 4: } k \sin(\theta^*) > 1/2$$

$$\text{Subsection 1: } k \cos(\theta^* - 30^\circ) < 1/2$$

$$\text{Subsection 2: } k \cos(\theta^* + 30^\circ) > 1/2$$

$$\text{Subsection 3: None of the previous}$$

(2)

where $\theta^* = \theta \pmod{60^\circ}$, just as in Table I.

Once the subsection is known, the equations from Table I are used to define t_a , t_b and t_c . Now, in order to apply the switching pattern correctly, a triangular counter and six compare variables are used. Their comparison defines which one of the switching states from the lookup table must be used. Fig. 5 illustrate this principle, making use of the previous example of switching pattern for the region A2.

If we consider that the counter goes from zero to $T_s/2$ and back to zero, then, in this example

$$\text{cmp}_1 = t_a/8 \quad \text{cmp}_2 = \text{cmp}_1 + t_b/4$$

$$\text{cmp}_3 = \text{cmp}_2 + t_c/4$$

$$\text{cmp}_4 = \text{cmp}_3 + t_a/4 \quad \text{cmp}_5 = \text{cmp}_4 + t_c/4 \quad \text{cmp}_6 = \text{cmp}_5 + t_b/4$$

(3)

Finally, with all switching states, for all regions, saved in a lookup table, an initial address is determined by the section and subsection information. The crossings between the counter and the different compare variables define which switching state must be assessed from that initial address in order to apply the command pulses at the output of the system.

Now, an important feature of the patterns selection can help improve the harmonic content at the output: the type of voltage symmetry that exists in the switching patterns allow to use a discretization time of $T_s/4$ to update the compare variables. As the pattern voltages repeat twice in one switching period and are pair functions, this does not result in additional commutations.

Fig. 5. Counter-compare scheme to determine instantaneous switching state application.

Fig. 6. Winding steady state voltage and current.

IV. SIMULATION RESULTS

The vector modulation technique was implemented in simulation using Plexim's PLECS software in order to verify its functionality. A power structure such as that from Fig. 1, but with an RL load, was simulated. Simulation parameters are presented in Appendix B.

Fig. 6 presents the voltage and current directly on one of the windings while the modulation index is set to its rated value. It can be seen that the voltage presents a total of 9 distinct levels, because of the resulting zero sequence, and its maximum value is $4/3V_{dc}$.

The current has a low ripple with higher frequency than that of the switching, as a result of the symmetry of the commutation patterns. The harmonic spectrum is presented in Fig. 7. Aside from the traditional low frequency harmonics,

Fig. 7. Winding current harmonic spectrum.

Fig. 8. Gate pulses for three switching periods and the respective reference region.

the ripple appears in fact around four times the commutation frequency, which is a very attractive feature for a modulation technique especially for systems with high power, high voltage devices.

Another important feature of the switching patterns selection is the number of commutations during the transition between regions. Fig. 8 shows all the gate pulses during three switching periods and the location of the reference, in other words, the region where it is located. The two vertical lines, I and II, delimit the commutation periods.

We can observe that, with the processing period of $T_s/4$, region transition can occur inside a switching period and more than one time.

At the first and third periods, there is a transition from A4 to B2 and C2 to C3, respectively. Those transitions happen in different instants, half and three quarter the period, and does not introduce additional commutations, with the proposed switching patterns.

However, from subsections 3 to 4, as it is the case of the second period shown (B3 to B4), the change of pattern introduces one additional commutation of the switch S_1 , which is highlighted. This is the minimum number of such additional switchings per section, so what the proposed scheme does to minimize its relevance is to equilibrate them among the switches.

V. CONCLUSION

In this paper, a vector modulation strategy for a three-level open-end winding drive system using two-level converters was presented.

The modulation technique consists of using the nearest voltage space vectors produced by the system to form a linear combination that corresponds to the reference. A methodology to obtain the switching patterns for this system is presented which leads to commutation sequences with a permanent switching frequency for all switches, a current ripple with double this frequency and an equilibrated number of commutations per fundamental period.

Simulation results have shown the achievement of these objectives which are specially beneficial to systems with high power, high voltage semiconductor devices where commutation losses are a key issue.

APPENDIX A SWITCHING PATTERNS

	Region	Switching Pattern
A1		
A2		00→01→03→07→39→55→63→55→39→07→03→01→00 01→33→49→48→49→51→55→51→49→57→49→33→01 01→33→32→48→50→51→55→51→59→57→41→33→01 03→35→33→32→33→35→39→35→51→59→51→35→03
A3		
A4		
B1		00→32→40→56→58→59→63→59→58→56→40→32→00
B2		
B3		03→35→34→32→34→35→39→35→43→59→43→35→03 03→02→34→32→34→38→39→47→43→59→43→11→03 02→34→42→40→42→43→47→43→42→58→42→34→02 00→02→06→07→15→47→63→47→15→07→06→02→00
B4		
C1		
C2		02→10→42→40→42→46→47→46→42→58→42→10→02
C3		02→10→08→40→44→46→47→46→62→58→26→10→02
C4		
D1		06→14→10→08→10→14→15→14→46→62→46→14→06 00→08→24→56→60→62→63→62→60→56→24→08→00 06→14→12→08→12→14→15→14→30→62→30→14→06 06→04→12→08→12→13→15→31→30→62→30→22→06
D2		
D3		
D4		04→12→28→24→28→30→31→30→28→60→28→12→04
E1		00→04→05→07→23→31→63→31→23→07→05→04→00
E2		04→20→28→24→28→29→31→29→28→60→28→20→04
E3		04→20→16→24→25→29→31→29→61→60→52→20→04
E4		05→21→20→16→20→21→23→21→29→61→29→21→05
F1		00→16→48→56→57→61→63→61→57→56→48→16→00
F2		05→21→17→16→17→21→23→21→53→61→53→21→05
F3		05→01→17→16→17→19→23→55→53→61→53→37→05
F4		01→17→49→48→49→53→55→53→49→57→49→17→01

APPENDIX B SIMULATION PARAMETERS

Parameter	Value
DC-link voltage	1800V
Load voltage	2300V
Load frequency	60Hz
Load power	2MVA
Load power factor	0.95
Switching frequency	540Hz

ACKNOWLEDGMENT

The authors would like to thank the Brazilian agencies CNPq and CAPES, the French agency COFECUB and LAPLACE laboratory, for their support to this research.

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