Non-destructive techniques for evaluating the reliability of high frequency active devices

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Non-Destructive Techniques For Evaluating The Reliability Of High Frequency Active Devices

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Abstract

SiGe and GaN technologies have achieved rapid development over the last two decades. High level of RF circuit integration on Si low cost substrates open the way for large development of SiGe HBTs, while needs for high power density make GaN HEMT a key technology for solid state power modules. As both of these technologies achieve very elevated frequencies, they become strong contenders to GaAs technologies. Then reliability studies are needed to improve the process at the lower technology readiness level scale, and to stabilize the technological process till the final qualification step. To make an efficient diagnostic on the causal origin of the physical root mechanisms involved during the application of a stress, a multi-tool approach is mandatory to secure the diagnostic. In this paper, case studies on SiGe HBT and GaN HEMT stressed devices are proposed through the cross-analysis of low frequency noise spectral densities, of electrical transient measurements, and of TCAD simulations.

1. Introduction

Over the last five decades, the modern era of telecommunications has developed considerably, beyond military and space applications, and with consumer applications (mobile telephony, wireless sensors networks or home automation systems). All these systems need to modulate a high frequency carrier (ranging between few MHz to more than one hundred GHz) with analog or digital data.

The spreading of the markets and related applications have been made possible due to the emergence of solid state active devices, from the development of silicon based transistors in the early 1960s to the various available solutions using GaAs, silicon(germanium) (Bi)CMOS, or also GaN technologies. First, it must be considered that technological development (both with top-down or bottom-up strategies) involves customers and foundries; this means that the final context of use of a technology can be very different according to the customer targeted markets (and subsequent performance, size, cost, environment, expected operating life, …). Therefore, strategies of development of each party must be combined as far as possible: this can become hard to meet those requirements (development of general purpose devices for foundries, requirement of specific performances and reliability tests for customers).

In section 2, development strategy of solid state devices towards higher frequency and elevated power are discussed, also considering the qualification final step. Considering the roadmap of a qualification, the first studies are focused on the development and on the improvement of demonstrator devices at low technology readiness levels (TRL 3 initial gate), then the implementation in the final product needs to pass through the critical threshold of TRL 5 main gate when reliability analysis usually starts. From a simple qualification procedure, first generic stresses are performed both on die or packaged devices. Then customers carry out specific tests according to the mission of the designed system. Anyway, considering the most stringent operating conditions, stresses involving d.c life tests, RF life tests, thermal cycling or also radiations tests are at least good indicators to evaluate the reliability of a technology.

In section 3, the outline of a procedure for the characterization and for data analysis is proposed: usually, specific characterization procedures are established, closely bind to the device under test specificities. Various experimental workbenches are available to achieve studies on virgin and stressed devices, and to improve a technology process to its qualification level. From the different sets of experimental tools, it can be distinguished destructive and non-destructive (non-invasive)

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techniques. If the first ones are able to reveal the structural defects (mechanical or chemical, in the surface or in the volume of the stacked layers), it is not possible to definitely conclude about their impact on the active device performance. On the other hand, non-invasive techniques are good markers of the effects of defects on electrical performances, but it is more speculative to determine their precise locations and physical nature.

Section 4 focuses on two case studies concerning HBT devices (SiGe) and the disruptive GaN HEMT technology. Cross-analyses between transient and harmonic electrical characterizations, as well as electrical low frequency noise (LFN) measurements are summarized. For each case study, TCAD models are used to consolidate the experimental results.

2) High Frequency applications: consequences of downscaling solid state devices

The mainstream of the developments of solid state technologies target the increase of the frequency carrier and the improvement of the maximum achievable power, according to radio-link budgets studies. If both sides of the emitter and receiver are of prime importance to make the telecommunication system efficient, the most critical part concerning the reliability of a system is the emitter module; elevated d.c and RF powers are achieved, together with thermal management at the device level. Therefore, the reliability studies bringing up to the qualification of a process are mainly oriented towards elevated current or voltage (direct or reverse) and elevated temperatures (with or without d.c or RF electrical signal Then, the main timeline that make up the development of a technological process is presented.

The demonstrators which are developed from the lower Technology Readiness Levels scale up to the validation in relevant environment at TRL 5. Then a new phase starts at product demonstration level TRL 6; it is quite unreasonable to consider an innovation process as linear, and iterations are needed to master a process both on the performances and on the reliability figures of merit. In keeping with the high speed device development objective, aggressive geometrical downsizing rules (vertical and lateral scaling of devices with optimized lengths, widths, heights) and new materials (lattice and thermal mismatches, spontaneous polarization or piezoelectricity) bring new paradigms the manufacturers have to manage with. It becomes particularly difficult when solutions to achieve good performances metrics are balanced with targeted reliability figures of merit (at least maximum junction temperature T_j and elevated mean time to failure MTTF). This cycle involves different partners from the lowest TRL scale (where academic institutes are largely associated during fundamental and technological levels studies) to the highest TRL scale concerning the industry management of the final portfolio (TRL 8 for technology qualification or initial market, and TRL 9 for final successful missions and market expansion). Fig. 1 gives a brief overview of frequency and power performances, with time to failure metrics for SiGe Heterojunction Bipolar Transistors (HBT) and GaN High Electron Mobility Transistors (HEMT); some of the best academic and commercial figures of merits are reported (transition or maximum oscillation frequency, power density, mean time to failure). The step between academic studies and end-of-line manufacturing is relative to the field of studies concerning solutions to heal and stabilize a process, and then to defining the security operating area (SOA) for customers.

Nota: as the proposed FoM are rarely available together, this table gathers some examples	**Ft/Fmax GHz (gate length for FET)**	**Output power density (@freq)**	**MTTF in hours @Temperature**
Examples from academic best results			
HBT SiGe	230/300 [1] 505/720 [2]	6,5 mW/µm² [1] @77 GHz	10^6 hours [3] (Tj=125°C or Jc=10mA/µm²))
GaN HEMT	320/580 [4] (Lg=20 nm)	22 W/mm [5] (2-4 GHz) 8 W/mm [6] (94 GHz)	Not available – studies are usually associated to foundry
Examples from some manufacturers available portfolio			
HBT SiGe	285/475 [7] 323/332 [8]	18,5 mW/µm² [8] @94GHz	3.2 10^5 hours [9] (Tj=69°C, stress 125°C)
GaN HEMT	115/155 [10] (Lg=100 nm) 115/155 [11] (Lg=250 nm)	>3.3 W/mm [10] @ 30 GHz >4,5 W/mm [11] @ 20 GHz	<10^6 hours [10] (Tj=200°C) 10^6 hours [11] (Tj=200°C) 10^7 hours [12] (Tj=225°C)

Fig. 1. Overview of frequency, power and mean time to failure (MTTF) from academic studies and manufacturer production line, for SiGe Heterojuntion Bipolar Transistors and GaN High Electron Mobility Transistors (references are listed in the final relevant section).

Reliability studies and associated technological development concerns TRL scale mainly focused between TRL 5 to TRL 7. TRL scale is used for decision making in terms of technological investments; it is strongly correlated to the expected markets. The robustness of the development model depends on the market volume (placement versus other competitors on performance / price of a technological process) and the end-users variety. This last consideration makes it hard to define the decision maker about the generic stress conditions to develop for a given technology: automotive and ground applications criteria are less stringent than those of space and military applications, still considering the expected performances together with the environment of use. Anyway, a qualification strategy requires close cooperation between manufacturers and end-users customers.

As previously mentioned, the most critical aspects of reliability defining the SOA for active solid state devices are more or less closely related to current-voltage and thermal operating conditions for high power segment (transmitter). However, due to its small dimension, the active element of the receiver must sustain critical doses of radiation (space applications) or elevated RF jamming signals (radar). Technologies must be hardened in a representative environment (intrinsic, extrinsic related failures). The two main active devices used for high frequency applications are Heterojunction Bipolar Transistors (HBT or double-HBT) and Field Effect Transistors (FET, with various MESFET, HEMT, pHEMT or mHEMT declinations). This paper reports on intrinsic failures case studies (i.e. wear out of the device due to structural defects activated during stress); process variability or other low mastering technological events are not under the scope of this review. Two sets of reliability stresses can be distinguished for a qualification process:

-the first package of stresses concerns representative usual conditions under which the devices are supposed to be operated. Direct current life tests (HTRB, HTOL, I_{DQ}-I_{GQ}) can be operated at different constant biasing conditions, or by step variation (current or voltage). RF life tests (CW or pulsed with single or multi-tone signals) are used to assess the aptitude of the devices to sustain critical RF levels for high performance or rugged applications.

-the second group concerns specific extreme

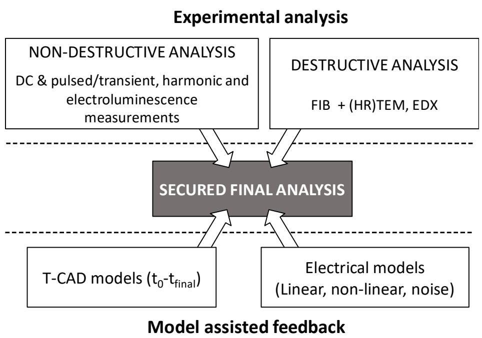


Fig. 2. Cross interpretation of non-destructive and destructive studies with electrical models for secured stress analysis. Characterizations are performed on virgin (or initial state) and stressed (or final state) devices, with possible intermediate measurements.

environment: cryogenic temperatures are used for very stable oscillators in space applications, whereas very high temperature can be largely out of the commercial applications standards (with usual stresses at 125°C instead of 85°C respectively for military and commercial specifications). Also radiation in space is much more critical than at ground level, and must be carefully considered. Even if those space and military applications represent so-called "niche" applications (i.e. usually concerning small market volumes), their impact is strongly strategic; it concerns defense, weather forecast (and resultant economy), and other commercial satellite services (open, commercial and public regulated services, safety of life, search and rescue).

3) Collective use of experimental setups and models for the assessment of active devices reliability

Fig. 2 exposes the cooperation between experimental analysis modelling techniques developed to diagnose on failure root mechanisms and to optimize the technological process. The proposed methodology used to identify the defects

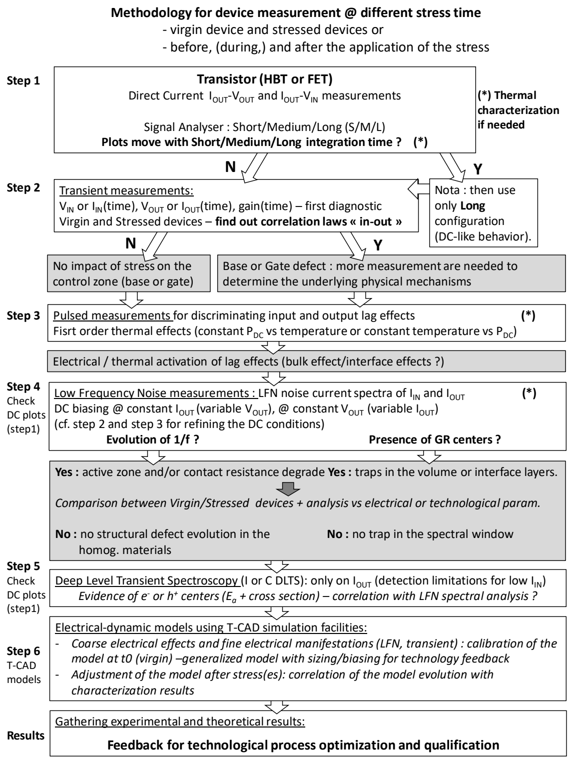


Fig. 3. Methodology to reveal defects in a device, based on transient, harmonic electrical and noise measurements. TCAD models strengthens the experimental analysis outputs. Comparison between initial/final measurements allows to locate and to determine the nature of the defects.

and their activation mode in the transistors is slightly simplified in Fig. 3 to match both for FET and HBT devices. In this presentation, the case studies are focused on the analysis of non destructive techniques and T- CAD models; non-destructive experimental setups allow the user to keep the devices (virgin or stressed) operational, and to apply a large variety of experimental procedures. Two distinct experimental setups can be differentiated:

-electrical measurements provide the user with functional data, and resulting parameters extracted from models. In addition to d.c characterizations, transient and frequency domain measurements are achieved (small or large signal, CW or pulsed, with or without temperature as a varying parameter).

-Low Frequency Noise spectra and Random Telegraph Noise reveals microscopic defects in the zones where the various currents flow (output current from the controlled source, input or leakage currents). Step 4 in Fig. 3 represent a crucial part of the survey, as the involved mechanisms that are detected in the noise spectra at the input and output of the device are very sensitive to the technological process. The noise signature is a fine marker of latent defects, some of them remain stable with time and stress, some are activated by the stress conditions.

The workflow and the subsequent interpretations can reveal the location, the nature and the operating mode of these defects by tuning adequate d.c biasing conditions, by varying the geometry or by performing measurements at different temperatures. The next section proposes some chosen case studies on SiGe HBT and on GaN HEMT devices, for which electrical and LFN measurements have been used in a complementary way to reveal the defects, and to propose potential technological solutions towards a stabilized technological process.

For very complex case studies, additional experimental setups and electrical models are developed to reduce (or remove) any speculative assumption. In Fig. 3, TCAD simulations are also used at the final step of the procedure. Model is calibrated on virgin device measurements, and is modified to account for the experienced degradation. In the next section, TCAD simulations are used as a complementary tool for providing clues on how devices can be degraded under stress application.

4) Reliability case studies on SiGe HBT and GaN HEMT

With the still evolving landscape of technologies, the emergence of SiGe BiCMOS integrated solutions in the early 1990s has shaped new architectures and new possibilities thanks to a high integration level and to low cost. However, GaAs HBTs and FETs were still positioned as frontline technologies for high performance and high frequency fields of applications. In parallel with the development of SiGe bipolar transistors, a second step was achieved in the 2000s with the advent of wide bandgap GaN technologies: thus critical areas concerning high frequency and high power applications (as well as robust low noise modules) have led to a redistribution of systems architectures. GaAs are still present in the roadmaps and portfolios of electronic devices manufacturers. But, as the benefits of GaAs technologies are more and more reduced to niche applications, most manufacturers change their strategy by centering their activities on SiGe or GaN solutions. The first case study gathers some reliability analysis on precursor devices of SiGe HBT (BiCMOS technologies), while the second one concerns some achievements on reliability of GaN HEMT devices.

4.1. Electrical and LFN measurements and models for reliability case studies on SiGe HBTs

Low frequency noise and random telegraph signal are sensitive metrics for determining defects in the active devices [13, 14, 15], as it can reveal defects prior to any stress application, while most electrical characterization setups are not able to track those defects (except for DLTS measurement techniques). For long-term operation, the main reliability issue in SiGe HBTs is the cumulative degradation of the base current that occurs under combined high emitter current and high collector voltage stress. An illustration of the different zones of SOA, soft degradation and catastrophic failure, is

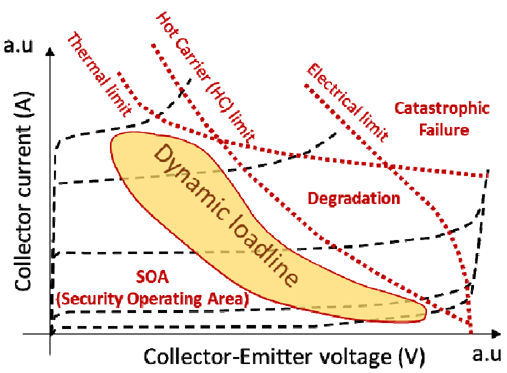


Fig. 4. Illustration of output characteristics of SiGe HBT devices with thermal, hot carrier and electrical limits defining the area of safe operating mode, degradation and catastrophic failure. Example of a dynamic load-line is represented, close to the SOA limit for power applications. Current and voltage are in arbitrary unit.

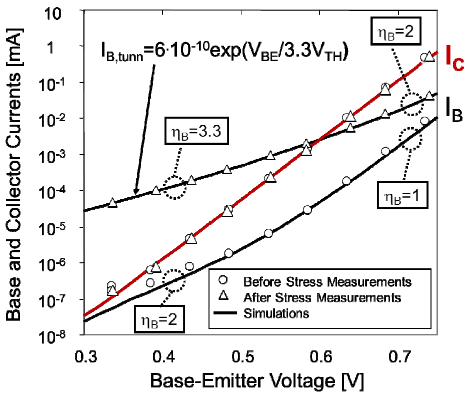
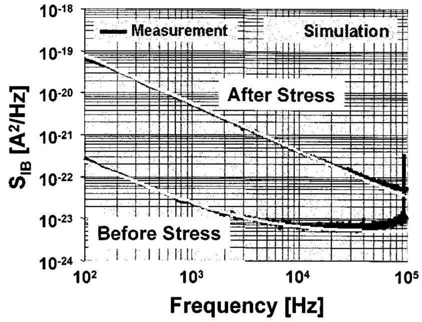


Fig. 5. Measured and simulated Gummel plots before and after applying the stress. The ideality factors are all experimental.

given with the output characteristics of a device in Fig. 4. The stress plan for long term reliability studies can be developed from these d.c biasing and RF plots (dynamic loadline), whereas extreme or harsh conditions are defined considering very low or very high temperatures (or wide temperature range), or also radiation-rich environment (or their combination). The reliability of SiGe HBT devices is a complex issue as various physical limiting mechanisms are involved. These effects such as hot-carrier (HC), self-heating, electromigration, impact ionization or radiated ionization interact in a complex way.

In the present study, hot carrier (HC) and ionizing radiations (IR) effects on the RF S-parameters are illustrated. HC stress was developed by the application of reverse base-emitter voltage stresses [16]; these conditions are relevant for reliability concerns as the base of the HBT devices is highly doped. The d.c effects of the HC stress have been investigated first by the observation of the forward Gummel plots (Fig. 5). The base current and the ideality factor both increase with the stress, whereas the collector current remains unchanged, as a typical signature of HC stress [17]. LFN spectra on S_{IB} (relative to base current fluctuations) and S_{IC} (relative to collector current fluctuation) have been measured and modelled, both exhibiting an increase of the 1/f component (two orders of magnitude for S_{IB}), as depicted in Fig. 6. The noise floor also features a slight decrease after the stress, that is not discussed in this paper. By a dedicated model of the different noise sources located in the base and in the emitter (bulk and space charge region), it has been evidenced how these LFN contributors evolve with stress. Defects associated to surface recombination (at the emitter perimeter) and trap-assisted tunneling recombination mechanism have been created by the hot carriers during the stress. All these conclusions



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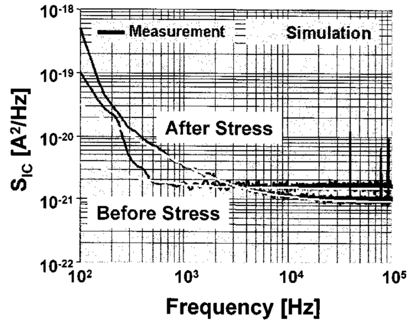


b)

Fig. 6. Measured and simulated LFN spectra of S_{IB} (a) and S_{IC} (b) before and after the application of the stress.

are supported by electrical d.c and LFN measurements, as well as electrical and noise modellings. More detailed analysis can be found in [18], also with numerical simulations. TCAD model has been developed and instructed to simulate the d.c and dynamic RF signatures before and after the application of the stress. Fig. 7 and Fig. 8 show the measured and simulated change in S_{21} gain parameter (from [S] matrix) at constant base current. Impact of stress on the transition frequency f_T is given in the inset of Fig. 7. Slight differences between measurement and simulation are due to the access pads contribution on the module (losses) and phase (electrical lengths of lines), not removed from the measured S-parameters. The simulation well reproduce the experimentally observed behavior. It must be mentioned that at constant collector current, no change is noticed on S_{21} (simulation and measurement). Proton irradiation have been experienced on these devices, with no change in the S-parameters at constant I_C. Same conclusions have been obtained on different new generations SiGe technologies, and improvements on the base process (stabilization of the doping species) and on the passivation technique have led to mature technologies, thanks to the fine determination of events occurring within the volumes or interfaces of the active zones. Similar studies have been developed on recent technologies, featuring current gain enhancement in SiGe HBTs under inverse and

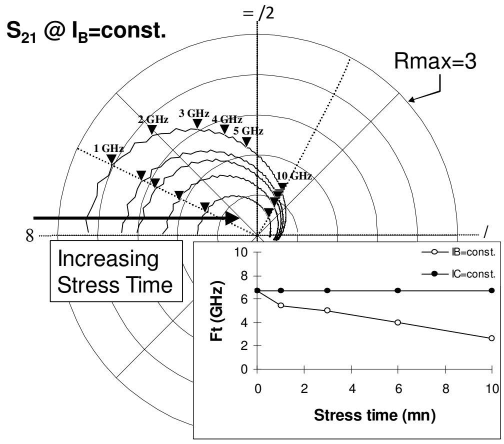


Fig. 7. Changes in the extrinsic scattering parameter S_{21} measured from 40 MHz to 30 GHz at constant base current I_B during the stress. The inset represents the variations of the measured extrinsic transition frequency f_t during the stress, measured at constant I_B and constant I_C.

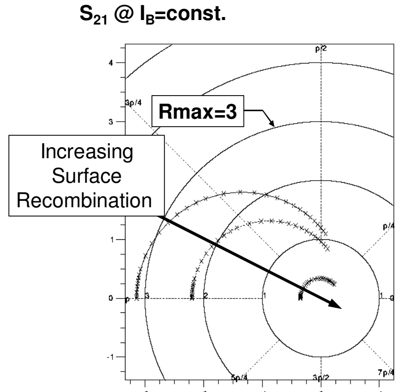


Fig. 8. Changes in the intrinsic transmission scattering parameter S_{21} simulated from 40 MHz to 40 GHz at constant I_B (V_{CE}=1 V) before and after stress.

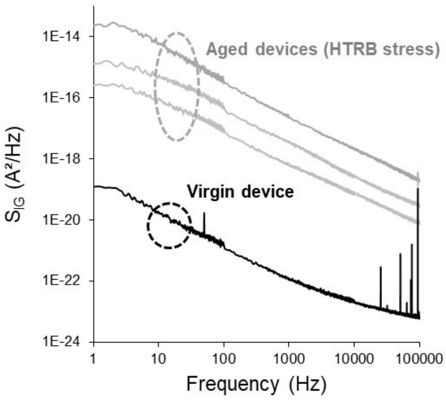
forward operation modes, and have been analyzed with TCAD models [19].

Other studies on SiGe and III-V HBT technologies have taken full advantage of electrical and LFN measurements, with dedicated models. Hydrogen related defects in GaInP/GaAs HBT have been evidenced, with complex kinetic affecting surface recombination and carbon passivation, which translates into enhancement and decrease periods on gain current β as reported in [20]. Advanced TCAD models have been developed to optimize the performance and the reliability for very high frequency application purpose [21, 22]. The different trade-offs induced by the device size reduction in Si/SiGe and InP/GaAsSb HBTs (extrinsic to intrinsic base link due to lateral and vertical scaling), with isolation strategies (trench isolation) and the related increase of the thermal resistance R_{TH} are considered together. Reliability predictive models are used for the simulation of HC damage in SiGe HBT [23].

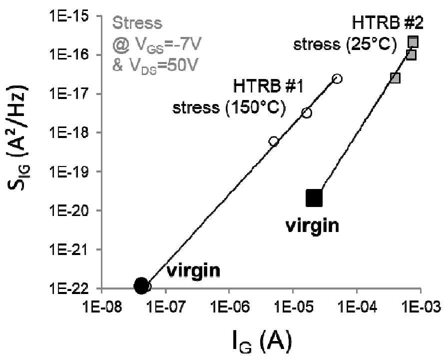
4.2. Electrical and LFN measurements and models for reliability case studies on GaN HEMTs.

Wide bandgap semiconductors feature superior material properties enabling power device operation at higher temperatures, voltages, and switching speeds than current Si or GaAs technologies. While GaAs devices total achievable power had plateaued in the 2010th after more than three decades of developments, GaN HEMT overcomes low breakdown voltages and low thermal conductivity, and makes much higher operating voltages as well as higher current densities. These combine to enable six to ten times higher output power density with GaN than with GaAs, even at high frequencies thanks to the high mobility of electrons in the GaN quantum well. Thermal effects are one of the major issue for HF devices, as the output power is proportional to the barrier thickness, which is inversely proportional to the device cut off frequency.

However, SOA limits are not at their higher potential due to still limiting reliability issues to solve: in these complex devices, it is necessary to discriminate between electrical, thermal and mechanical effects that can combine in direct and inverse relationship. A method based on variable stimuli such as temperature, time or frequency makes it possible to distinguish between these events. Fig. 3 lays the outline for the measurement and modeling techniques, mixed with destructive techniques as proposed in Fig. 2, to define a coarse and fine analysis of defects related to the application of a stress. Among drastic intrinsic limitations for RF applications, lag effects on drain current can raise from various origins below the gated zone and in the ungated drain-gate or gate-source regions, with static or dynamic behaviors that can interfere with the carrier frequency according to the load line area. Even for power devices field effect transistors, LFN measurements are of great interest to scan the spectral signatures of the defects. By defining constant temperature, d.c quiescent drain (leakage) current, or gate-drain (gate-source) voltage measurement strategies, it is possible to perform cross-experiments according to various stimuli. Frequency (LFN spectra or HF frequency dispersion [24]), time (transient d.c or pulsed lag measurements [25, 26]) or temperature (DLTS) measurements have been carried out on different GaN technological processes during development steps (low TRL scale 3 to 5) or qualification steps (higher TRL scale 5 to 8). Two main mechanisms can be sorted out. The



a) S_{IG} LFN spectra vs frequency



b) S_{IG} (@1kHz) versus I_G for two HTRB stresses

Fig. 9. a) Gate current LFN spectra for virgin (black) and HTRB stressed devices (greys) and b) linear plot from S_{IG} vs I_G for virgin and stressed devices (two HTRB stresses @ 150°C and 25°C).

first one concerns defects that affect the carriers flowing in the 2DEG channel, and not related to the gate command. The second one is attributed to the gated zone, and represent the most challenging electrical issue for the control of the electron density in the 2DEG.

A listing of common phenomena is identified in [27]. It has been demonstrated that, even if (de)trapping centers are identified in the channel of the device, their evolution after the application of a stress is not significant (drain current spectral density S_{ID}). However, if these centers are located in the gate-source or gate-drain interfaces, or in the GaN bulk layer, they can strongly impact the stability of the RF signal (lag and other transient effects).

Fig. 9 represents the gate current LF spectra S_{IG} on virgin devices and HTRB stressed devices. From Fig. 9 a. S_{IG} features a strong degradation after ageing (increase by more than 3 decades). This evolution is clearly correlated to an increase of the gate leakage current during stress as reported in Fig. 9 b. The induced degradation during HTRB stress impacts the 1/f noise source (electron carrier

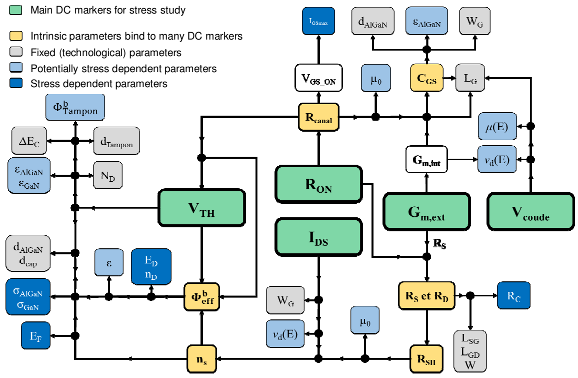


Fig. 10. Tree structure for the analysis of TCAD model before/after stress. Application to GaN HEMT technologies. Electrical parameters (green boxes) are bind to physical parameters; fixed technological parameters (grey) or stress dependent parameters (blue & cyan) are used to fit the main d.c electrical markers (orange and green) defining the output & transfer characteristics, leakage current [31]).

fluctuation in the leakage conduction path), and thus the leakage current I_G can be used as a dependable marker of reliability for device selection. A unified model has been developed to account for the gate Schottky barrier height inhomogeneity [28], for the thermal evolution of the I_G-V_{GS} plots and for the trap effects on the transient characteristics I_{GS}(time) and I_{DS}(time) [29]. In addition to these electrical and noise characterizations, TCAD models have been developed to successfully account for the physical origin of the evolutions on drain current and gate leakage current [30, 31]. A synoptic of the tree structure used to discriminate between the different physical parameters that are tuned to account for the degradation process is given in Fig. 10. This structure helps to find the set of parameters evolving with stress. In addition to usual IDQ or HTRB stresses, RF stresses are also of great interest to track

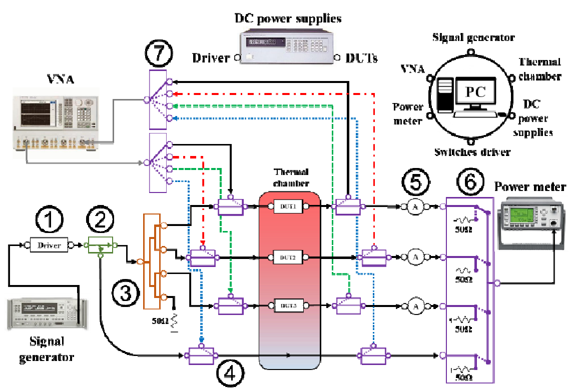
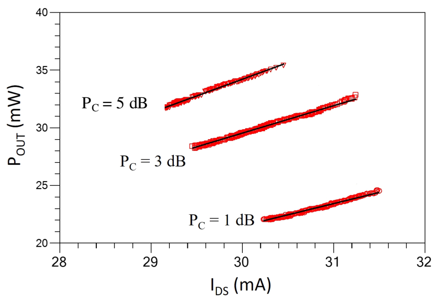


Fig. 11. Schematic of RF/thermal stress test setup: ① power amplifier, ② coupler, ③ four-way power divider, ④ SPDT, ⑤ attenuators, ⑥ SP4T 50Ω RF load terminations ⑦ SP4T.

the stability both on static and dynamic electrical parameters. From a dedicated experimental setup depicted in Fig. 11, scattering S-parameters can be measured during the stress campaign (removing the RF signal and switching on vector network analyzer for each of the 4 paths under stress). Fig. 12.a. illustrates the linear dependance between the output power and the d.c drain current during the application of the RF signal at 1 dB, 3 dB and 5 dB compression points. Fig. 12.b. reports on the linear coefficient evolution for each RF stress. From the small signal linear model extracted at different stress intervals, it is possible to state that the electrical parameters possibly involved in the change of I_{DS} are stable during the different stress campaigns (gate-source capacitance C_{GS}, intrinsic resistance R_i, source contact resistance R_s or transconductance gain g_m) [30]. Hence, the degradation of the coefficient *a* versus the RF compression level is attributed to the activation of charges beneath the gated zone; these stress induced charges generate an intrinsic generator (in series with the d.c biasing external source), that in turn modifies the gate-source voltage controlling g_m, and thus the electron density in the channel. Similarly, the evolutions on access resistances as proposed in [32] could be interpreted as the consequence of variations in the intrinsic local biasing of the device (charges accumulation) [31],



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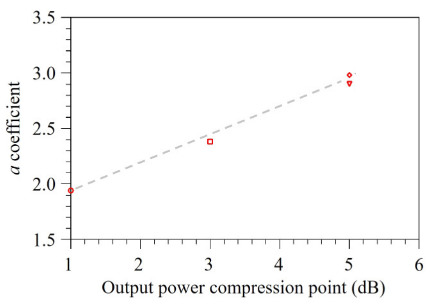

b)

Fig. 12. a) Correlation between output power @ 10 GHz and d.c drain current, featuring a correlation law $P_{OUT}= a.I_{DS}+ b$: power compression are performed at 1 dB, 3 dB and 5 dB consecutively for the GaN HEMTs, b) plot of the linear coefficient *a* extracted from the affine function (figure a) at 1 dB, 3 dB, 5 dB compression point.

and not as a structural change in the resistive layers constitution.

5) Conclusions and perspectives

A focus on two key technologies used for high frequency applications (SiGe HBT and GaN HEMT) is achieved, demonstrating the need to develop a multi-tool strategy for fine and secured reliability analysis; it makes use of cross-experiments in spectral and transient domains, with electrical and noise models. With the SiGe HBT evolution, BiCMOS technologies and mixed-signal applications have strongly proliferated for multiple high-performance and high frequency applications. As a consequence, reliability issues has come to the forefront. The safe-operating area of SiGe HBTs is strongly defined by Hot-Carrier mechanisms, that have been presented through a collective use of experimental and simulation tools. Althrough these effects have been widely studied over the past two decades, a T-CAD based predictive approach is required to estimate the impact of HC when scaling device performance and technology. The roadmap to high frequency and high power applications takes advantage of GaN HEMT technologies, with challenges to overcome concerning self-heating dissipation by various strategies. Besides the elevated junction temperature that affects the drift velocity and mobility [33], and that accelerate aging of the device [34], the presence of charges still need to be mastered to avoid any current collapse or even virtual gate effects, or any other mechanism inducing high frequency dispersion effects. LFN and electrical measurements are used with TCAD simulations to determine with a high degree of confidence the origin and the kinetic of the defects responsible for the degradation of the device.

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