Scalable Modeling of Thermal Impedance in InP DHBTs Targeting Terahertz Applications

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***Abstract*— In this work we report a new scalable model for the thermal impedance of III-V DHBTs that has been developed based on the physics of heat diffusion within the HBT architecture. The heat flows through both the emitter metal layers and towards the substrate are taken into account for the model development. The model constitutes of individual thermal contributions of the different regions of the intrinsic device and metal layers. On-wafer low-frequency S-parameters measurements have been performed on several device geometries to study the device dynamic self-heating. The model has been validated against the measurements showing good accuracy and scalability. Time domain pulse measurements have also been performed to correlate with the frequency domain S-parameter measurements.**

***Index Terms*— Compact model, III-V HBTs, low-frequency S-parameters, pulse measurement, self-heating, thermal impedance.**

I. Introduction

THE growing demand for high-volume, high-speed wireless communication in terahertz (THz) applications has been sustained by aggressive miniaturization of electronic devices thus allowing increasing frequency of operation [1]. At the onset of 5G and beyond communication standards, monolithic integration of electronic and photonic technologies has become a viable solution, which employs cutting-edge high speed InP-based III-V HBTs [2]. However, miniaturization is another issue in addition to the already existing thermal issues in InP-based III-V HBTs, especially for operating conditions close to the limits of their safe operating areas [2]. Due to the shift of DC operating points to higher current densities to operate at peak-f_T in miniaturized advanced and cutting-edge technologies, self-heating and thermal instabilities are the key factors limiting reliable device operation. Particularly for InGaAs/InP DHBTs, operating conditions around and beyond peak-f_T have been observed to exhibit significant self-heating [3]. Therefore, alongside scaling, there have been significant efforts to reduce electro-thermal effect by reducing the thermal impedance (Z_{TH}) of the transistors [4]. Due to significant impact of self-heating on the transistor operating conditions, the temperature rise within the device needs to be model accurately using a more complex electro-thermal network than the already implement single pole network in HiCuM compact model [5]. Hence, there is a growing need of an accurate and scalable thermal impedance model for InP DHBTs.

The heat flow through the transistor can be divided into two contributions: the upward flow through the emitter metal layers and the downward flow through the collector towards the substrate. Existing models for SiGe HBTs take into account the temperature-dependent thermal conductivity with and without trench isolations [6]. Such isolations block lateral heat flow, thus increasing the device temperature. In [7], an average thermal conductivity of silicon has been used to determine the junction temperature-dependent thermal resistance while taking into account the contribution of the BEOL layers. In [8], a complete thermal impedance model is developed using the downward heat flow with a heat-source located at the base-collector junction. This model allows extraction of a physical thermal network with multiple thermal time constants, specific to different regions of the transistor architecture, applicable for both frequency and time domain analyses. Despite the model accuracy, the large number of cells (9 cells) increases the simulation time. In InP HBTs, however, the device architecture is fundamentally different due to their mesa structure and absence of trench isolations, thus requiring a new formulation for the Z_{TH}. There have been efforts to model thermal behavior in III-V HBTs through extensive characterization and VBIC [9], R-C network based small signal [10] or 3D finite element simulations [11]. In this paper, we propose a comprehensive and computationally efficient as well as geometry scalable HiCuM-integrated compact model implementation of electro-thermal network for InGaAs/InP HBTs derived from physical relations which can be used in time and frequency domain analyses with three cells, improving model computation time. The implemented model replaces the single-pole thermal network in the intrinsic HiCuM model [5] by a three-pole thermal network for more accurate computation. The overall scalable modeling strategy is applicable regardless of the technology type (HBT or FETs), however, the model equations need to be adapted to the specific device architecture under test.

The scalable thermal impedance model in this work is developed based on the approach presented in [6] taking into consideration both emitter metal layer and intrinsic device contributions for a InGaAs/InP DHBT technology from the III-V lab. The device structure and process are similar to the ones described in [12] except for the emitter metallization which is composed of TiPdAu. These InP DHBTs feature a balanced f_T/f_{MAX} of 400/400 GHz at J_C ~7mA/µm² and V_{CE}=1.6V, a maximum current gain of ~40 and a breakdown voltage above 4.5V at J_C=50µA/µm². The rest of this paper is structured as follows: Section II presents the low-frequency S-parameter measurement setup and discusses the results of

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dynamic self-heating and thermal impedance extraction. The model formulation is presented in section III followed by model validation in section IV. Model validation using pulse measurements is presented in section V followed by the conclusion.

II. Low-Frequency S- Parameter Measurement

The LF S-parameter measurement setup constitutes of a semiconductor parameter analyzer, HP 4155, for DC biasing and a vector network analyzer, Agilent E5061B (5Hz-3GHz), as shown in Fig. 1. In order to couple RF and DC bias, bias tees (bandwidth of 30 kHz to 3 GHz) were used. The dynamic self-heating is observed in the 30 kHz-300 MHz range where thermal impedance is extracted. A standard SOLT calibration was used with an RF input power of -30 dBm, followed by open-short de-embedding. DC bias points were chosen with higher V_{BE}, where self-heating effects are dominantly visible.

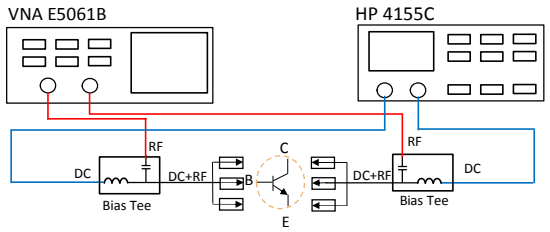

Figure 1: Low-frequency S-parameters measurement setup

In order to study dynamic self-heating, Y-parameters are obtained from LF S-parameters [13], using the following,

$$Y_{11}=\left.\frac{I_B}{V_{BE}}\right|_{V_{CE}=0},\ Y_{21}=\left.\frac{I_C}{V_{BE}}\right|_{V_{CE}=0},\ Y_{12}=\left.\frac{I_B}{V_{CE}}\right|_{V_{BE}=0},\ Y_{22}=\left.\frac{I_C}{V_{CE}}\right|_{V_{BE}=0} \quad (1)$$

Here, Y_{11} and Y_{21} are less sensitive to self-heating effects, while the self-heating effects are more visible for Y_{12} and Y_{22}. Hence, we mainly focus on these two parameters for self-heating parameter extraction. The extracted Y parameters are then used to calculate the normalized thermal impedance using the following [14, 15],

$$Z_{TH,norm}(\omega)=\left(\frac{Y_{22}(\omega)-Y_{22}^{AC}}{Y_{22}^{DC}-Y_{22}^{AC}}\right)\left(\frac{I_C+V_{BE}Y_{12}^{DC}+V_{CE}Y_{22}^{DC}}{I_C+V_{BE}Y_{12}(\omega)+V_{CE}Y_{22}(\omega)}\right) \quad (2)$$

Where Y_{22}^{AC} corresponds to Y_{22} without dynamic self-heating, Y_{12}^{DC} and Y_{22}^{DC} are the Y parameters in DC condition (i.e. $\omega\rightarrow 0$). These parameter can be extracted following the method demonstrated in [15].

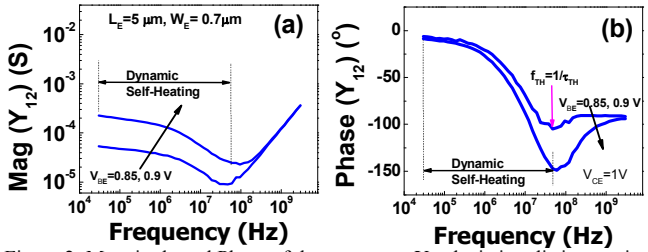

Figure 2: Magnitude and Phase of the parameter Y_{12} depicting distinct regions of self-heating.

Figure 2 shows an example depicting the magnitude and phase of the Y-parameter, Y_{12}, for one chosen device geometry (0.7×5 µm^2). Two distinct zones are observed in the results, separated by a threshold thermal frequency (f_{TH}). This frequency denotes a phase shift leading to the minimum amplitude of the Y-parameter. The first region (frequencies higher than f_{TH}) reflects only static self-heating and does not evolve with frequency. Hence, the observed behavior is purely electrical [15]. In the other region, at frequencies below f_{TH}, dynamic self-heating is dominant [15] and electro-thermal network can be used to extract the thermal impedance parameters. The analysis in the next sections will show that we require three poles to fit the dynamic self-heating region. Hence the heat dissipation region is divided into three major subsections for which we have extracted three thermal resistances and capacitances.

III. Analytical Model Formulation

As presented in [8], the downward heat flow can be modeled by the superposition of a number of subsections, leading to a distributed electro-thermal network. Each subsection is represented by one thermal resistance $R_{TH,i}$ and one thermal capacitance $C_{TH,i}$ as follows:

$$R_{TH,i}=\int_{h_{i-1}}^{h_i}\frac{dz}{\kappa A_i(z)},\ C_{TH,i}=\int_0^{h_i}\frac{\kappa}{\alpha}A_i(z)dz \quad (3)$$

where i is the number of the subsection number, A(z) is the cross-sectional area vertically located at a distance z from the heat-source, h_i is the subsection thickness, κ is the temperature dependent thermal conductivity and α is the heat diffusion coefficient in InP. The total thermal resistance of the intrinsic device can be calculated by the sum of the individual thermal resistances, R_{THi}, of each subsection, as follows:

$$R_{THF}=\sum_{i=1}^{N}R_{TH,i} \quad (4)$$

The total thermal resistance of the DHBT can be written as

$$\frac{1}{R_{TH}}=\frac{1}{R_{THF}}+\frac{1}{R_{THM}} \quad (5)$$

where R_{THF} refers to the downward contribution of thermal resistance, R_{THM} refers to the thermal resistance due to upward heat-flow (emitter, metal layers) and R_{TH} refers to the total transistor thermal resistance.

A. *Influence of the angle of heat diffusion*

The pyramidal downward heat flow through the device can be represented by two different scenarios depending on the value of the heat diffusion angle. These two scenarios are schematically illustrated in Fig. 3. For an angle $\theta < \theta_C$ (where θ_C is the critical angle at which the heat flow changes from scenario (a) to (b), with $\theta_C = \tan^{-1}[(W_{COL}-W_E)/2D_{ox}]$), with W_{COL} and W_E being the collector and emitter lateral widths, respectively, and D_{ox} is the height of the passivation layer, the heat flow is not stopped by the isolation surrounding the collector and the diffusion is pyramidal along the depth of the transistor (Fig. 3 (a)). On the contrary, for an angle $\theta > \theta_C$, the heat flow is blocked by the mesa edge, leading to a uniform heat diffusion in one subsection (see Fig. 3 (b)). In the literature, the heat diffusion angle is always lower than 65° [8], leading to the heat-flow scenario depicted in Fig. 3 (a). In our case, the mesa-edge does not come into play for the heat diffusion through the device. For the rest of the paper, we have thus considered scenario (a). For the thermal impedance modeling, the number of subsections for the downward heat

flow is crucial in order to correctly identify the contributions from different layers of the vertical structure. An electro-thermal network with only one R-C pole will lead to an inaccurate modeling of the time domain behavior [8]. On the other hand, the use of a high number of R-C poles will increase the computational time.

Moreover, for modeling the behavior of dynamic self-heating (Fig. 2) and the thermal impedance, we required a three-pole electro-thermal network. For a physical representation of this network in the vertical transistor, we have considered three major vertical sections of the heat diffusion for the thermal impedance model, which include the collector region beneath the heat source located at the B-C junction, the sub collector and the substrate. This representation is sufficient to accurately model the frequency and the time domain behavior of the thermal impedance.

B. Thermal Contribution of the Intrinsic Transistor

To represent the thermal impedance of the intrinsic DHBT, we consider a modified Foster-like thermal network, as shown in Fig. 4 (a), consisting of three thermal resistances, $R_{THF,1}$, $R_{THF,2}$ and $R_{THF,3}$, and capacitances, $C_{THF,1}$, $C_{THF,2}$ and $C_{THF,3}$. The three sets represent the three regions of the downward heat flow, the collector, the sub-collector and the substrate. The two main model parameters that control the spreading of the heat-flow are t_{si}, which determines the depth of the heat flow where the temperature reaches T_{AMB}, and the heat flow angle θ, for which the values considered in our model simulation to be around 5-7 µm and 40°, respectively. Considering an average thermal conductivity for each section and evaluating the integrals in (3), one can write the following expressions for the thermal resistance and impedance of the InP DHBT structure following the approach presented in [6]:

$$\left.\begin{aligned} R_{THF,1} &= \frac{1}{2\tan\theta\left(L_E-W_E\right)\kappa_{avg1}}\ln\left[\frac{L_E\left(W_E+2h_1\tan\theta\right)}{W_E\left(L_E+2h_1\tan\theta\right)}\right] \\ R_{THF,2} &= \frac{1}{2\tan\theta\left(L_E-W_E\right)\kappa_{avg2}}\ln\left[\frac{\left(L_E+2h_1\tan\theta\right)\left(W_E+2(h_1+h_2)\tan\theta\right)}{\left(W_E+2h_1\tan\theta\right)\left(L_E+2(h_1+h_2)\tan\theta\right)}\right] \\ R_{THF,3} &= \frac{1}{2\tan\theta\left(L_E-W_E\right)\kappa_{avg3}}\ln\left[\frac{\left(L_E+2h_2\tan\theta\right)\left(W_E+2(h_2+h_3)\tan\theta\right)}{\left(W_E+2h_2\tan\theta\right)\left(L_E+2(h_2+h_3)\tan\theta\right)}\right] \end{aligned}\right\} \quad (6)$$

Here, h_1, h_2 and h_3 denote the depths of the three regions calculated as $h_1 = (W_{COL}-W_E)/2\tan\theta$, $h_2 = (D_{OX}+D_{sc}-h_1)$ and $h_3 = t_{si}-(h_1+h_2)$. While W_{COL}, W_E, D_{OX} and D_{sc} are device technological parameters, t_{si} and θ are model parameters. W_E and L_E are the effective emitter width and length, respectively and κ_{avg1}, κ_{avg2} and κ_{avg3} are the average thermal conductivities of the three regions calculated for InP following the approach in [16]. Following a similar approach and using (3) one can, thereby, write the expressions of the thermal capacitances of the three regions as follows,

$$\left.\begin{aligned} C_{THF,1} &= \frac{\kappa_{avg1}}{D_{th}}\left[\frac{4}{3}h_1^3\tan^2\theta+\left(L_E+W_E\right)h_1^2\tan\theta+L_EW_Eh_1\right] \\ C_{THF,2} &= \frac{\kappa_{avg2}}{D_{th}}\left[\begin{aligned}&\frac{4}{3}h_2^3\tan^2\theta+\left(L_E+W_E+4h_1\tan\theta\right)h_2^2\tan\theta \\ &+\left(L_E+2h_1\tan\theta\right)\left(W_E+2h_1\tan\theta\right)h_2\end{aligned}\right] \\ C_{THF,3} &= \frac{\kappa_{avg3}}{D_{th}}\left[\begin{aligned}&\frac{4}{3}h_3^3\tan^2\theta+\left(L_E+W_E+4h_2\tan\theta\right)h_3^2\tan\theta \\ &+\left(L_E+2h_2\tan\theta\right)\left(W_E+2h_2\tan\theta\right)h_3\end{aligned}\right] \end{aligned}\right\} \quad (7)$$

C. Thermal Contribution of the Emitter and Metal Layers

The upward heat flow through the emitter metal layers is represented only by a thermal resistance, R_{THM}, in parallel with the remaining electrical part, as shown in Fig. 4 (a). The emitter-metal layer thermal resistance is calculated in a similar manner as the intrinsic device, considering three different thermal conductivities of the emitter layers: InP, InGaAs and TiPdAu [17]. The upward heat flow is illustrated in Fig. 4(b) depicting the three thermal resistances of the three emitter metal layers, $R_{THM,1}$, $R_{THM,2}$ and $R_{THM,3}$. Following the method used for the intrinsic device, expressions of the contributions of emitter metal layer thermal resistances can be written as:

$$\left.\begin{aligned} R_{THM,1} &= \frac{t_{M1}}{L_EW_E\kappa_{avg,InP}} \\ R_{THM,2} &= \frac{1}{2\tan\theta\left(L_E-W_E\right)\kappa_{avg,InGaAs}}\ln\left[\frac{L_E\left(W_E+2t_{M2}\tan\theta\right)}{W_E\left(L_E+2t_{M2}\tan\theta\right)}\right] \\ R_{THM,3} &= \frac{1}{2\tan\theta\left(L_E-W_E\right)\kappa_{avg,TiPdAu}}\ln\left[\frac{\left(L_E+2t_{M2}\tan\theta\right)\left(W_E+2t_{M3}\tan\theta\right)}{\left(W_E+2t_{M2}\tan\theta\right)\left(L_E+2t_{M3}\tan\theta\right)}\right] \end{aligned}\right\} \quad (8)$$

Here, t_{M1}, t_{M2} and t_{M3} are the thicknesses and $\kappa_{avg,InP}$, $\kappa_{avg,InGaAs}$ and $\kappa_{avg,TiPdAu}$ are the thermal conductivities of the three emitter layers. The thickness t_{M3} signifies the height of the upward heat flow where ambient temperature is reached. The complete electro-thermal network including downward and upward contributions of heat diffusion, shown in Fig. 4, has been implemented in HiCuM compact model [5] to estimate the junction temperature rise through the device.

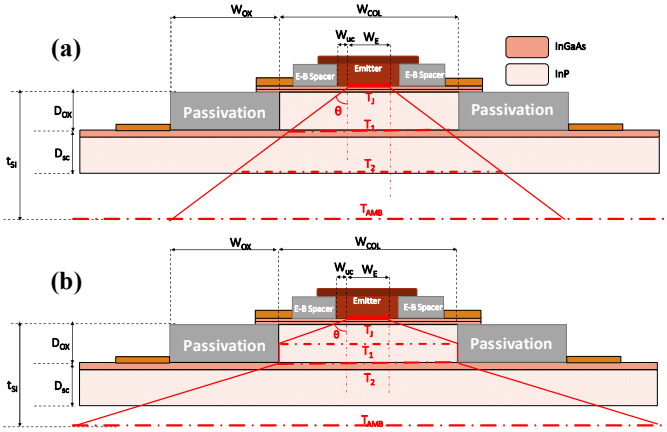

Figure 3 : Downward heat diffusion for (a) $\theta < \theta_C$ and (b) $\theta > \theta_C$

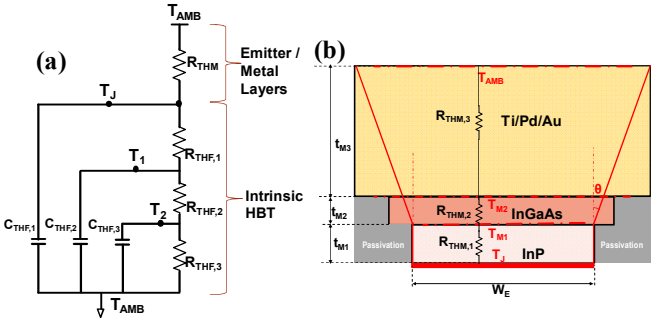

Figure 4: (a) Equivalent electro-thermal network for the vertical InP HBT architecture implemented in HiCuM compact model; (b) Thermal resistance contribution of the emitter and metal layers (upward heat-flow).

IV. Compact Model Validation

Low-frequency S-parameters have been measured on 7 device geometries [3] using the measurement setup described in

section II. Fig. 5 illustrates the results comparing the magnitudes and phases of the measured low-frequency Y-parameters (solid symbols), Y_{12} and Y_{22}, and the scalable thermal model simulation (solid lines) for different device geometries. The results are shown for a bias condition of V_{BE}=0.85V and V_{CE}=1V, chosen specifically around peak f_T of the transistors (at J_C=1.33, 1.6, 1.66, 1.67 and 1.97 mA/μm^2, respectively, for the 5 geometries shown here) that were measured, where self-heating becomes dominant. Both Y-parameters show a good agreement between measurement and the simulation results. Also, good model scalability has been observed for all the geometries. The thermal frequency (f_{TH}) for this device is around 200 MHz as observed in Fig. 5.

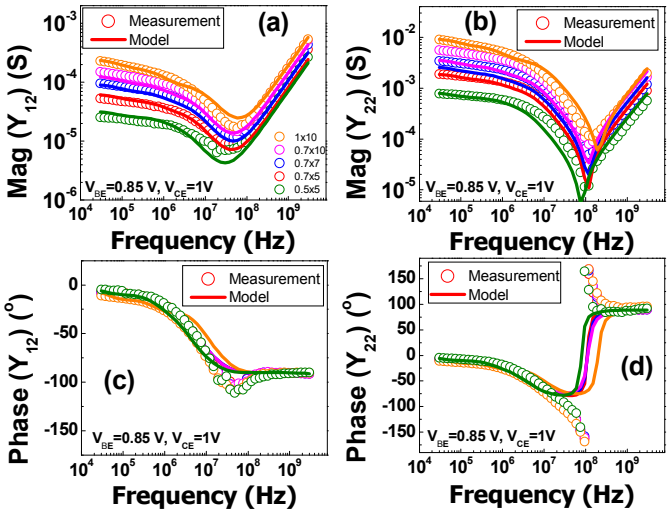

Figure 5: Comparison between measurements (symbols) and simulation (solid lines) showing the magnitudes of (a) Y_{12} and (b) Y_{22} and phases of (c) Y_{12} and (d) Y_{22} for different geometries

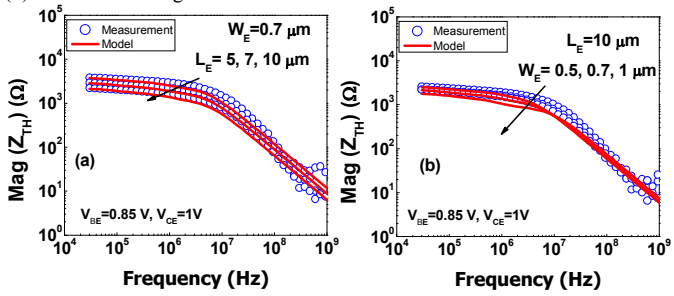

Figure 6 : Comparison between measurements (symbols) and simulation (solid lines) showing the magnitudes of Z_{TH} for different (a) L_{E0} and (b) W_{E0}.

Fig. 6 presents the magnitudes of the thermal impedance, Z_{TH}, extracted using (2), comparing the measurements (solid symbols) and the proposed model simulation (solid lines), depicting good model accuracy and scalability. Figs. 6(a) and (c) show the magnitude and phase of the Z_{TH} for emitter length scaling for a fixed emitter width (0.7 μm), while Figs. 6 (b) and (d) show the magnitude and phase of the Z_{TH} for emitter width scaling for a fixed emitter length (10 μm). In both cases, the model describes the behavior of the dynamic self-heating (below f_{TH}) quite well.

The thermal resistances and capacitances for the three regions of the intrinsic device are shown in Table I, extracted using (6) and (7), for three geometries with different emitter lengths and an emitter width of 0.7 μm. The total thermal resistance is calculated taking into account both intrinsic device and R_{THM} as shown in table II. R_{TH} is extracted from the measurement using the intersection technique [18]. The total thermal resistances from the model simulation are extracted using equations (6) and (8). The extraction results are summarized in table II for all available geometries, depicting a very good estimation of the thermal resistances using the proposed model, in comparison with the values extracted from the measurement, corroborating good model accuracy and scalability. Finally, Fig. 7 and 8 show the magnitudes and phases of the Y-parameters for higher V_{BE}, and V_{CE}, i.e. at higher collector current densities, to validate the model under pronounced self-heating conditions. These two figures depict results for the geometry 0.7×5 μm^2 (representative transistor for this technology generation) under the operating conditions V_{BE}=0.85V and V_{CE}=1, 1.2 V (at J_C=1.6, 1.72 mA/μm^2) (Fig. 7) and V_{BE}=0.85, 0.9V and V_{CE}=1V (at J_C=1.6, 4.06 mA/μm^2) (Fig. 8). These operating points are chosen around peak-f_T and beyond for the DHBT technology to where an increased collector current increases the dissipated power and thus the device self-heating. Note that the range of junction temperature studied for this geometry is between 294 and 331 K, while the entire range of junction temperature between the smallest and the largest geometries is 289-349 K.

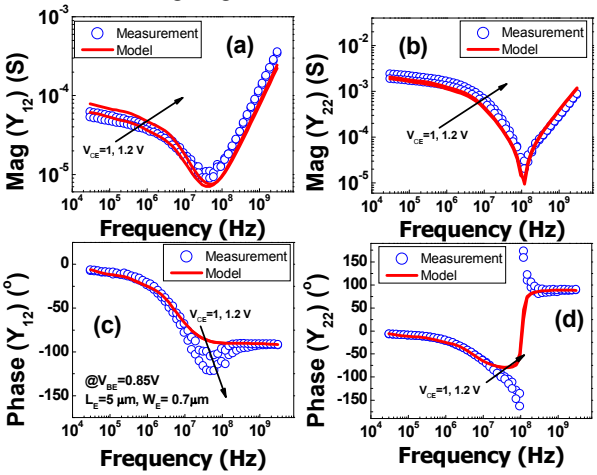

Figure 7 : Comparison between measurements (symbols) and simulation (solid lines) for magnitudes of (a) Y_{12}, (b) Y_{22}, and phases of (c) Y_{12} and (d) Y_{22} for the geometry 0.7×5μm^2 as a function of different V_{CE} at V_{BE}=0.85V.

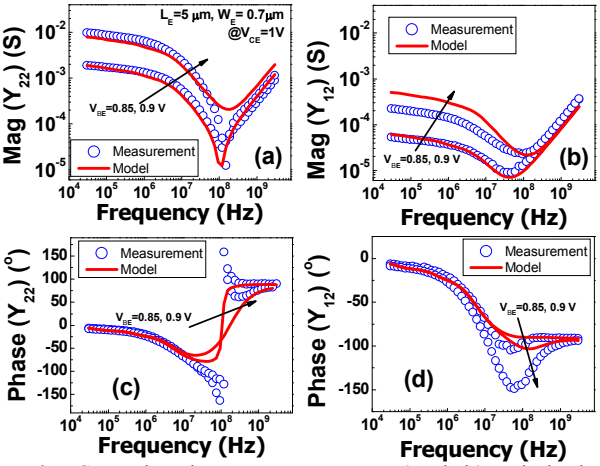

Figure 8 : Comparison between measurements (symbols) and simulation (solid lines) for (a) Y_{12} magnitude, (b) Y_{22} magnitude, (c) Y_{12} phase and (d) Y_{22} phase for the geometry 0.7×5μm^2 as a function of different V_{BE} at V_{CE}=1V.

We observe that the variation in V_{BE} causes a more pronounced increase in the magnitude of the Y- parameters (Fig. 8) compared to that with the variation in V_{CE} (Fig. 7). In both cases, the model captures the self-heating effects very well thus validating the proposed model.

TABLE I. THERMAL RESISTANCES AND CAPACITANCES OF THE INTRINSIC HBT EXTRACTED FROM THE MODEL SIMULATION

$W_E \times L_E$ [μm²]	$R_{THF,1}$ [K/W]	$R_{THF,2}$ [K/W]	$R_{THF,3}$ [K/W]	$C_{THF,1}$ [pJ/K]	$C_{THF,2}$ [pJ/K]	$C_{THF,3}$ [nJ/K]
0.7×5	2844	1490	1051	13	170	1.8
0.7×7	2109	1197	907	18	203	2.1
0.7×10	1516	926	753	24	260	2.5

TABLE II. THERMAL RESISTANCE EXTRACTION INCLUDING INTRINSIC HBT AND EMITTER METAL LAYER CONTRIBUTIONS FOR DIFFERENT GEOMETRIES

$W_E \times L_E$ [μm²]	R_{TH} Extracted [K/W]	R_{THF} Model [K/W]	R_{THM} Model [K/W]	R_{TH} Model [K/W]
0.5×5	4150	6131	17000	4505
0.7×5	3700	5384	13067	3812
0.7×7	3100	4213	9511	2920
0.5×10	3200	3615	8752	2558
0.7×10	2400	3195	6760	2170
1×10	2100	2812	5135	1817

V. VALIDATION WITH PULSE MEASUREMENT

Pulse measurements were carried out to validate the data obtained from the low-frequency S-parameter measurement. The pulse measurement setup includes a pulsed DC analyzer, Keithley 4200-SCS, including two pulse measurements units (4225-PMUs) as illustrated in Fig. 9. The system generates the pulse trains for the base and the collector and measures the pulse time response. The pulse train in CH1 is directly applied to the base of the transistor by setting the amplitude. The collector port (CH2) is biased at a constant voltage while the emitter is grounded. The PMU allows creating pulses with widths larger than 70ns for a minimum rise and fall times of 20ns.

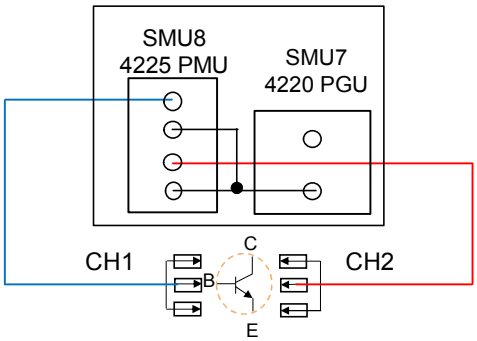

Figure 9 : Experimental setup for pulse measurements

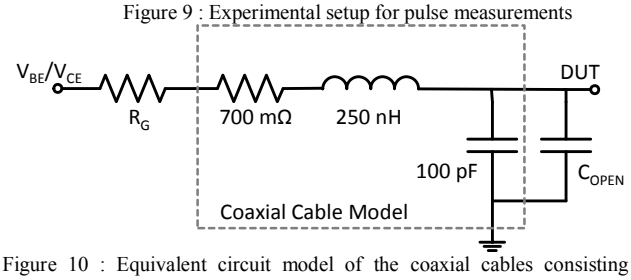

Figure 10 : Equivalent circuit model of the coaxial cables consisting of passive elements, the generator resistance R_G and device open capacitance C_{OPEN}.

During pulse measurements collector current or voltage overshot may appear while a base pulse is applied [19]. This is partly due to the passive elements associated with the coaxial cable and the connectors. It is therefore necessary to take a model of the coaxial cable and the connectors into account during the simulation of DHBTs. For the pulse measurements setup, two coaxial cables were used between the base and collector ports and the pulsed DC analyzer. Therefore, a model of the coaxial cables, as depicted in Fig. 10 (shown for a single port), has been added to the simulation test-bench**.** The internal resistance of the pulse generator is 50Ω for each of the base and collector ports. The values of the other components of the coaxial cable model depend on the length of the cables, and are thus adjusted accordingly during simulation. The capacitance, C_{OPEN}, corresponds to the device open capacitance and is quite low (typically, around a few fF).

Transient simulations were performed with HiCuM model using a fully calibrated model card for the InGaAs/InP DHBTs [3], taking in account, additionally, the proposed thermal network model. The transient simulations are performed under the bias conditions V_{BE}=0.85V and V_{CE}=1.2 V for the geometry 0.7×5 μm², with an applied pulse width of 500ns and a pulse delay of 200ns. Fig. 11 shows the comparison between the transient simulation and the pulse measurements, depicting the transient behavior of the collector current I_C. The simulation using the proposed thermal impedance model agrees very well with the waveform captured using pulse measurement, thus validating the accuracy of the model in the time domain.

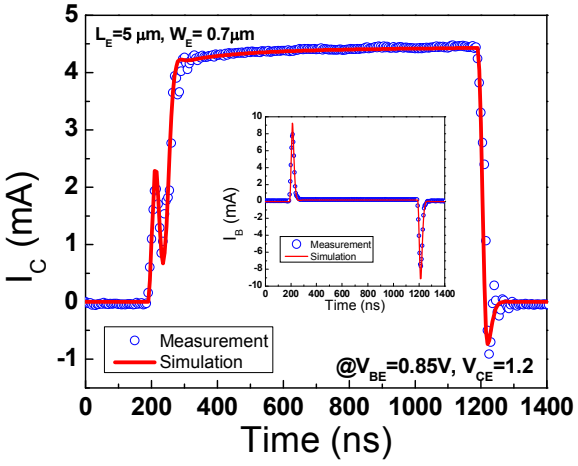

Figure 11: Comparison between measurements (symbols) and simulation (solid lines) of the collector current evolution as a function of the time for V_{BE}=0.85V and V_{CE}=1.2V.

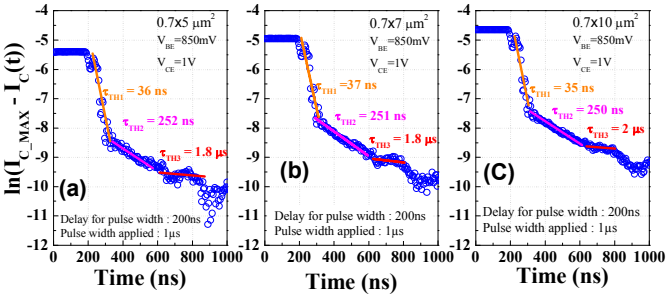

Figure 12: Extraction of thermal time constant, τ_{TH}, from pulse measurements for the geometries with W_{E0}=0.7μm and L_{E0} (a) 5, (b) 7 and (c) 10 μm.

TABLE III. COMPARISON OF THERMAL TIME CONSTANTS EXTRACTED FROM THE MODEL AND PULSE MEASUREMENT

	Thermal Model			Pulse measurement		
$W_E \times L_E$ [μm^2]	τ_{TH1} [ns]	τ_{TH2} [ns]	τ_{TH3} [μs]	τ_{TH1} [ns]	τ_{TH2} [ns]	τ_{TH3} [μs]
0.7×5	36	253	1.9	≤40	252	1.8
0.7×7	37	243	1.9	≤40	251	1.8
0.7×10	36	241	1.9	≤40	250	2

Finally, we compare the values of the thermal time constants obtained from both the pulse measurements and the model simulation. In Fig. 12, we analyze the collector current plotted as a function of the time for the three geometries depicted in table I. The quantity $\ln(I_{C\_MAX}-I_C(t))$ (where I_{C_MAX} is the stead-state value of the $I_C(t)$ waveform) is plotted as a function of time for the three geometries, which allows to segregate the thermal contributions of different regions in the intrinsic transistor. Fig. 13 plots the thermal resistance (13 (a)), the thermal capacitances (13 (b)) and the thermal time constants (13 (c)) obtained by $\tau_{THn}=R_{THn}\times C_{THn}$, for the three geometries depicted in table I. From Fig. 12 we see these distinct regions (with distinct slopes) confirming the existence of the contributions in the dynamic self-heating. From the slopes of the first two regions we obtain the thermal time constants that can be associated with the values in Fig. 13. Note that the first slope, giving τ_{TH1}, results from a combined effect of the thermal device and the experimental setup, which contributes roughly 15ns (cables + pulse generator rise time + electrical contribution of the transistor itself). The third slope, which is not so distinct, but is consistent with the value of τ_{TH3} from Fig. 13. In table III, the two sets of values of the thermal time constants are compared. This validates the accuracy of the proposed model in the time domain.

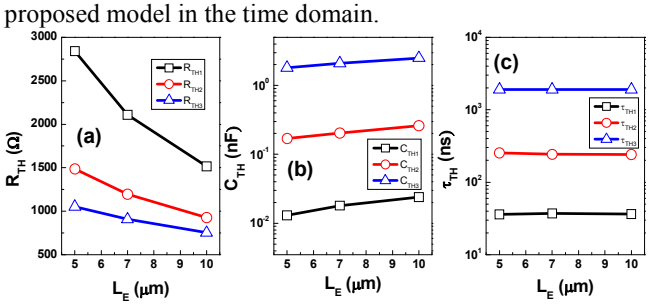

Figure 13: Extracted values of the (a) R_{TH}, (b) C_{TH} and (c) τ_{TH} of the three regions for three geometries with L_{E0}=5,7 and 10 μm and W_{E0}=0.7 μm.

VI. CONCLUSION

A new thermal impedance model for InP DHBTs has been presented in this work. The model is scalable and includes both intrinsic transistor and emitter metal layer contributions to heat diffusion. The downward heat flow has been modeled taking into account three contributions from the vertical InP DHBT architecture in order to correctly represent the dynamic self-heating. The developed analytical model formulation has been implemented in Verilog-A in order for it to be compatible with HiCuM compact model. The proposed model was validated against on-wafer low-frequency S-parameters measurements. A secondary validation was then performed through pulse measurements thus establishing a correlation between the frequency and time domains. Very good model accuracy and scalability have been demonstrated over a wide range of geometries and operating conditions in both frequency and time domain for a high-speed InGaAs/InP DHBT technology. Owing to its compatibility with existing circuit design tools, the proposed model has the potential to serve as a future building block for high-speed communication system design, especially for InP HBT technologies that are prone to pronounced self-heating under operating conditions close to the limit of their safe operating area.

REFERENCES

[1] P. Chevalier, M. Schröter, C. R. Bolognesi, V. d'Alessandro, M. Alexandrova, J. Böck, R. Flückiger, S. Fregonese, B. Heinemann, C. Jungemann, R. Lövblom, C. Maneux, O. Ostinelli, A. Pawlak, N. Rinaldi, H. Rücker, G. Wedel, and T. Zimmer, "Si/SiGe:C and InP/GaAsSb Heterojunction Bipolar Transistors for THz Applications," *Proc. IEEE*, vol. 105, no. 6, pp. 1035–1050, Jun. 2017. DOI: 10.1109/JPROC.2017.2669087

[2] C. Mukherjee, B. Ardouin, J. Y. Dupuy, V. Nodjiadjim, M. Riet, T. Zimmer, F. Marc, and C. Maneux, "Reliability-Aware Circuit Design Methodology for Beyond-5G Communication Systems," IEEE Trans. Device Mater. Rel. vol. 17, no. 3, pp. 490-506, Sept. 2017, DOI: 10.1109/TDMR.2017.2710303.

[3] C. Mukherjee, C. Raya, B. Ardouin, M. Deng, S. Frégonèse, T. Zimmer, V. Nodjiadjim, M. Riet, J.-Y. Dupuy, M. Luisier, W. Quan, A. Arabhavi, C. R. Bolognesi, and C. Maneux, "Scalable Compact Modeling of III-V DHBTs: Prospective Figures of Merit towards THz Operation", IEEE Trans. Electron Dev. vol. 65, no. 12, pp. 5357 - 5364, Sep. 2018, DOI: 10.1109/TED.2018.2876551.

[4] Y. Shiratori, T. Hoshi, M. Ida, E. Higurashi and H. Matsuzaki, "High-Speed InP/InGaAsSb DHBT on High-Thermal-Conductivity SiC Substrate", *IEEE Electron Dev. Lett.*, vol. **39**, no. 6, pp. 807-810, Jun. 2018, DOI: 10.1109/LED.2018.2829531.

[5] M. Schröter and A. Chakravorty, "Compact hierarchical modeling of bipolar transistors with HICUM", World Scientific, Singapore, ISBN 978-981-4273-21-3, 2010.

[6] A. Chakravorty, R. D'Esposito, S. Balanethiram, S. Frégonèse, and T. Zimmer, "Analytic Estimation of Thermal Resistance in HBTs," *IEEE Trans. Electron Devices*, vol. 63, no. 8, pp. 2994–2998, Aug. 2016. DOI: 10.1109/TED.2016.2572959.

[7] S. Balanethiram, A. Chakravorty, R. D'Esposito, S. Fregonese, D. Céli, and T. Zimmer, "Accurate Modeling of Thermal Resistance for On-Wafer SiGe HBTs Using Average Thermal Conductivity," *IEEE Trans. Electron Devices*, vol. 64, no. 9, pp. 3955–3960, Sep. 2017. DOI: 10.1109/TED.2017.2724939

[8] A. K. Sahoo, S. Fregonese, M. Weis, N. Malbert, and T. Zimmer, "A Scalable Electrothermal Model for Transient Self-Heating Effects in Trench-Isolated SiGe HBTs," *IEEE Trans. Electron Devices*, vol. 59, no. 10, pp. 2619–2625, Oct. 2012. DOI: 10.1109/TED.2012.2209651.

[9] O. Sevimli, A. E. Parker, A. P. Fattorini and S. J. Mahon, "Measurement and Modeling of Thermal Behavior in InGaP/GaAs HBTs," in IEEE Transactions on Electron Devices, vol. 60, no. 5, pp. 1632-1639, May 2013. DOI: 10.1109/TED.2013.2254117

[10] K. Lu and X. Zhang, "Characterization and modeling of thermal dynamic behavior of AlGaAs/GaAs HBTs," 1998 IEEE MTT-S International Microwave Symposium Digest (Cat. No.98CH36192), Baltimore, MD, USA, 1998, pp. 611-614 vol.2. DOI: 10.1109/MWSYM.1998.705067.

[11] A. Xiong, R. Sommet, A. A. L. de Souza and R. Quere, "Dual approach for HBT thermal impedance," 2008 14th International Workshop on Thermal Inveatigation of ICs and Systems, Rome, 2008, pp. 190-194. DOI: 10.1109/THERMINIC.2008.4669906.

[12] V. Nodjiadjim S. Cros-Chahrour, J.-Y. Dupuy, M. Riet, P. Berdaguer, J.-L. Gentner, B. Saturnin, and J. Godin, "InP/GaInAs DHBT with TiW emitter demonstrating f_T/fmax ~340/400GHz for 100 Gb/s circuit applications," Proc. IEEE IPRM, Santa Barbara, CA, 2012, pp. 192-195.

[13] A. K. Sahoo, S. Fregonese, M. Weiß, N. Malbert, and T. Zimmer, "Electro-thermal dynamic simulation and thermal spreading impedance modeling of Si-Ge HBTs," *Proc. IEEE BCTM*, 2011, pp. 45–48. DOI: 10.1109/BCTM.2011.6082746

[14] A. K. Sahoo, S. Fregonese, T. Zimmer and N. Malbert, "Thermal Impedance Modeling of Si–Ge HBTs From Low-Frequency Small-Signal Measurements," IEEE Electron Dev. Lett., vol. 32, no. 2, pp. 119-121, Feb. 2011. DOI: 10.1109/LED.2010.2091252.

[15] A. K. Sahoo, "Electro-thermal Characterizations, Compact Modeling and TCAD based Device Simulations of advanced SiGe: C BiCMOS HBTs

and of nanometric CMOS FET, *PhD Thesis*, University of Bordeaux, 2012. http://www.theses.fr/2012BOR14557

[16] B. Grandchamp, V. Nodjiadjim, M. Zaknoune, G. A. Koné, C. Hainaut, J. Godin, M. Riet, T. Zimmer, and C. Maneux, "Trends in Submicrometer InP-Based HBT Architecture Targeting Thermal Management", IEEE Trans. Electron Dev, vol. 58, no. 8, pp. 2566-2572, Aug. 2011. DOI: 10.1109/TED.2011.2150224

[17] G. A. Kone, B. Grandchamp, C. Hainaut, F. Marc, N. Labat, T. Zimmer, V. Nodjiadjim, M. Riet, J. Dupuy, J. Godin, C. Maneux, "Submicrometer InP/InGaAs DHBT Architecture Enhancements Targeting Reliability Improvements", IEEE Trans. Electron Dev., vol. 60, no. 3, pp. 1068-1074, 2013. DOI: 10.1109/TED.2013.2241067

[18] S. Balanethiram, R. D'Esposito, S. Fregonese, T. Zimmer, J. Berkner, and D. Celi, "Extracting the temperature dependence of thermal resistance from temperature-controlled DC measurements of SiGe HBTs," *Proc. IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM)*, 2017, pp. 94–97. DOI: 10.1109/BCTM.2017.8112919.

[19] M. Weiß, S. Fregonese, M. Santorelli, A. K. Sahoo, C. Maneux, and T. Zimmer, "Pulsed IV - pulsed RF measurement system for microwave device characterization with 80ns/45GHz," in *2012 Proceedings of the European Solid-State Device Research Conference (ESSDERC)*, 2012, pp. 189–192, DOI: 10.1109/ESSDERC.2012.6343365.