An Analog CMOS Voltage-Controlled Phase-Shifter With A 100° Tuning Range For Telecommunication Baseband Signal Processing

Blaise Mulliez, Olivier Bernal, Hélène Tap

An Analog CMOS Voltage-Controlled Phase-Shifter With A 100° Tuning Range For Telecommunication Baseband Signal Processing

Blaise MULLIEZ
LAAS-CNRS, Université de Toulouse
INP-ENSEEIHT
Toulouse, France
bmulliez@enseeiht.fr

Olivier BERNAL
LAAS-CNRS, Université de Toulouse
INP-ENSEEIHT
Toulouse, France
obernal@enseeiht.fr

Hélène TAP
LAAS-CNRS, Université de Toulouse
INP-ENSEEIHT
Toulouse, France
tap@enseeiht.fr

***Abstract*—In order to correct phase non-linearities due to High Power Amplifiers (HPA) operating near saturation in telecommunication transceivers, a voltage-controlled phase-shifter based on Differential Difference Current Conveyors (DDCC) and a tunable resistor were developed. In order to suit a large variety of HPAs with broad phase non-linearities, the circuit's tuning capability has even been optimized up to an unprecedented 100° while maintaining a good linearity (THD<-30 dB) and a gain close to 0 dB at 50 MHz. Designed in a 3.3 V 0.35 μm CMOS technology, the circuit current consumption ranges from 3.5 mA to 4.5 mA for a 50 MHz bandwidth, depending on the tuning range to be achieved. This paper describes the general architecture of the phase shifter as well as the inner structure of each implemented function and presents simulation results of the whole circuit.**

***Index Terms*—Phase-shifter, All-pass filter, ASIC, CMOS, DDCC, EOTA, phase linearization.**

I. Introduction

In satellite telecommunications, power and spectral efficiencies are the two main concerns. In particular, some High Power Amplifiers (HPA) have to operate close to saturation so as to achieve the maximum power efficiency onboard. Nevertheless, this leads to amplitude and phase non-linearities, strong distortions of the transmitted signals and a deteriorated link transmission quality [1].

There are several solutions to operate the HPA close to its saturation point without generating non-linearities [2]. One method is called the predistortion and consists in implementing a module among the equipment located before the HPA, to obtain a linear transfer characteristic of the whole transmission chain [2], [3]. This method is interesting in case of payloads with on-board processing, since it becomes possible to predistort the signal at intermediate frequency before frequency transposition and HPA amplification. Thus, the predistortion system may operate in lower frequency bands, which opens new technological solutions never explored before. Particularly, amplitude and phase distortions issues can be addressed independently, at intermediate frequency.

The phase non-linearity characteristic depends on the HPA itself and on the signal power at the amplifier input and can vary over several tenths of degrees. Further, it varies with time, along with temperature drifts and components aging. In this context, a circuit that can provide phase distortion compensation, that is real-time tunable and introduces neither any other non-linearities nor amplitude loss, is needed.

The authors would like to thank the French National Centre for Space Studies (CNES) for their technical and financial support and the French General Armament Direction (DGA) for their financial support.

TABLE I
PROPOSED PHASE SHIFTER TARGETED SPECIFICATIONS

Property	Value
Peak-to-peak input amplitude	250 mV
Bandwidth	$>$ 50 MHz
Tuning range	$>$ 60°
Gain	within $\pm$ 200 mdB
THD @ 50 MHz	$<$ -30 dB

This paper presents an analog phase-shift circuit designed to take into account those concerns. An analog architecture was chosen to comply with stringent accuracy, consumption and bandwidth considerations. Here, as a proof of concept, the circuit was optimized to fit HPA characteristics provided by the CNES for a 50 MHz input signal bandwidth, that corresponds to a 200 Mbp/s rate with 16-QAM non-constant envelope modulation. The circuit was implemented in a CMOS technology. Table I describes the aimed specifications of the circuit. The architecture, based on Differential Difference Current Conveyors (DDCC) and a tunable resistor, as well as transfer functions of each sub-circuit are presented in section II. Then, sections III and IV detail the CMOS integrations of the proposed DDCC and voltage-controlled resistor. The simulation results of the whole architecture are shown in part V. Finally, the conclusions are drawn in section VI.

II. Phase shifter architecture

A. State of the art

Analog phase shifting circuits are mainly implemented as all-pass filters [4]–[10]. This family of filters exhibits a constant gain (usually 0 dB) over their whole operating frequency range and a phase, sometimes tunable via biasing voltage or current adjustment or passive component values modification. Many CMOS implementations have been introduced in the literature: in [4]–[6], over 60 distinct solutions are presented and compared. Among all the existing circuits to the best of our knowledge, none showed the characteristics required for the linearization of HPA and telecommunication

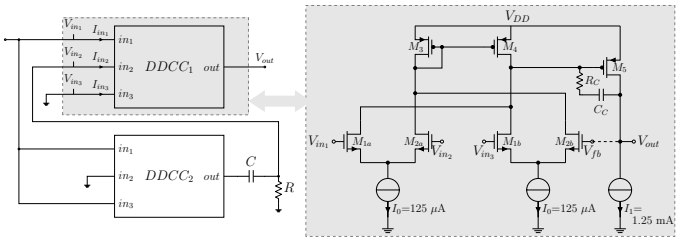


Fig. 1. Architecture of the proposed phase shifter circuit on the left, with DDCC CMOS implementation (on the right), based on a DDA architecture including a feedback in dotted line between the ouput V_{out} and the input V_{fb}

baseband signal processing. First, some cannot be tuned [5]–[7]. When the circuit is tunable, the phase shift range is either limited [8], [9], or maximal at frequencies too low for baseband signal processing and phase HPA linearization [4], [10]. Further, tunability is often implemented through current biaising modifications of active blocks over several decades, which results in linearity issues [4], [5], [8]. In some cases, the architecture complexity may also prevent the use of these circuits in the context of HPA phase linearization [8], [11]. Nevertheless, architectures based on DDCC [9], [10], [12] show relatively good performances in terms of tuning range for an architecture rather simple to implement. However, none of them can be directly used because they do not meet the specifications mentioned above and because they do not include the implementation of a tunable passive component. Here, a new approach is proposed that achieves a highly linear, widely tunable phase shifting circuit, optimized for a 50 MHz operation.

B. Proposed phase-shifter architecture

The proposed phase-shifter (Fig. 1) consists in two DDCCs, one capacitor and one resistor. As mentioned in the previous section, the DDCC (Fig. 1, in gray) is one of the key block of our proposed phase shifter. Its input/output voltages and currents satisfy:

$$I_{in1} = I_{in2} = I_{in3} = 0 \tag{1}$$

$$V_{out} = V_{in1} - V_{in2} + V_{in3} \tag{2}$$

Therefore, the phase-shifter transfer function is:

$$H(j\omega) = \frac{1 - jRC\omega}{1 + jRC\omega} \tag{3}$$

Its gain is $|H(j\omega)| = 1$ and its phase is $\angle H(j\omega) = -2arctan(RC\omega)$.

It is therefore an all-pass filter with a 0 dB gain and a phase that can be adjusted thanks to a variable resistor and/or capacitor (or varactor). Yet, no varactors complying with the constraints of HPA linearization are available either in the AMS design kit or in literature: they either suffer from an insufficient tuning phase range or from a too narrow bandwidth [13], [14]. Therefore here, the capacitor is fixed and a variable resistor is implemented instead.

In the following section, the CMOS implementation of the DDCC and of a voltage-controlled resistor are presented, complying with the frequency and linearity constraints of phase linearization, to create a phase shifter with a large bandwidth and an unprecedented phase shift tuning range (over 100°) at 50 MHz.

III. DDCC IMPLEMENTATION

The DDCC is based on a Differential Difference Amplifier (DDA) introduced in [15], with a negative feedback. The schematic of the DDA (or the DDCC including feedback) is shown in Fig 1. Its operating principle has been thoroughly described in [12].

Note that the complete DDCC introduced in [12] includes an additional high impedance output stage, useless here, thus not shown.

Here, the transistors channel sizes and the current sources values have been optimized in the AMS 0.35 μm CMOS technology, with a supply voltage of 3.3 V, in order to keep all transistors in saturation within the whole phase shifter operating range, and to maintain the distortion as low as possible for input signals up to 500 mV peak to peak for a bandwidth larger than 50 MHz. The compensation capacitor C_C and resistor R_C have been added and sized to improve the DDCC stability [16].

Note that the targeted peak-to-peak input voltage for the whole phase shifter circuit is 250 mV (Table I) but the different building blocks have been overdesigned to accomodate PVT variations and architecture constraints.

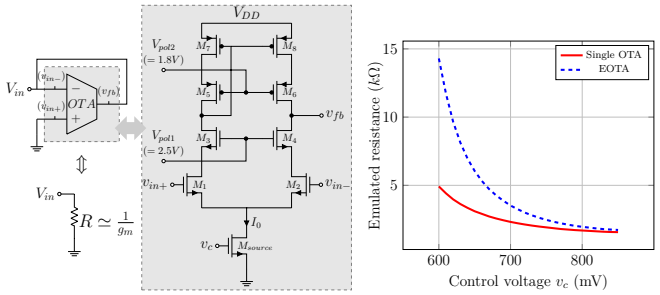
IV. VARIABLE RESISTOR IMPLEMENTATION

To determine the values of the fixed capacitor C and the tuning range of the resistor R, trade-offs need to be made. First, the phase-shift depends on $R \cdot C$ and follows an $arctan$ function. In order to achieve the maximum phase-shift range with a minimum $R \cdot C$ variation, $R \cdot C$ must be within the steep portion of the $arctan$ slope. Further, the capacitance has to be chosen large enough so as not to be in the same range as parasitic capacitances, but small enough so that the capacitor silicon area remains small. Taking into account these considerations as well as the processing of the data provided by the CNES, a suitable set $[R; C]$ is chosen with a capacitor of 1 pF and a resistor varying by at least a factor 2, with a minimal value between 200 Ω and 2 $k\Omega$.

Note that Resistor-DAC might sometimes be a satisfactory solution. However, HPA phase linearization requires continuous phase-shift performances and this kind of discretized approach cannot be chosen here.

A. Emulation of a resistor using an Operationnal Transconductance Amplifier (OTA)

The most versatile solution to emulate a resistor with one pin grounded, as shown in Fig. 1, is to use an OTA with a serial-shunt feedback on the inverter input, as shown in Fig. 2a [16]. The equivalent resistance is then: $R = 1/g_m$ where g_m is the OTA transconductance.



(a) (b)

Fig. 2. (a) Resistor implementation using an OTA [16] on the left and its CMOS telescopic cascode implementation on the right
(b) Emulated resistance as a function of v_c using a single OTA (red plain line) and a EOTA (blue dotted line) configured as in (a)

TABLE II

DDCC components' sizes	
Transistors	W/L(μm)
M_{1a-b}, M_{2a-b}	2/0.35
M_3, M_4	20/1.4
M_5	50/0.35
Passive comp.	Value
C_C	60 fF
R_C	440 Ω

EOTA components' sizes	
Transistors	W/L(μm)
M_1-M_4	8/0.5
M_5-M_8	40/0.5
M_{source}	50/0.7

Here, the OTA is implemented with a telescopic cascode architecture, presented in Fig. 2a. Since the transconductance g_m is proportional to $\sqrt{I_0}$ in strong inversion regime and, assuming that the transistor M_{source} remains in saturation, I_0 is proportional to $(v_c - V_T)^2$ where V_T is the threshold voltage of M_{source} and v_c an external control voltage injected at its gate. Thus, the R_{eq} is inversely proportional to $(v_c - V_T)$ and can be adjusted via the voltage v_c. By sizing the transistors and choosing the cascode voltages to comply with the considerations given above for a supply voltage of 3.3 V, we built a tunable resistor whose value varies from 1.4 $k\Omega$ to 4.8 $k\Omega$ for v_c varying from 850 mV down to 600 mV (Fig. 2b).

B. Extension of the resistance range

The use of a second OTA and of an additional resistor R_{conv} to create an Extended OTA (EOTA) (Fig. 3, in gray) [17] further enlarges the variation range of the emulated resistor since, with the use of 2 identical OTA, $R_{eq,EOTA} = 1/g_{m,EOTA} = 1/(R_{conv} \cdot g_m^2)$. The value of this extended emulated resistor varies from 1.8 $k\Omega$ to 15.3 $k\Omega$ for v_c from 850 mV down to 600 mV accordingly (Fig. 2b). Moreover, whatever the control voltage is, the THD at 50 MHz remains below -34 dB for input signal dynamics up to 500 mV peak-to-peak: the emulated resistance is highly linear.

The DDCC and EOTA component's sizes are presented in Table II.

V. Phase Shifter Simulations

The DDCC and the EOTA are combined to implement a phase shifter as shown in Fig. 3 and simulated at 50 MHz and with a varying control voltage v_c, at room temperature and in typical process conditions. In the proposed architecture,

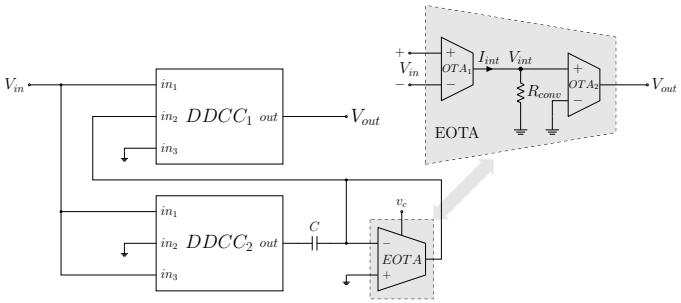


Fig. 3. Implementation of the phase-shifter with 2 DDCCs and an EOTA

$DDCC_2$ is configured as a voltage doubler circuit (as implied by Eq. 2) and its output is injected, through the RC filter, to one of the $DDCC_1$ inputs. Thus, to maintain $DDCC_1$ in its operating range, the input amplitude of the whole system is limited to 250 mV peak-to-peak.

A. Simulations for static values of v_c

Fig. 4 shows the transient response of the circuit for different values of the control voltage v_c (Fig. 4a), the gain and phase at the phase-shifter output (Fig. 4b) and the THD at 50 MHz (Fig. 4c) for v_c varying from 600 mV to 850 mV. Whatever the value of v_c is, the circuit plays the role of an all-pass filter with a gain close to 0 dB (average gain is -200 mdB). Moreover, the phase-shift of the circuit can be tuned via v_c from -59.7° to -173°, *i.e.* over an unprecedented 113.3° range (Fig. 4b), while remaining highly linear (Fig. 4c).

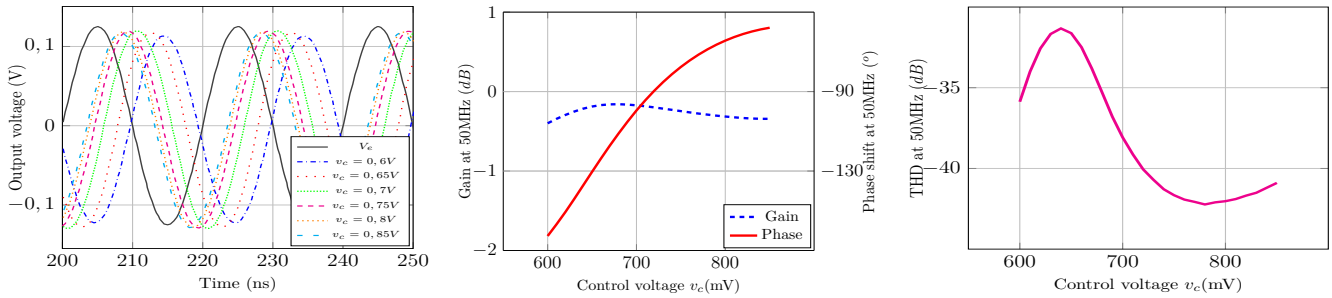
B. Results for v_c dynamically varying during transient simulations

In the context of phase linearization, the phase shift has to be dynamically modified. The circuit is therefore tested with sine wave input signals of 250 mV peak-to-peak at 50 MHz and v_c varying by steps along the simulation. In Fig. 5 v_c is incremented then decremented) by 50 mV steps every 20 ns. Its value is represented as a shaded background on the figures. When the differences in the phase-shift to generate is low (for instance, when v_c varies from 750 mV to 800 mV or from 800 mV to 750 mV), the output signal is stabilized within 5 ns. This time increases for higher differences in phase-shift to generate (*i.e.* for smaller values of v_c) but remains below 16 ns overall.

Depending on the voltage control amplitude, the average current consumption of the whole phase-shifter is between 3.5 mA and 4.5 mA under a supply voltage of 3.3 V.

C. Process and temperature influence on the overall performances

The whole circuit has been simulated over process and temperature variations (worst, typical, and best cases, -40°C, 27°C and 125°C). The maximum and minimum values are summarized in Table III. The achievable phase-shift range typically remains above 100° with a gain close to 0 and a low THD at 50 MHz. Nevertheless, in the context of HPA phase



(a) (b) (c)

Fig. 4. Transient and AC simulations of the proposed phase-shifter

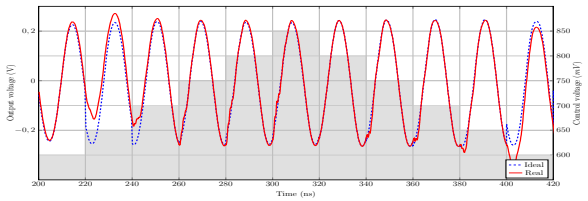


Fig. 5. Simulation of the phase-shifter output V_{out} for transient variations of the control voltage v_c (represented as shaded background)

TABLE III
CIRCUIT PERFORMANCES OVER PROCESS AND TEMPERATURE VARIATIONS

Property	Worst case	Typical	Best case
Phase tuning range (°)	87.9	113.3	148.5
Gain variation (dB)	2.02	0.40	0.24
THD @ 50 MHz (dB)	- 22.4	-30.5	-33.3

linearization, highly adaptive circuits are used and this particular phase-shifter will be embedded within a neural network capable of taking into account these process and temperature variations [3]. Thus, the phase-shifter performances comply with the constraints of phase linearization through all the process and/or temperature conditions.

VI. CONCLUSION

In this paper, a phase-shifter, with key specifications determined by the experimental data provided by the CNES in the context of phase linearization of HPA, is introduced. The objectives of its design are a wide range of tunability, a high operational frequency (50MHz) with low amplitude distortion. The proposed architecture uses 2 DDCCs, one EOTA and a fixed capacitor. The optimization of each block leads to the implementation of a highly linear, widely tunable circuit, capable of phase-shifting a 50 MHz input signal over an unprecedented range of 113.3°, with a THD lower than -34 dB in typical conditions, for an average current consumption of 3.5 to 4.5 mA (*cf.* Tab. III). Those performances are barely degradated over process and tempeature variations and, in any case, can be compensated thanks to neural networks control. Further, the circuit presents a fast response to dynamic voltage control modifications. With such versatility and performances, this circuit may be efficiently inserted into an analog processing chain of HPA linearization, and will be particularly appropriate for regenerative loads of future telecommunications satellites.

REFERENCES

[1] J. B. Sombrin, "Optimization criteria for power amplifiers," *Int J Microw Wirel T*, vol. 3, no. 1, pp. 35–45, February 2011.

[2] G. Lazzarin, S. Pupolin, and A. Sarti, "Nonlinearity compensation in digital radio systems," *IEEE T Commun*, vol. 42, no. 2-4, pp. 988–999, 1994.

[3] B. Mulliez, E. Moutaye, H. Tap, L. Gatet, and F. Gizard, "Predistortion system implementation based on analog neural networks for linearizing HPAñs transfer characteristics," *S2IS*, vol. 7, no. 1, pp. 400–422, March 2014.

[4] N. Herencsar, S. Minaei, J. Koton, E. Yuce, and K. Vrba, "New resistorless and electronically tunable realization of dual-output VM all-pass filter using VDIBA," *Analog Integr Circ S*, vol. 74, no. 1, pp. 141–154, January 2013.

[5] B. Metin, N. Herencsar, and K. Vrba, "A CMOS DCCII with a grounded capacitor based cascadable all-pass filter application," *Radioengineering*, vol. 21, no. 2, pp. 718–724, June 2012.

[6] A. Lahiri, "New CMOS-based resistor-less current-mode first-order all-pass filter using only ten transistors and one external capacitor," *Radioengineering*, vol. 20, no. 3, pp. 638–644, Sept. 2011.

[7] E. Yuce, S. Minaei, N. Herencsar, and J. Koton, "Realization of first-order current-mode filters with low number of MOS transistors," *J Circuit Syst Comp*, vol. 22, no. 01, pp. 125–139, 2013.

[8] N. Herencsar, J. Koton, K. Vrba, and S. Minaei, "Electronically tunable MOSFET-C voltage-mode all-pass filter based on universal voltage conveyor," in *ICCSN 2011*, May 2011, pp. 442–445.

[9] B. Chaturvedi and S. Maheshwari, "An ideal voltage-mode all-pass filter and its application," *JCC*, vol. 9, pp. 613–623, May 2012.

[10] R. Arslanalp, "A novel DDCC+ based first-order current-mode active-C all-pass filter using a grounded capacitor," *Turk J Electr Eng Co*, vol. 25, pp. 783–793, 2017.

[11] B. Metin and K. Pal, "New all-pass filter circuit compensating for C-CDBA nonidealities," *J Circuits, Syst Comp*, vol. 19, no. 02, pp. 381–391, 2010.

[12] W. Chiu, S.-I. Liu, H.-W. Tsao, and J.-J. Chen, "CMOS differential difference current conveyors and their applications," *IEE P-Circ Dev Syst*, vol. 143, no. 2, pp. 91–96, Apr 1996.

[13] R. L. Bunch and S. Raman, "Large-signal analysis of MOS varactors in CMOS-G_m LC VCOs," *IEEE J Solid-St Circ*, vol. 38, no. 8, pp. 1325–1332, August 2003.

[14] S. Chatterjee, T. Musah, Y. Tsividis, and P. Kinget, "Weak inversion MOS varactors for 0.5V analog integrated filters," in *S VLSI Tech*, June 2005, pp. 272–275.

[15] E. Sackinger and W. Guggenbuhl, "A versatile building block: the CMOS differential difference amplifier," *IEEE J Solid-St Circ*, vol. 22, no. 2, pp. 287–294, April 1987.

[16] P. R. Gray, P. J. Hurst, S. H. Lewis, and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*. Wiley, 2001.

[17] K. Kaewdang and W. Surakampontorn, "A wide tunable range CMOS OTA," in *ECTI-CON 2008*.