Three multi-terminal silicon power chips for an optimized monolithic integration of switching cells: validation on an H-bridge inverter

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***Abstract*— The paper deals with the monolithic integration in silicon of a multi-phase static power converter (DC/AC or AC/DC) for medium power applications from few kilowatts to few tens of kilowatts. The power devices blocking capability is in the range of 600V to 1200V. The authors present an original 3-chip integration approach that combines both monolithic integration in silicon and Printed Circuit Board (PCB) packaging process. It allows for taking advantage of both silicon level technology as well as PCB level technology within a limited and well-mastered complexity. Indeed, the multiphase converter is integrated within three new multi-terminal power chips, that are then judiciously packaged on a PCB board so as to minimize both the switching cell stray inductance as well as the impact of voltage variations (dv/dt) across the common mode stray capacitance of the assembly. The static as well as dynamic operating modes of the proposed multi-terminal power chips were validated using 2D-Sentaurus™ TCAD simulations. The realized chips were assembled on a PCB board to realize both classical as well as 3-chip based H-bridge inverters. First characterization results validate the electrical operating modes of the H-bridge inverter realized according to the 3-chip approach.**

***Index Terms*— monolithic integration, buck converter, orthogonal switching cell, stray inductance, reverse conducting IGBT, IGBT, PiN diode.**

I. Introduction

POWER modules are generally composed of discrete diode and IGBT chips that are interconnected by wire bonds. The modules are therefore bulky and their mass fabrication is limited in productivity. Wire bonds require an expensive wiring operation and are a source of reliability problems [1]-[3]. Moreover, they are a source of stray inductance [4] that limits the frequency of operation of the power modules. In addition, the power dies being bonded on their backside, the midpoints of each phase leg of the converter is on the circuit board's plane. As a result, the circuit board is directly subjected to voltage variations *(dv/dt)* during switching events, which is a source of the undesirable common mode current through the PCB board.

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In order to overcome these shortcomings, a significant breakthrough can be achieved by an optimized mixed hybrid/monolithic integration of the multi-phase power converters. Different monolithic "on-chip" integration approaches were proposed in literature [5][6]. However, they are either limited in performance due to lateral integration with vertical insulation trenches through the die [5] or require a complex technological process for their realization due to molecular bonding of two silicon wafers [6]. Within the same context, the authors have recently proposed a vertical quasi-monolithic integration of a multiphase converter called dual-chip approach (Fig. 1) as well as an ultra-compact single chip approach [7].

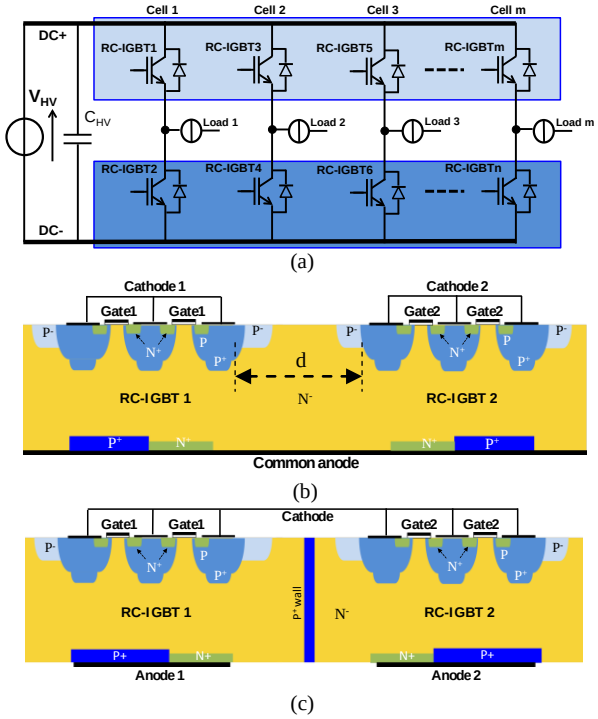


Fig. 1. The dual-chip integration concept [7]: (a) The multiphase converter, (b) cross-sectional view of the three-terminal common anode chip, (c) cross-sectional view of the three-terminal common cathode chip.

As one can notice in Fig. 1(b), no vertical P+ wall is required for electrical insulation between the adjacent Reverse Conducting Insulated Gate Bipolar Transistor (RC-IGBT) [8]-[12] in the three-terminal common anode chip. However, the P+ wall is required in the case of the three-terminal common cathode chip. The realization of this latter is complex. Indeed, it requires the realization of regularly spaced deep trenches [13] that are then filled with highly boron-doped polysilicon.

After an annealing step, at a high temperature, the diffusion of boron atoms within the silicon volume allows to materialize the vertical P^+ wall [14]. The realization of deep trenches in silicon makes the wafer handling difficult as they can affect the mechanical rigidity of the silicon wafer. To overcome this technological complexity, the authors propose in this paper the three-chip integration approach. It should be noted that with this new approach the switching cell electrical performance is identical to that of the dual-chip approach [7].

II. THE THREE-CHIP INTEGRATION CONCEPT

Wire bonds in power modules are source of parasitic inductance [1-2] that induces high turn-off voltage overshoot, which not only add electrical stress on the power dies, but also result in switching losses and thus affect the overall efficiency. To improve reliability, electrical performance and reduce cost of power modules, significant breakthrough can be achieved by the monolithic integration of the 2D-multiphase module within three multi-terminal silicon chips that are judiciously packaged so as to minimize the number of wirebonds, the switching cell stray inductance as well as the impact of voltage variations on the common mode current that flows through the converter's PCB.

As shown in Fig.2, according to the three chip concept, the high-side row is integrated in one monolithic multi-terminal chip consisting of RC-IGBT transistors. The low-side row is integrated within two distinct monolithic multi-terminal power chips: the IGBTs are integrated within one dedicated single multi-IGBT power chip, while the PiN diodes are integrated within another dedicated multi-diode power chip. This offers an easier insulation management between the switches within each multi-terminal chip.

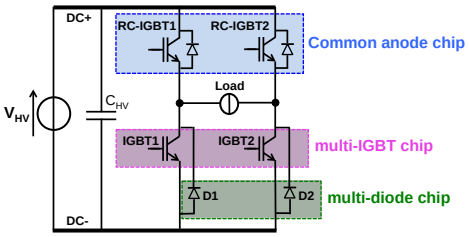


Fig. 2. Principle of the three-chip integration concept.

The packaging of these chips is presented in Fig. 3. The common anode chip is placed at the center, and the two low-side chips are symmetrically positioned on each side of it. The multi-IGBT chip is flipped then bonded on the PCB board. In Fig. 3, wire bonds are used for illustration purposes although the authors have studied their replacement by copper clips offering more compactness and less stray inductance [24]-[25]. For the case of an H-bridge inverter, each monolithic multi-terminal chip is composed of only two switches. The common-anode power chip in Fig. 1(b) is made of two RC-IGBT transistors. The multi-IGBT power chip in Fig. 4 is composed of two IGBTs that share the same N^- epitaxial drift region. The electrical insulation between the IGBT transistors is achieved by non-through P^+ wall that extends from the top face of the wafer down to the backside P^+ substrate. Consequently, as compared to the case of the P^+ wall used in the common-cathode multi-terminal power chip [Fig. 1(c)] [7][14], its technological realization is easier.

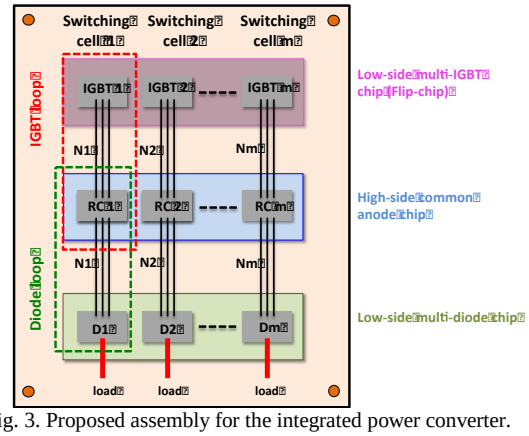


Fig. 3. Proposed assembly for the integrated power converter.

The non-through trenches can be filled either by a highly boron-doped polysilicon to realize a P^+ deep trench [14] or by a dielectric [16]-[17]. On the backside, a trench filled by a dielectric [15] is necessary for electrical insulation between anode1 and anode2. The combination of this latter with the non-through P^+ wall ensures the lateral voltage blocking between anode1 and anode2 electrodes.

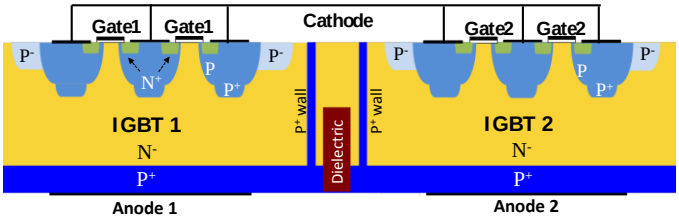


Fig. 4. Cross-sectional view of the common cathode multi-IGBT chip.

The multi-diode power chip in Fig. 5 consists of two diodes that share the same N^- drift region. Similarly to the multi-IGBT chip, electrical insulation between adjacent diodes can also be achieved either by non-through P^+ deep trenches [14] or by non-through trenches filled by a dielectric [16]-[17]. To make easier the packaging of the multiphase converter on a PCB/DBC (Direct Bond Copper)/IMS (Insulated Metal Substrate), the architecture of the multi-diode chip is designed so as to have the common P^+ region on the bottom side of the chip. Indeed, this allows the multi-diode chip to be directly bonded to the PCB substrate by its backside common electrode avoiding a flip-chip operation. The lateral voltage blocking between anode1 and anode2 is achieved by the reverse biased junction backside_P+_P^+wall/N-.

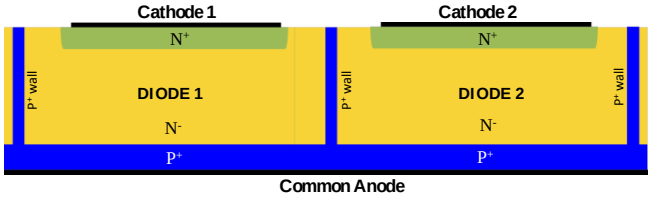


Fig. 5. Cross-sectional view of the common anode multi-diode chip.

III. VALIDATION OF THE OPERATING MODES OF THE THREE MULTI-TERMINAL CHIPS

The proposed chips are studied using 2D TCAD Sentaurus™ simulations [18]. The active area of each switch section is set to 1 cm^2. Each monolithic chip has to support 600 V both vertically and laterally, and to carry out a 100 A DC-current. For illustration purposes, Fig. 6 shows a cross sectional view of a planar RC-IGBT section and the main parameters of the diffusion regions. Minority carrier lifetimes τ_{n0} = 5 µs and τ_{p0} = 3 µs were used in simulations. Table 1 summarizes the main geometrical and physical parameters of the elementary RC-IGBT section.

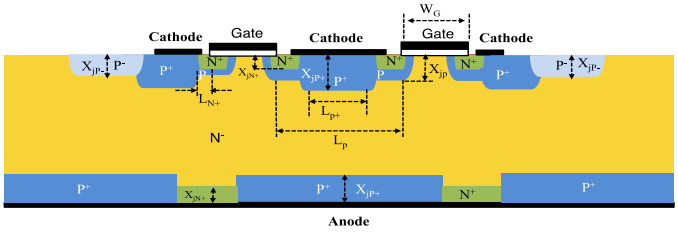


Fig. 6. Schematic cross-sectional view of an RC-IGBT section illustrating the geometrical parameters used in 2D simulations.

TABLE 1. MAIN GEOMETRICAL AND PHYSICAL PARAMETERS USED IN 2D-SIMULATIONS

Symbol	Parameter	Value	Doping concentration
W_G	Gate width	30 µm	
e_{ox}	Gate oxide thickness	55 nm	
L_{P^-}	P^- junction termination	80 µm	$9X10^{15}$ cm^{-3}
X_{jP^-}	P^- junction depth	4 µm	
L_P	P diffusion width	48 µm	$2.5X10^{17}$ cm^{-3}
X_{jP}	P diffusion depth	5 µm	
L_{P+}	P^+ diffusion width	26 µm	$5X10^{19}$ cm^{-3}
X_{jP+}	P^+ diffusion depth	7 µm	
L_{N+}	N^+ diffusion width	18 µm	$1X10^{20}$ cm^{-3}
X_{jN+}	N^+ diffusion depth	1 µm	

Each multi-terminal chip was first simulated separately to validate its static operating modes. Then, the three multi-terminal chips were assembled to realize an inverter circuit and validate the dynamic operating modes of the chips.

A. *Static analysis of the monolithic multi-terminal chips*

Each multi-terminal chip (common anode, multi-IGBT and multi-diode) was simulated in worst-case conditions that would correspond to its static operating mode in an inverter application. Indeed, in each monolithic chip, this condition occurs when one switch (IGBT, diode or RC-IGBT) in a multi-terminal chip is ON-state while the adjacent section is in OFF-state and supports the applied DC-bus voltage.

1) *The three terminal common anode chip*

The simulation conditions are given in Fig. 7. Contrary to the case of the multi-IGBT chip [Fig. 4] and multi-diode chip [Fig. 5], the vertical P+ wall is not required in the common anode chip [7]. A gate-cathode voltage of 15 V is applied to the gate of RC-IGBT2 with respect to cathode2 while gate1 is tied to the cathode1. A 600 V DC-voltage source is connected between cathode2 and cathode1 and a DC-current source of 100 A is connected to the common anode electrode. As shown in Fig. 8(b), a space charge region expands on both sides of the reverse biased P/N^- junction in the RC-IGBT1. The separation distance between the two RC-IGBT sections used in these simulations is d = 1 mm [7]. The current density distribution in the structure, in IGBT mode, is given in Fig. 8(a). The RC-IGBT2 is in ON-state while RC-IGBT1 is in OFF-state. The load current flows through the right side IGBT section. The leakage current through the OFF-state RC-IGBT1 is negligible (~ 6.9 µA). The leakage current in the common anode chip decreases with the increase of the separation distance "d" [7]. For a distance d≥1mm, the electrical interaction between the two vertical RC_IGBTs is negligible.

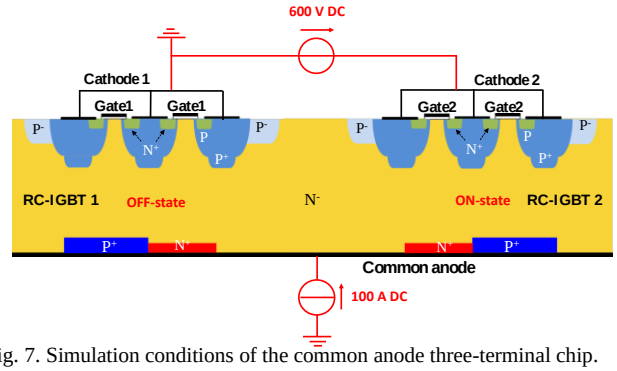


Fig. 7. Simulation conditions of the common anode three-terminal chip.

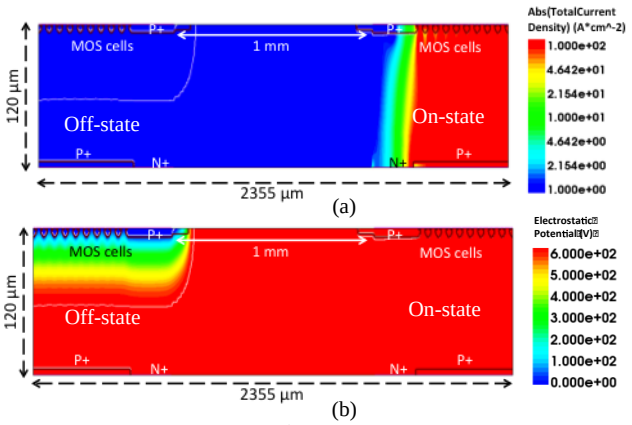


Fig. 8. 2D simulation results of the common anode three-terminal chip: (a) current density distribution and (b) equipotential lines distribution.

2) *The multi-IGBT chip*

The simulation conditions are given in Fig. 9. A DC-voltage source of 600 V is applied between the electrodes anode2 and anode1, and a DC-current source of 100 A is connected to the common-cathode electrode. The backside dielectric region (SiO_2) is necessary for electrical insulation between anode 1 and anode 2. The doping concentration of the P^+ wall is $5x10^{19}$ cm^{-3}. The left-side IGBT section is in ON-state while the right-side IGBT section is in OFF-state. The applied voltage between anode2 and anode1 is supported both vertically by the reverse biased P/N^- of IGBT2 and also horizontally by both the reverse biased junction deep-P^+wall/N^- and the dielectric region, as shown in Fig. 10(b). For the sake of illustration, the current density distribution as well

as equipotential lines distribution for the case of L_{SiO2} = 300 µm, D_{SiO2} = 5 µm and W_{Pwall} = 20 µm are given in Fig. 10. The leakage current through the OFF-state IGBT section depends on the length of the backside dielectric trench (L_{SiO2}), on the depth of the dielectric trench (D_{SiO2}) as well as on the width of the P^+ wall (W_{Pwall}). Indeed, as shown in Fig. 11, the leakage current decreases with the increase of L_{SiO2}, D_{SiO2} and W_{Pwall}. According to Fig. 11(b), for D_{SiO2} higher or equal to 5 µm, the dependence of the leakage current on D_{SiO2} is negligible. Qualitatively, for L_{SiO2} higher than 300 µm, D_{SiO2} higher than 5 µm and W_{Pwall} higher than 30 µm, the leakage current through the off-state IGBT section is negligible as compared to the nominal on-state current.

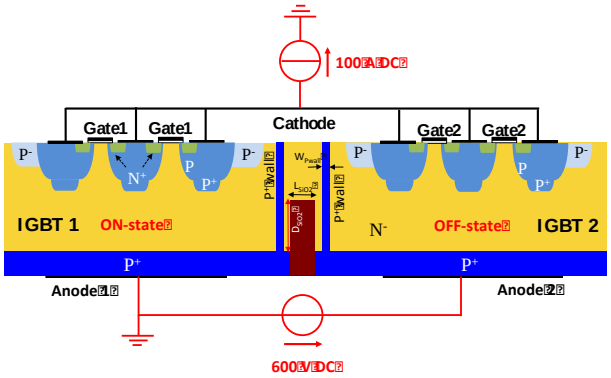


Fig. 9. Simulation conditions of the common cathode multi-IGBT chip.

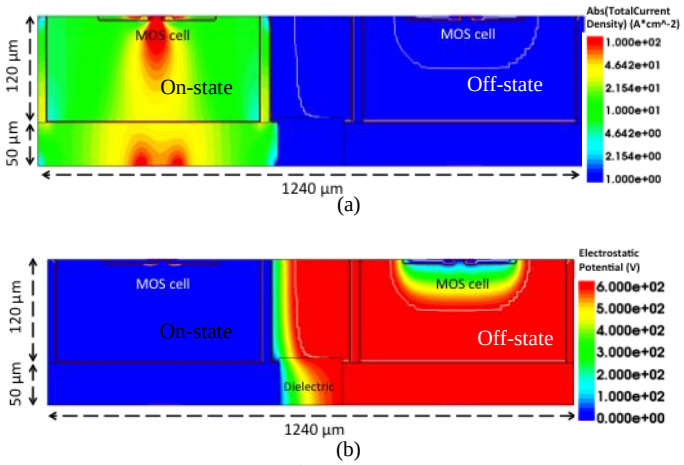


Fig. 10. 2D simulation results of the common cathode multi-IGBT chip: (a) current density distribution and (b) equipotential lines distribution. Case where L_{SiO2} = 300 µm, D_{SiO2} = 5 µm and W_{Pwall} = 20 µm, P_{wall} doping = $5x10^{19}$ cm^{-3}.

The impact of capacitive current through the P+(wall)/N- junction capacitance was studied by the authors in a similar multi-terminal chip called "three terminal common cathode chip consisting of two RC-IGBTs" [7]. For a dv/dt = 10kV/µs, the equivalent stray capacitance of the P+ wall is approximately equal to 40pF. The area factor of the simulated P+ wall in [7] is 4 cm, this value corresponds to the perimeter of an RC-IGBT chip of 1 cm2 surrounded by the P+ wall. Considering IGBT technology, this value of parasitic capacitance is very small. The influence of this capacitance in switching phases, compared with the discrete case, is negligible. In the case of fast wide-band-gap, such an order of magnitude can no longer be negligible. However, in this case, this stray capacitance does not seem to be the most relevant to consider. The equivalent capacitance between anode and gate electrodes is the most important factor in the switching speed because Cga (gate - anode capacitor) is directly involved through the Miller plateau sequence of the dv/dt. In this case, the layout of the PCB on which the chips are assembled must be carefully designed to minimize additional stray capacitance in parallel of the Cga's chips [26].

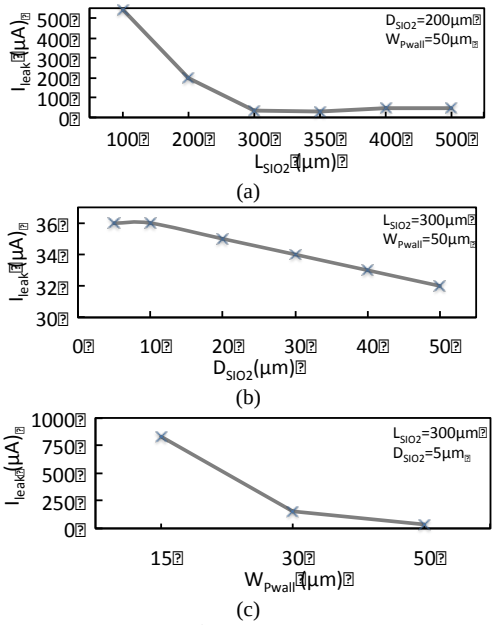


Fig. 11. Qualitative evaluation of the leakage current in the OFF-state IGBT section as function of: (a) the length of the backside oxide trench (L_{SiO2}), (b) the depth of the backside oxide trench (D_{SiO2}) and (c) the width of the P^+ wall (W_{Pwall}), P_{wall} doping = $5x10^{19}$ cm^{-3}.

3) The multi-diode power chip

The simulation conditions are given in Fig. 12. The N^+ area (W_{N+} x area-factor Z) in each diode is set to $1cm^2$. The N^+ junction depth is 1 µm and surface concentration $1x10^{20}$ cm^{-3}. The left-side diode is in ON-state and carries a current density of 100 A/cm^2, while the right side diode is in OFF-state. As shown in Fig. 13, the applied voltage is supported both vertically and laterally by the right-side diode (diode 2). In the case of a deep P^+ trench, the leakage current through OFF-state section depends both on the width (W_{Pwall}) and the doping concentration of the deep P^+ trench. The doping concentration of the P^+ wall is $5x10^{19}$ cm^{-3}.

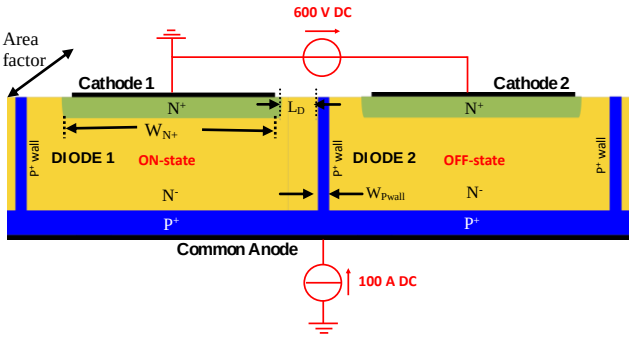


Fig. 12. Simulation conditions of the common anode multi-diode chip.

As shown in Fig. 14, the leakage current through the OFF-state diode section depends on the P^+ wall width (W_{Pwall}) and on the distance L_D that separates N^+ cathode diffusion from the P^+ wall. Qualitative 2D simulations showed that for W_{Pwall} higher than 20 µm and L_D higher than 250 µm, the leakage current through the simulated OFF-state diode section is lower than 20 µA.

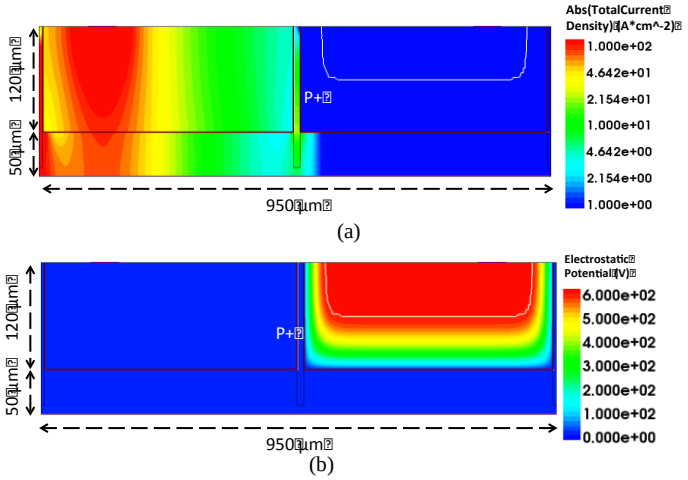


Fig. 13. 2D simulation results of the common anode multi-diode chip: (a) current density distribution and (b) equipotential lines distribution. W_{Pwall} = 20 µm, P_{wall} doping = $5x10^{19}$ cm^{-3}.

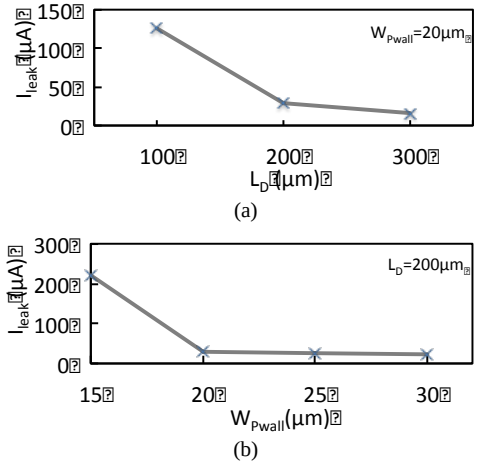


Fig.14. Qualitative leakage current evaluation in the OFF-state diode section as function of: (a) distance L_D, (b) P^+ wall width W_{Pwall}. P_{wall} doping = $5x10^{19}$ cm^{-3}.

B. Dynamic analysis of the monolithic chips

The previous three power chips were assembled to form a two-phase voltage inverter circuit of Fig. 15(a). The circuit is studied using 2D Sentaurus™ mixed mode simulations. To avoid excessive simulation time and convergence problems, the stray inductances, stray capacitors and decoupling capacitors were not included in the simulated circuit of Fig. 15(a). This is carried-out experimentally on the realized converter Fig. 16. A DC-voltage source of only 100V between the Bus and Ground electrodes is applied in this qualitative simulation. A unidirectional DC-current source of 100 A is connected between the mid-points of the H-bridge. The phase legs are controlled diagonally to realize a two-level voltage inverter. So, one can distinguish two conduction phases:

- Conduction phase 1 in which the high-side IGBT (in RC-IGBT 1) and the low-side IGBT 2 (in multi-IGBT chip) are in ON-state;
- Conduction phase 2 in which the high-side body-diode (in RC-IGBT 2) and the low-side diode D1 (in multi-diode chip) are in ON-state.

Fig. 15(a) shows the observed electrical quantities in the circuit, and Fig. 15(b) and (c) show a zoom into the turn-off and turn-on waveforms of RC-IGBT1, respectively. The different waveforms are similar to those that one can observe in the classical discrete case.

IV. SINGLE PHASE INVERTER REALIZATION

The targeted single-phase converter is shown in Fig. 16. The chips are positioned on the PCB as detailed in §II. Each phase leg is made of two distinct switching loops ($L_{loop\text{-}IGBT}$ and $L_{loop\text{-}diode}$) but only one loop is electrically involved at a time.

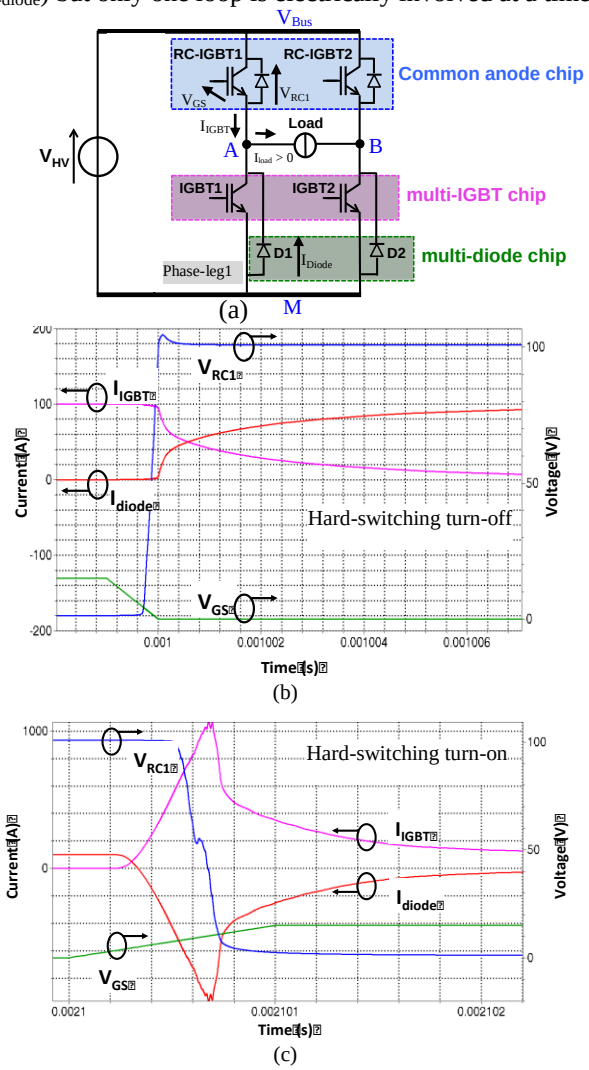


Fig. 15. Mixed-mode Sentaurus™ 2D simulations of the single-phase inverter: (a) H-bridge circuit consisting of the three multi-terminal chips, (b) zoom into the turn-off of RC-IGBT1, (c) zoom into the turn-on of RC-IGBT1.

The three-terminal common anode chip consisting of two

monolithically integrated RC-IGBT structures, discrete RC-IGBT and IGBT power chips were realized at LAAS-CNRS micro and nanotechnology platform:

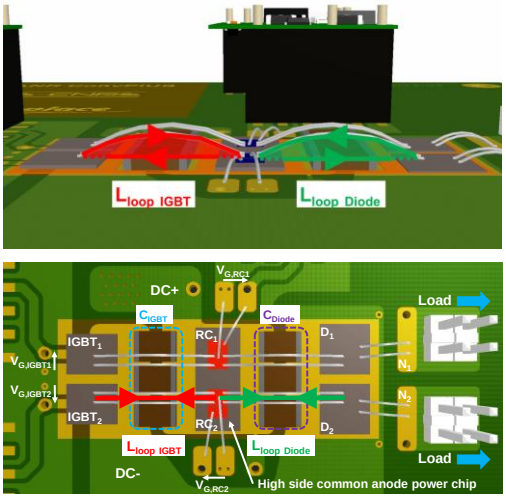


Fig. 16. Layout of the single-phase full-bridge voltage inverter for the proposed 3-chip approach with orthogonal switching loop with respect to the PCB plane.

Fig. 17(a) shows the top view of the realized common anode three-terminal chips. The starting silicon wafers were 300 µm thick, and uniformly doped (10^{14} cm^{-3}). Fig. 17(c) and Fig. 17(d) show respectively the forward and reverse on-state *I(V)* characteristics of the RC-IGBT of one common anode chip. The snap-back in the forward ON-state *I(V)* characteristics of the RC-IGBT is suppressed because the backside P^+ diffusion is very large (> 1 mm) [22]. Fig. 17(b) shows the *I(V)* characteristics of the two RC-IGBT sections that compose one common anode three-terminal chip, for the case in which one RC-IGBT section is in ON-state while the other RC-IGBT section is in OFF-state. The leakage current ($I_{cathode2}$) through the RC-IGBT section, which is in OFF-state, is negligible.

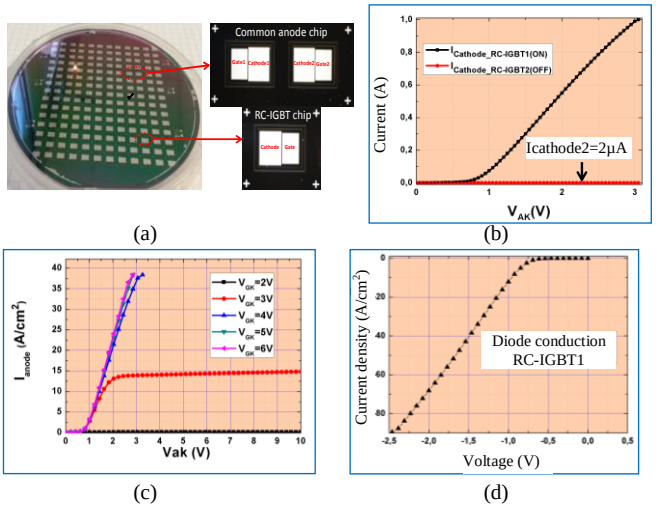


Fig. 17. (a) Realized common anode three-terminal chips (RC-IGBT1 in on-state while RC-IGBT2 in off-state) [7]. On-wafer characterizations of the common anode chip: (b) one RC-IGBT section is in on-state while the other is in off-state, (c) I(V) characteristics for the IGBT mode of the RC-IGBT, (d) I(V) characteristics for the diode mode of the RC-IGBT.

Fig. 18 shows the realized two-terminal IGBT chip [19]. The threshold voltage is about 2V. This is lower than that of the simulated devices (about 3V). For wafer handling reasons, a thick wafer (300 µm) was used. However, this leads to a high ON-state voltage drop (Fig. 18). It is about 4V at an anode current of 1A and V_{GK}=4V The on-wafer characterizations of the device show that it is able to support about 400 V. This is lower than the desired breakdown voltage 600V.

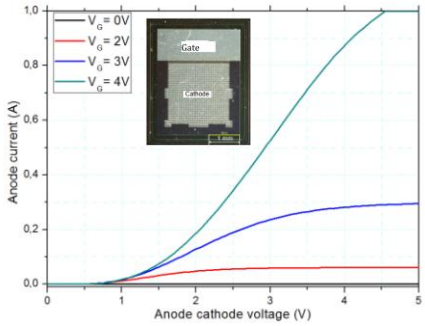


Fig. 18. The used IGBT chips [19] [23] in the 3-chip converter assembly: ON-state I(V) characteristics, chip dimensions: 4.3 mm x 5 mm x 300 µm.

The realized converter for validating the three-chip concept is given in Fig. 19(a). The IGBT chips were flipped and then bonded on the PCB substrate. To that end, an insulating 75 µm-thick kapton™ layer is used. Using a carbon dioxide laser (CO_2 laser), the kapton layer is precisely patterned to be consistent with the power chips to be bonded and assembled. Then, an electrically conducting epoxy (EpoTek H20E) is used in order to bond the chips on the PCB board.

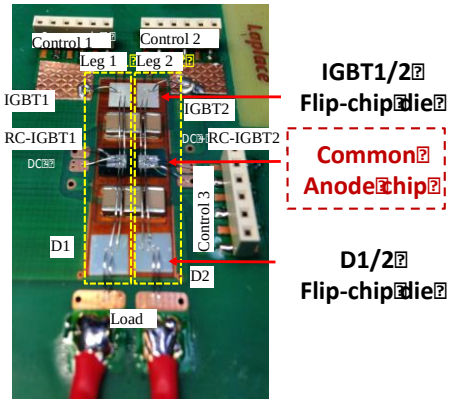
The common anode three-terminal chip is bonded on its backside anode electrode. Two discrete IGBT chips [19] are flipped in low-side configuration and bonded on the left side of the common anode chip. These two IGBTs replace, in these assemblies, the multi-terminal low-side two-IGBT monolithic chip presented in §II. Moreover, two commercial discrete fast power diode chips are bonded on the right side of the common anode chip in low side configuration. These two diodes replace the monolithic multi-terminal two-diode chip also described in §II.

V. Electrical Characterization Results

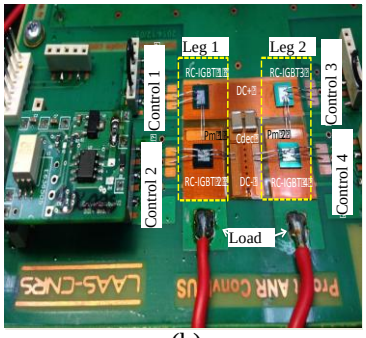
Fig. 19 shows the realized two full-bridge voltage inverters based on the schematic drawn in Fig. 15a). The voltage inverter of Fig. 19(a) makes use of the 3-chip approach while the voltage inverter of Fig. 19(b) is the reference assembly realized using four RC-IGBT chips. Each voltage inverter is controlled with a diagonal conduction setting of two controlled devices out of four. For the 3-chip inverter in Fig. 19a) : RC-IGBT1 and IGBT2 are turned-on over a first half switching period, RC-IGBT2 and IGBT1 are turned-on over a second half switching period. For the reference inverter in Fig. 19b) : RC-IGBT1 and RC-IGBT4 are turned-on over a first half switching period, RC-IGBT2 and RC-IGBT4 are turned-on over a second half switching period. Such a basic control provides a 2-level output voltage across the inductive load leading to a zero-voltage-switching (ZVS) operation of all controlled devices. On the one hand this allows to avoid hard switching and the reverse recovery current of the

integrated antiparallel diodes during switching phases and focus the study on the main functional validation. On the other hand, the ZVS mode allows no cross-talk between controlled devices of each leg and no gate-emitter spike voltage as it could be seen in hard switching mode with a possible short shoot-through conduction [27]. Note that all these properties are common to both test structures.

Fig. 20(a) shows the waveforms of the current through the load (green trace) and the voltage across the load (blue trace) for the case of the proposed three-chip approach. At the zero crossing of the load current, and depending on the current sign (direction), it is either the IGBT or the diode (high-side), of the same RC-IGBT section, within the common anode chip, that ensures current conduction.



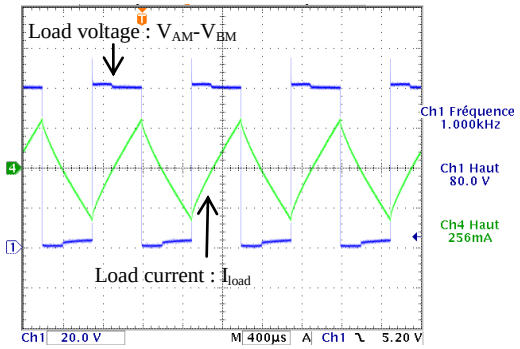
(a)



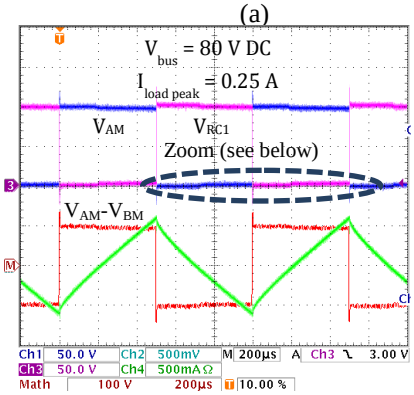
(b)

Fig. 19. (a) Realized 3-chip inverter *using one common anode chip (11.2mm X 4.9mm X300*µm*), two IGBTs and two diodes (SIDC30D120H8).* (b) Realized reference inverter using four RC-IGBT chips *(5.6mm X 4.9mm X300*µm*).* (Capacitor: Kemet C1812V104KCRACTU /0.1µF/500V/X7R)

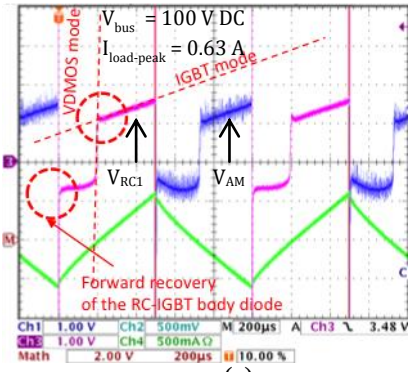
When the integrated diode turns-on, a slight overshoot in the voltage waveform due to the RC-IGBT's diode forward recovery is observed. The forward-recovery spike does not appear in low-side conduction because commercial diodes used are ultra-fast devices. The current conduction of the low-side power chips takes place only when the voltage across the low-side IGBT or diode chips reaches the built-in voltage ~ 0.8 V. This proposed three-chip converter assembly uses an orthogonal switching cell that was characterized using the double-pulse method [24]. The extracted stray inductance of the switching cell was about 4.2 nH. In Fig. 20(b) and Fig. 20(c), the reference converter assembly made of four RC-IGBTs shows the same properties as those of Fig. 20(a) even though forward diode recovery spikes are visible in all our four academic RC-IGBT chips. This 2D-planar reference converter assembly was also evaluated using the double-pulse method. The extracted stray inductance of the switching cell was about 10.2 nH which is more than two times higher than that of the proposed three-chip converter assembly.



(a)



(b)



(c)

Fig. 20. (a) Waveforms of the load current and voltage across the load for the proposed three-chip inverter consisting of one common anode chip, 2 IGBT chips and two diode chips, *(b)* Waveforms of the load current and voltage across the load for the reference assembly consisting of 4 RC-IGBTs (full bridge). For both inverters : control ZVS – load 50mH 10Ω (F_{SW}=1kHz, duty =½, T_{dead}=10µs, Rgon_ext=Rgoff_ext=0Ω), (c) Zoom into the region highlighted in graph (b).

VI. CONCLUSION

Three new monolithic silicon multi-terminal power chips designed for the integration of a multiphase converter within only three power chips were studied by extensive 2D-simulations. The concept aims at improving the compactness, reliability and performance of power converters. The integrated converter takes advantage of both monolithic integration in silicon technology and PCB process technology

within a limited and acceptable level of complexity. The three-chip concept is validated through realization of an H-bridge ZVS-mode voltage inverter. The main advantages that can be brought by these chips within the context of multiphase power converters integration are:

- Simpler silicon technological process for the realization of the three power chips as compared to the case of multi-terminal chip(s) used in the dual-chip and single chip approaches [7].
- Simpler 2D-packaging technology process. Only three power chips need to be packaged as compared to the classical approach, which is based on the interconnection of a great number of discrete diode and IGBT chips. Orthogonal flat quasi-3D switching cells can be used between the dies resulting in a lower stray inductance as compared to that of the classical 2D-planar approach.

The substitution of each set of *Al*-wire bonds by Cu-clips or a flat sheet of Cu-metal allows the assembly to evolve towards Direct Lead Bonding (DLB) assembly that will reduce further the switching cell stray inductance [20].

REFERENCES

[1] B. Weiss *et al*., "Operation of PCB-Embedded, High Voltage Multilevel-Converter GaN-IC," 2017 *IEEE 5th Workshop on Wide Bandgap Devices and Applications (WiPDA), Albuquerque, NM,2017,pp. 398-403.* doi: 10.1109/WiPDA.2017.8170580

[2] S. QiN et al., "A High-Power-Density Power Factor Correction Front End Based On Seven-Level Flying Capacitor Multilevel Converter," *in IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 7, no. 3, pp. 1883-1898, Sept. 2019. doi: 10.1109/JESTPE.2018.2865597

[3] S. Li, L. M. Tolbert, F. Wang and F. Z. Peng, "Stray Inductance Reduction of Commutation Loop in the P-cell and N-cell-Based IGBT Phase Leg Module," in *IEEE Transactions on Power Electronics*, vol.29, no.7, pp.3616-3624, July2014. doi: 10.1109/TPEL.2013.2279258

[4] A. K. Solomon, A. Castellazzi, N. Delmonte and P. Cova, "Highly integrated low-inductive power switches using double-etched substrates with through-hole viases," *2015 IEEE 27th International Symposium on Power Semiconductor Devices & IC's (ISPSD)*, Hong Kong, 2015, pp. 329-332. doi: 10.1109/ISPSD.2015.7123456

[5] D. W. Green and E. M. Sankara Narayanan, "Fully Isolated High Side and Low Side LIGBTs in Junction Isolation Technology," *2006 IEEE International Symposium on Power Semiconductor Devices and IC's*, Naples, 2006, pp. 1-4. doi: 10.1109/ISPSD.2006.1666111

[6] L. Benaissa, N. Rouger, J. Widiez, JC. Crébier, J. Dafonseca, D. Lafond, V. Gaude, K. Vladimirova, "A vertical power device conductive assembly at wafer level using direct bonding technology," *2012 24th International Symposium on Power Semiconductor Devices and ICs*, Bruges, 2012, pp. 77-80.

[7] A. El Khadiry, A. Bourennane and F. Richardeau, "Multiphase Power Converter Integration in Si: Dual-Chip and Ultimate Monolithic Integrations," in *IEEE Transactions on Electron Devices*, vol. 63, no. 5, pp. 1977-1983, May 2016. doi: 10.1109/TED.2016.2537212

[8] B. Yi, Z. Lin and X. Chen, "Snapback-free reverse-conducting IGBT with low turnoff loss," in *Electronics Letters*, vol. 50, no. 9, pp. 703-705, April 24 2014. doi: 10.1049/el.2014.0169

[9] U. Vemulapati, N. Kaminski, D. Silber, L. Storasta and M. Rahimo, "Reverse conducting–IGBTs initial snapback phenomenon and its analytical modelling," in *IET Circuits, Devices & Systems*, vol. 8, no. 3, pp. 168-175, May 2014. doi: 10.1049/iet-cds.2013.0222

[10] T. Yoshida, T. Takahashi, K. Suzuki and M. Tarutani, "The second-generation 600V RC-IGBT with optimized FWD," *2016 28th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*,Prague, 2016, pp. 159-162. doi: 10.1109/ISPSD.2016.7520802

[11] Ryohei Gejo, Tsuneo Ogura, Shinichiro Misu, Yosuke Maeda, Yuma Matsuoka, Norio Yasuhara, Kazutoshi Nakamura, "High switching speed trench diode for 1200V RC-IGBT based on the concept of Schottky Controlled injection (SC)," *2016 28th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, Prague, 2016, pp. 155-158. doi: 10.1109/ISPSD.2016.7520801

[12] M. Rahimo, M. Andenna, L. Storasta, C. Corvasce and A. Kopta, "Demonstration of an enhanced trench Bimode Insulated Gate Transistor ET-BIGT," *2016 28th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, Prague, 2016, pp. 151-154.

[13] Jeffrey P. Gambino, Shawn A. Adderly and John U. Knickerbocker, "An overview of through-silicon-via technology and manufacturing challenges", *Microelectronic Engineering 135 (2015). Volume 135, 5 March 2015, Pages 73–106. https://doi.org/10.1016/j.mee.2014.10.019*

[14] J.-L. Sanchez, E. Scheid, P. Austin, M. Breil, H. Carriere, P. Dubreuil, E. Imbernon, F. Rossel and B. Rousset, "Realization of vertical P^+ walls through-wafer for bi-directional current and voltage power integrated devices," *Power Semiconductor Devices and ICs, 2003. Proceedings ISPSD '03. 2003 IEEE 15th International Symposium on*, 2003, pp. 195-198. doi: 10.1109/ISPSD.2003.1225262

[15] Jongil Won, Jin Gun Koo, Taepok Rhee, Hyung-Seong Oh and Jin Ho Lee, "Reverse-conducting IGBT using MEMS technology on the wafer backside", ETRI Journal Vol. 35, No. 4, Aug. 2013, pp. 603-609 doi : http://dx.doi.org/10.4218/etrij.13.1912.0030

[16] L. Theolier, H. Mahfoz-Kotb, K. Isoird, F. Morancho, S. Assie-Souleille and N. Mauran, "A New Junction Termination Using a Deep Trench Filled With BenzoCycloButene," in *IEEE Electron Device Letters*, vol. 30, no. 6, pp. 687-689, June 2009. doi: 10.1109/LED.2009.2020348

[17] Chanho Park, Jinmyung Kim, Taehoon Kim and D. J. Kim, "Deep trench terminations using ICP RIE for ideal breakdown voltages," *Power Semiconductor Devices and ICs, 2003. Proceedings. ISPSD '03. 2003 IEEE 15th International Symposium on*, 2003, pp. 199-202. doi: 10.1109/ISPSD.2003.1225263

[18] Synopsis, Inc., TCAD Sentaurus, version G-2012.06

[19] A. Bourennane, H. Tahir, J. L. Sanchez, L. Pont, G. Sarrabayrouse and E. Imbernon, "High temperature wafer bonding technique for the realization of a voltage and current bidirectional IGBT," *2011 IEEE 23rd International Symposium on Power Semiconductor Devices and ICs*,SanDiego,CA,2011,pp.140-143.doi: 10.1109/ISPSD.2011.5890810

[20] A. El Khadiry, F. Richardeau, A. Bourennane, D. Zhifeng and M. Breil, "Multi-switch Si-chip structures and on-substrate packaging techniques for improving the electrical performance of power modules," *2013 15th European Conference on Power Electronics and Applications (EPE)*, Lille, 2013, pp. 1-7. doi: 10.1109/EPE.2013.6634426

[21] Szu-Ping Tsai, Heng-Tung Hsu, Che-Yang Chiang, Yung-Yi Tu, Chia-Hua Chang, Ting-En Hsieh, Huan-Chung Wang, Shih-Chien Liu and Edward Yi Chang, "Performance Enhancement of Flip-Chip Packaged AlGaN/GaN HEMTs Using Active-Region Bumps-Induced Piezoelectric Effect," in *IEEE Electron Device Letters*, vol. 35, no. 7, pp. 735-737, July 2014. doi: 10.1109/LED.2014.2324619

[22] U. R. Vemulapati, N. Kaminski, D. Silber, L. Storasta, M. Rahimo, "Analytical Model for the Initial Snapback Phenomenon in RC-IGBTs", ISPS, August 2012, Prague, Czech Republic.

[23] E. Imbernon *et al*., "Flexible technological process for functional integration," *2001 International Semiconductor Conference. CAS 2001 Proceedings (Cat. No.01TH8547)*, Sinaia, 2001, pp. 465-468 vol.2. doi: 10.1109/SMICND.2001.967506

[24] A. Lale, N. Videau, A. Bourennane, F. Richardeau and S. Charlot, "Mixed monolithic-hybrid integration of multiphase power converter : Preliminary evaluation of the 3-chip integration concept", 2016 International Conference on Electrical Systems for Aircraft, Railway, Ship Propulsion and Road Vehicles & International Transportation Electrification Conference (ESARS-ITEC), Toulouse, pp. 1-7. doi: 10.1109/ESARS-ITEC. 2016.7841426

[25] A.EL Khadiry, F.Richardeau, A.Bourennane, D.Zhifeng, M.Breil, " Multi-switch Si-chip structures and on-substrate packaging techniques for improving the electrical performance of power modules", European Conference on Power Electronics and Applications (EPE) 2013, Lille.

[26] T. Yanagi *et al*., "Circuit simulation of a silicon-carbide MOSFET considering the effect of the parasitic elements on circuit boards by using S-parameters," *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*, San Antonio, TX, 2018, pp. 2875-2878. doi: 10.1109/APEC.2018.8341425.

[27] N. Mohan, T.M. Undeland, W.P. Robbins, "Power Electronics - Converters, applications et design,", 3rd ed., John Wiley & Sons, ISBN-10: 9780471226932, ISBN-13: 978-0471226932, 2002.