New prospects on high on-current and steep subthreshold slope for innovative Tunnel FET architectures

C. Diaz Llorente, J.-P. Colinge, S. Martinie, S. Cristoloveanu, J. Wan, C. Le Royer, G. Ghibaudo, M. Vinet

Version of Record: https://www.sciencedirect.com/science/article/pii/S0038110119301571
Manuscript_9dacf72d4e37d86fa584c6919eed170d

New prospects on high on-current and steep subthreshold slope for innovative Tunnel FET architectures

C. Diaz Llorente[1], J-P Colinge[1], S. Martinie[1], S. Cristoloveanu[2], J. Wan[3], C. Le Royer[1], G. Ghibaudo[2], and M. Vinet[1]

[1] Université Grenoble Alpes, CEA, LETI, 38000 Grenoble, France
carlos.diazllorente@cea.fr
[2] IMEP-LAHC, INP-Grenoble, MINATEC, 38016 Grenoble, France
[3] Fudan University, Shanghai, China

Abstract

We propose three innovative SOI Tunnel FET architectures to solve the recurrent issue of low I_{ON} and degraded subthreshold slope measured on TFETs. These are evaluated and compared with a standard TFET structure (with lateral tunneling) using the Sentaurus TCAD tool. Extending the source (anode) at the bottom of the body region generates vertical band-to-band tunneling. Moreover, reducing the vertical distance between the extension and the gate oxide (L_{rt}) yields a very steep slope and higher I_{ON} compared to a device with only lateral tunneling, but only for gate lengths longer than 100 nm. Using an ultrahigh boron dopant concentration (10^{21} cm^{-3}) thin layer at the bottom for extremely small body thickness (T_{Si} < 7 nm), increases I_{ON} even for small gate lengths (L_G < 100 nm). The implementation of an embedded tip in the source enhances the maximum electric field at the source/channel junction, but the impact on the performance is limited because the tunneling area is not increased. Therefore, this architecture provides a performance similar to a standard TFET. TCAD simulations using SiGe with different germanium concentrations (30% and 50%) and pure germanium, instead of silicon, show an increase of the interband tunneling current when using an ultrahigh dopant concentration thin boron layer for small gate lengths (L_G < 50 nm). The reduction of the tunneling current using a relatively thick channel (11 nm – 7 nm) can be compensated by using a higher germanium concentration to reduce the energy bandgap. However, this will increase the density of defects causing a TAT tunneling instead of interband tunneling, jeopardizing the possibility of achieving a subthreshold swing below 60 mV/dec.

Keywords: Tunnel FET, TFET, SOI, tunneling, BTBT, Extended-Source, Pure Boron, Sharp Tip.

1. Introduction

During the last decade state-of-the-art microprocessors have experienced a change of paradigm with respect to the design rules. Currently, delivering the highest performance possible is longer always the major concern, and one often requires a computation efficiency which means the maximum performance at the lowest possible power consumption. This is consequence of the industrial needs for low power consumption in battery-operated handheld devices. The most effective path for decreasing of power consumption in integrated circuits is the reduction of bias supply to minimize the switching energy (~CV_{DD}^2) [1], while maintaining a very low off-current to avoid the static power consumption degradation (~$I_{OFF}V_{DD}$). However, lowering V_{DD} without decreasing the threshold voltage (V_{TH}) will severely degrade the operating frequency (~ $(V_{DD}-V_{TH})^2$). In CMOS technology, geometric scaling still provides a higher performance, lower power consumption and a lower cost per transistor. However, in the recent years, V_{DD} scaling has become quite difficult because the V_{TH} reduction severely increases leakage current [2] such that supply voltage scaling below 0.8 V has become very difficult [3]. Low subthreshold swing (SS) values, low I_{OFF} current and high I_{ON}/I_{OFF} ratio are crucial for ultra-low power applications (V_{DD} < 0.4 V) [4]. Unfortunately, in CMOS technology SS cannot be reduced below 60 mV/dec at room temperature (300 K) because it is limited by the thermionic emission of carriers from source to drain which contains a (kT/q) term and, as a result, I_{OFF} increases if low threshold voltages are used [5]. Because of this fundamental limit of MOSFETs the need for developing new concepts such as steep slope devices has arisen in the recent years [6].

Standard tunnel FETs (TFETs) are p-i-n gated diodes [7]–[9] based on a different carrier injection mechanism than CMOS devices. TFETs rely on band-to-band tunneling (BTBT) [10], [11] enabling very low off-current and have the theoretical capability of achieving a SS lower than 60 mV/dec (at 300K) [12]. These characteristics make the TFET a promising candidate for ultra-low power applications. The current in a TFET is determined by the tunneling probability given by the Wentzel-Kramers-Brillouin (WKB) approximation [13]. In theory, this probability can reach values close to unity if a narrow tunneling length, a small carrier effective mass and a small energy bandgap are used [14], [15]. In practice it has been proven extraordinarily difficult to simultaneously achieve a steep slope and a high I_{ON} current, regardless of the materials [16]–[21], architectures [22]–[24] or specific fabrication steps [25]–[27] employed to increase the tunneling probability [28]. In the best cases, a SS below 60 mV/dec has only been obtained for a narrow range of current values in all-silicon Tunnel FETs [29], [30], but with very modest current drive. The benchmarking of novel CMOS devices based on charge switching (TFETs, IMOS, NEMS, Negative capacitance FET or 2D material FET) [31], show that tunneling

devices have lower switching energy than high-performance CMOS, although the delay is larger. In addition, TFETs exhibit a standby power ranging between non-tunneling electronic and spintronic devices. These analyses indicate that the Tunnel FET can be considered a good candidate to CMOS replacement for ultra-low power applications.

1.1. Standard Tunnel FET: lateral tunneling

The TFET is a reverse-biased gated PIN diode (Figure 1a). The systematic measurements carried out in our fabricated TFETs have shown a small drain current ($5.7 \cdot 10^{-2}$ µA/µm) and a degraded SS of ~160 mV/dec over 3 decades of current [32]. The simulation of a p-i-n gated diode with the same geometric dimensions that our measured TFETs (Figure 1a), shows that the BTBT generation is located at the source/channel junction below the front gate (Figure 1b) and that it is independent of the gate length, which explains why standard TFETs exhibit such a low tunneling current.

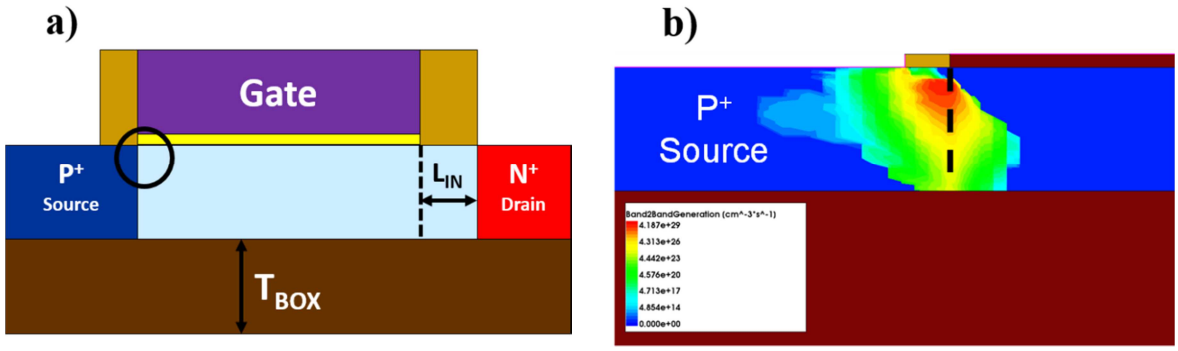

Figure 1. (a) Standard reference N-TFET structure simulated with TCAD Sypnosys. (b) Magnified view of the BTBT generation region indicating that in a lateral TFET (L_G = 500 nm and T_{Si} = 11 nm), the tunneling occurs in the source/channel junction below the front gate with V_G = 2.4 V and V_D = 0.9 V.

In order to increase the tunneling current it is necessary to enlarge the generation area where tunneling takes place. New disruptive approaches on TFETs architectures such as vertical nanowires using III-V compound materials have been recently fabricated [33] with promising results for I_{ON} current and SS below 60 mV/dec. Nevertheless, these types of solutions based on new BTBT materials and architectures are challenging because transferring them onto a silicon platform is not straightforward [20].

2. Proposed TFET architectures

Here simulations have been used to assess the performance of innovative planar TFET architectures with different source junction architectures designed to increase the tunneling generation area. The aim is to determine which solution provides best performance (Extended-Source TFET, Pure Boron TFET or Sharp Tip TFET), while staying compatible with a silicon platform and the enabling co-integration with CMOS

technology. We have performed 2D TCAD simulations of silicon Tunnel FETs using the Nonlocal Path Band-to-Band model of the Sypnosys tool with default tunneling parameters and coupled to classical Drift-Diffusion equation with constant mobility [34]. The standard TFET from Figure 1a serves as a reference to compare the results of the proposed architectures. The parameters common to all devices are: gate length L_G from 500 nm down to 15 nm, T_{BOX} = 145 nm, EOT = 1.18 nm, intrinsic body length L_{IN} = 20 nm near the drain region to suppress ambipolar effects [35], a gate work function Φ_{gate} = 4.0 eV and a dopant concentration in source and drain of $N_D = N_A = 10^{20}$ cm^{-3}. Since the simulations performed in this work are aimed at evaluating the relative performance of proof-of-concept TFET architectures and explore first-order impact of device structure on tunneling characteristics, quantum effects such as subband formation and variation of bandgap energy in thin-film devices have been neglected. Because such effects are known to arise in silicon films thinner than 5nm, they should be included in further simulations of ultrathin devices. The possible tunneling through thin gate oxides has been neglected as well since the EOT of 1.18 nm can in practice be achieved by using a high-k dielectric significantly thicker than the EOT.

2.1. Extended-Source TFET

The extension of the source doping into the channel region is an interesting solution to increase the tunneling area. When the source is extended (Figure 2a) and an inversion layer is created at the channel top (in on-state), an effective vertical p-i-n structure is formed in the whole gate region. This is confirmed by the BTBT generation mapping shown in Figure 2b, where two tunneling components can be seen. One is located at the source/channel junction (the lateral tunneling component), and the other one is located along the extension of the source at the bottom body ($N_{ext} = N_A$). The latter component significantly increases the BTBT generation area and thus the drain current. As a result, the Extended-Source TFET (ES-TFET) presents a higher tunneling area and current than the standard TFET.

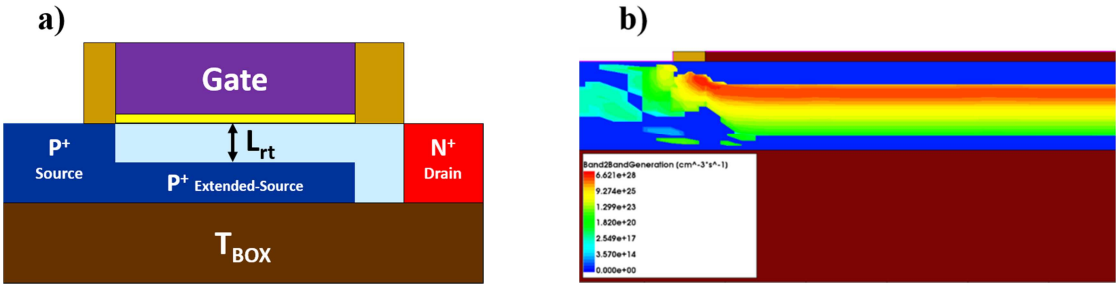

Figure 2. (a) Schematic of an Extended-Source N-TFET architecture (T_{si} = 11 nm, L_{rt} =3 nm and L_G = 500 nm) with tunneling parallel to the gate electric field. (b) BTBT generation showing the presence of vertical BTBT above the extension of the source into the channel region (with V_G = 2.4 V and V_D = 0.9 V).

The idea of source extension has already been demonstrated in different studies. For example, Y. Morita *et al.*, [36] have fabricated a Tunnel FinFET with an ultrathin epitaxial channel on silicon CMOS platform. The FZ Jülich laboratory has implemented some boosters in planar TFET architectures such as a counter-doped pocket in the source junction to enable vertical BTBT aligned with the gate electric field in an enlarged area. In addition, a selective and self-aligned silicidation process was used to enhance the on current [37]. In both cases the objective was focused on making vertical tunneling the main contribution to the drain current.

Our ES-TFET architecture features two main differences with respect to the previous fabricated Tunnel FETs. Firstly, the source junction extends in the channel region underneath the whole front gate, thereby enlarging the tunneling area. Moreover, the implementation of the intrinsic region (L_{IN}) minimizes the non-desired BTBT in the drain region and other possible parasitic effects. Secondly, the tunneling can be modulated by changing the thickness of the silicon film, which determines the contribution of the vertical BTBT and modifies the vertical distance between the source extension and the gate oxide (given by the restricted tunneling length L_{rt}). A small L_{rt} distance means a thin channel region, which translates into a more efficient band bending by the gate terminal and a smaller tunneling length and thus, a larger drain current. On the contrary, a large L_{rt} implies a higher tunneling length, and therefore a lower tunneling current.

2.2. Pure Boron TFET

The Pure Boron TFET (PB-TFET) architecture appears as an evolution of the Extended-Source TFET because it fulfills the requirement of obtaining a SS lower than 60 mV/dec (theoretically) when using extremely thin channels (T_{Si} < 10 nm). Note that, the fabrication of an ES-TFET with a heavily doped extended region that is only a few nanometers thick is not feasible using an implantation process because the generated defects will completely degrade the steepness in the subthreshold region.

The PB-TFET is schematically shown in Figure 3. Like the ES-TFET it features an extension of the source into the channel region, this time by means of an ultrahigh dopant concentration in a thin bottom epitaxial layer. We have performed the simulations with a heavily doped 1 nm thick pure boron layer for different doping concentration ($N_A = 10^{20}$ cm^{-3} and 10^{21} cm^{-3}) located at the bottom. This configuration enables the simultaneous presence of electrons and holes in the channel in the very thin SOI layer in order to increase the on-current. This heavily doped layer avoids the supercoupling effect [38], [39] which prevents the formation of electrons and holes bilayers in ultrathin silicon films (T_{Si} < 11 nm), because a high concentration of holes is achieved by actual doping and not by field effect. Although this study is based only on TCAD simulations, pure boron technology is already demonstrated, so it would be possible to fabricate Tunnel FETs with a similar architecture. For the sake

of simplicity, the simulations have neglected the effects of high doping concentrations on the distribution of density of states in the semiconductor. Further studies should, however, include the effects of bandgap narrowing and the formation of band tails inside the bandgap, which might affect the tunnel characteristics and degrade the subthreshold slope.

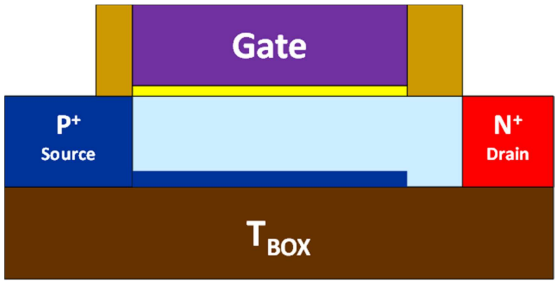

Figure 3. Schematic architecture of a Pure Boron TFET (PB-TFET) in N-mode configuration. An ultra-heavily doped 1 nm boron layer is implemented at the bottom body to generate an enhanced vertical BTBT.

L.K. Nanver *et al.*, have demonstrated the feasibility to fabricate Pure-Boron thin-film layers deposited by Chemical Vapor Deposition (CVD), which present electrical and processing properties that are very interesting for device integration [40]. In particular, it is important to highlight that this fabrication technology allows for the formation of shallow junctions in p^+-n diodes [40]

An important property of this technology is that the boron layer can act as an abundant source of boron dopants for ultra-shallow junctions. Besides, this high doping concentration is achieved because of the interface conditions between the boron layer and the crystalline silicon and not due to the doping of the bulk silicon. When the monolayer of acceptor states is created and filled with electrons at the interface, a fixed negative charge is created [41]. This negative charge attracts about $5 \cdot 10^{14}$ cm^{-2} surface density of holes, which behave just like a p-doped layer with respect to the hole injection from the p-region into the n-layer and electron injection from the n-layer into the p-layer. The boron doping concentrations, confirms that is possible to get the equivalent of about 10^{22} cm^{-3} in a couple of nanometers thick layer [42]. After the α-Boron layer removal there is a boron concentration left of 10^{14} cm^{-2}, which is equivalent to a boron peak concentration around 10^{21} cm^{-3}.

For Pure Boron TFET architecture it is most interesting deposit the boron layer at 400°C, because there is no boron impurity doping of the bulk silicon (at 700°C the boron can diffuse a few nanometers into the bulk silicon, doping it to values of $2 \cdot 10^{19}$ cm^{-3} [42]). Moreover, activating the boron with higher temperature steps is counterproductive because the annealing will finally destroy the attractive interface properties and the bulk doping is limited by the solid solubility, so it will not be possible to reach the required high doping levels. Therefore, the possibilities for fabricating PB-TFETs will depend on the thermal budget of post-boron deposition

steps and the possibilities for performing the deposition. Finally, there will be also boundary conditions not described here in order to achieve a successful deposition.

2.3. Sharp Tip TFET

The last innovating architecture is the Sharp Tip TFET (Tip-TFET), which is schematically represented in Figure 4. The idea behind this device configuration is to implement a sharp tip at the source junction to enhance the electric field. BTBT generation rate and tunneling current, given by Kane's equation [43], is proportional to the electric field. Therefore, if the electric field is increased the drive current should be enhanced as well.

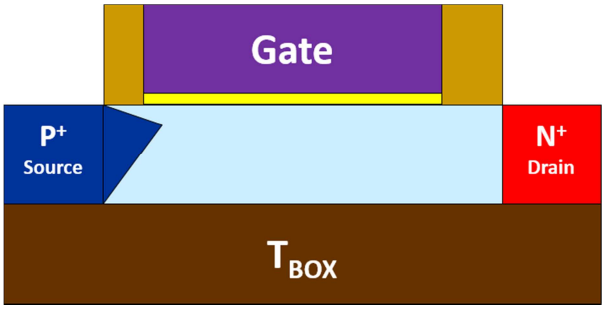

Figure 4. Schematic architecture of a Sharp Tip TFET in N-mode configuration used to enhance the electric field at the source junction.

The purpose of this architecture is to determine the possibility of taking advantage of an embedded raised source and drain process with a sharp source junction tip. Intel's trigate CMOS transistors were the first to demonstrate these embedded structures for the 45 nm technology node with high-k metal gate dielectric [44]. This process innovation was initially developed for strained PMOS transistors to increase the hole mobility and thus performance. Here, our aim is to increase the electric field at the source junction and therefore increase the tunneling current. 32 nm logic technology also includes these embedded SiGe regions, but they are closer to the channel region to increase the channel strain [45]. It is important to highlight that two technological parameters will drive the enhancement of the tunneling current: firstly, the proximity of the embedded tip source and drain areas to the channel region and secondly, the position of the peak with respect to the front gate.

3. Extended-Source TFET architecture

3.1. Impact of the restricted tunneling length (L_{rt}) for a given T_{Si}

Figure 5 shows the $I_D(V_G)$ curves for different L_{rt} distances ranging from L_{rt} = 3 nm to L_{rt} = 10 nm, with a silicon body thickness of 11 nm. The ES-TFET exhibits a higher on-current and a steeper slope for small vertical distances between the extension and the gate oxide (L_{rt} =3 nm, blue line). As long as the distance of the L_{rt} region is larger, the front gate terminal starts to lose the electrostatic control of the vertical BTBT. In addition,

the drain current begins to decrease due to the increase of the tunneling distance, causing a severe degradation of the slope in the subthreshold region. Good performance is maintained until L_{rt} = 7 nm (purple line), but for larger undoped regions the tunneling distance becomes too large. A larger L_{rt} creates a lower electric field and thus a small band bending. Figure 5 also confirms that Tunnel FETs require a very thin body and explains why it is not possible to obtain an SS below 60 mV/dec for channel thickness in the range of 10-11 nm for a standard TFET [46].

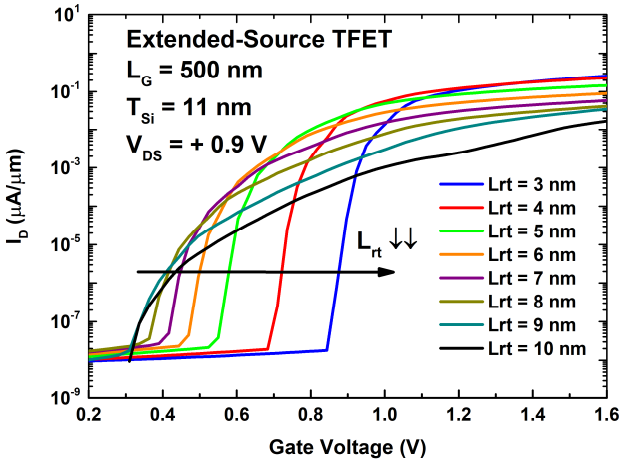

Figure 5. $I_D(V_{GS})$ curves of ES-TFET for a 11 nm silicon body thickness and different extension depths (L_{rt}) with respect to the gate.

One of the drawbacks of ES-TFET is related with the degradation of the threshold voltage, as long as the P^+ extension of the source occupies the majority of the channel region. In this case the channel is at a lower potential than in a fully undoped channel region (as in a standard TFET), so it will be necessary to apply a higher front gate voltage to create an inversion layer at the channel top. Even though we are using a gate work function of 4.0 eV instead of 4.61 eV (which provides an extra electrostatic control of 0.61 V and thus a reduction of the threshold voltage), the threshold voltage is higher than 0.8 V for L_{rt} = 3 nm, which is not suitable for ultra-low power applications (V_{DD} < 0.4 V). Using simulation it is possible to lower the value of the work function parameter to reduce the threshold voltage. However, for a real process fabrication, gate materials with work functions lower than 4.0 eV such as potassium (3.0 eV), calcium (2.87 eV) or even cesium (1.95 eV) are unpractical in N-TFET devices. On the other hand, for P-TFETs it is possible to find useful gate metals with a high work function, such as platinum (5.63 eV) that at least in theory can work with a lower bias supply. For L_{rt} = 5 nm there is a trade-off between a low threshold voltage (~ 0.5 V) and a high on-current, although slightly lower compared to L_{rt} = 3 nm, without changing the gate work function.

3.2. Impact of T_{Si} for a given restricted tunneling length (L_{rt})

Previously we have obtained the best performance for T_{Si} =11nm and the smallest possible extension depth (L_{rt} = 3nm). Figure 6a shows the $I_D(V_G)$ curves at a given L_{rt} = 3 nm and different silicon thicknesses. Thinning down the T_{Si} from 11 nm to 4 nm, we observe that there is a progressive enhancement of the on-current and the best case occurs for T_{Si} = 6 nm. This is associated with a better electrostatic control and a more efficient band bending for a narrow body thickness. However, for T_{Si} = 4 nm a degradation of the on-current and the subthreshold slope can be noticed. This is most likely due to the fact that each time that the body thickness is reduced, as L_{rt} is fixed to 3 nm, the extended source is thinner, and therefore more resistive minimizing the on-current.

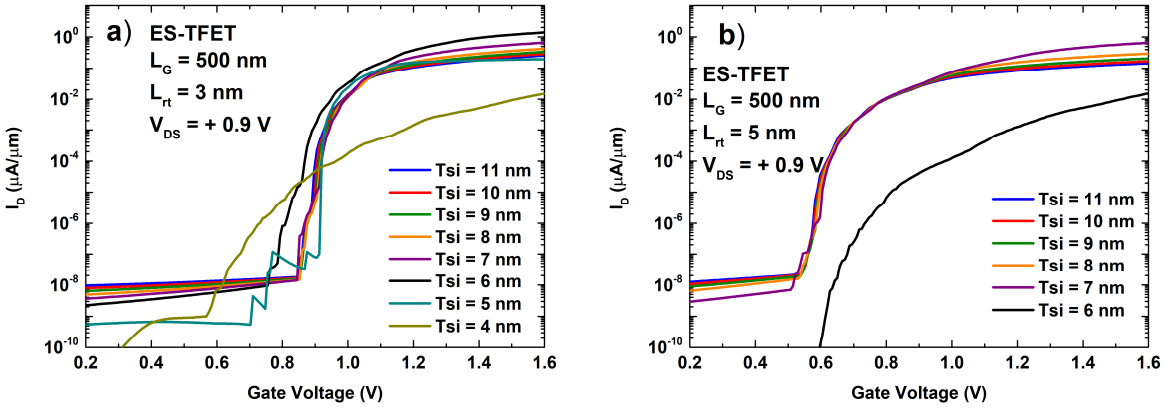

Figure 6. $I_D(V_{GS})$ curves of ES-TFET with L_G = 500 nm and different silicon body thickness for a given extension depth: (a) L_{rt} =3 nm and (b) L_{rt} = 5 nm.

Figure 6b shows the $I_D(V_G)$ curves in this case for an extension depth of 5 nm (trade-off case from Figure 5). The best on-current is obtained for a silicon body thickness of 7 nm, while for T_{Si} = 6 nm a clear degradation of the on-current and subthreshold slope is observed. In both cases the degradation occurs when the thickness of the extended source is only 1 nm.

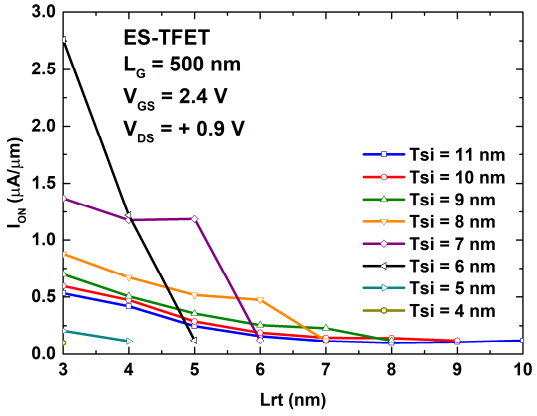

Figure 7. On-current versus extension depth (L_{rt}) for different silicon thickness of ES-TFET architecture with L_G = 500 nm.

For a better understanding of the ES-TFET operation regarding the tunneling length (L_{rt}), Figure 7 shows the on-current at V_{GS} = 2.4 V obtained for different L_{rt} values with the variation of the silicon body thickness. A general trend is observed in all the cases: when L_{rt} is decreased the on-current increases, owing to a shortening of the tunneling length. Regardless of the simulated thickness the highest on-current is always obtained for the smallest vertical distance possible between the extension and the gate oxide (L_{rt} = 3 nm). The most optimized ES-TFET architecture is for a film thickness of 6 nm, while for T_{Si} = 5 nm and 4 nm the on-current is degraded. Other simulation results (not shown in Figure 7) suggest that an extremely thin body thickness (T_{Si} < 6 nm) requires an L_{rt} lower than 3 nm to enhance the tunneling current. Nevertheless, the fabrication of this extended-source architecture with enough quality and accuracy is not feasible nowadays by means of an implantation process.

3.3. Comparison of Extended-Source TFET with Standard TFET

The comparison of the ES-TFET architecture with an 11 nm body thickness and an extension depth L_{rt} = 3 nm with respect to the standard Tunnel FET (Figure 8a), clearly establishes how the ES-TFET outperforms the standard architecture for a long gate length (L_G = 500 nm). The higher on-current is due to the fact that the vertical BTBT occurs in the whole source extension, while in the standard TFET it is localized at the source/channel junction. The steeper subthreshold slope is a consequence of the restricted tunneling path length (3 nm) owing to the extended source in the channel region, which significantly improves the electrostatic control compared to the standard TFET. The SS extractions in Figure 8b confirm that ES-TFET achieves SS below 60 mV/dec over 4-5 decades of current. For comparison, in the standard TFET the SS is degraded (~ 75 mV/dec) even at extremely low values of drain current.

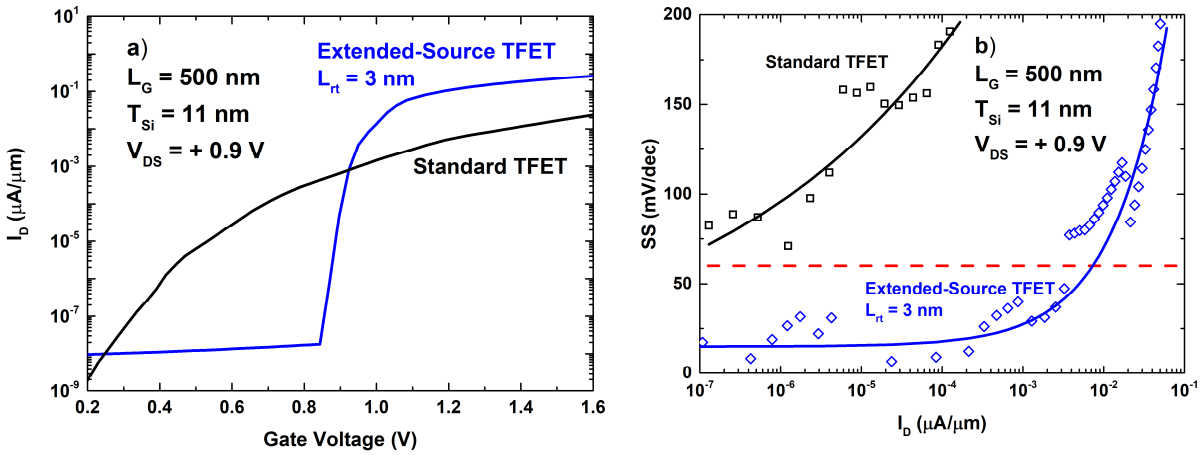

Figure 8. Comparison of: a) $I_D(V_G)$ curves and b) figure of merit $SS(I_D)$ for standard and ES-TFET.

The next section presents a thorough study to determine the impact of the gate length on the total tunneling current drive.

3.4. Impact of gate length on drive current

Another confirmation of the independence of the current on gate length in a standard TFET is provided in Figure 9. In an ES-TFET, however, the magnitude of the on-current depends on the length of the extension of the source into the body. Therefore, if the gate length is reduced (L_G < 100 nm) the current will be degraded because the tunneling area will be reduced (as shown in Figure 9). A detailed analysis of the simulation results indicates that for long channel distances we obtain an on-current that outperforms the standard TFET by a factor of 3x in the best case where L_{rt} = 3 nm. If the extension depth L_{rt} is increased the tunneling current decreases, but current drive remains high until L_{rt} = 5 nm. For gate lengths below 50 nm the benefit of the vertical BTBT disappears because of the reduction of the BTBT generation area and the standard TFET shows better on-current values.

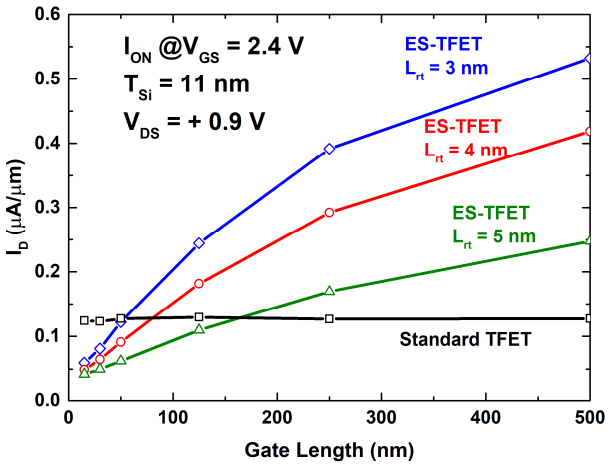

Figure 9. $I_{ON}(L_G)$ for standard and ES-TFET architecture. The standard TFET achieves better I_{ON} for small gate lengths (< 100 nm).

The reduction of body thickness improves the electrostatic control for the ES-TFET architecture and enhances the on-current. For long channel devices with T_{Si} = 8 nm (Figure 10a), the on-current outperforms the standard TFET by a factor of 7x and the benefits of vertical BTBT are extended for L_G down to 30 nm. For T_{Si} = 6 nm (Figure 10b) vertical BTBT dominates even for extremely short gate lengths (L_G < 30 nm).

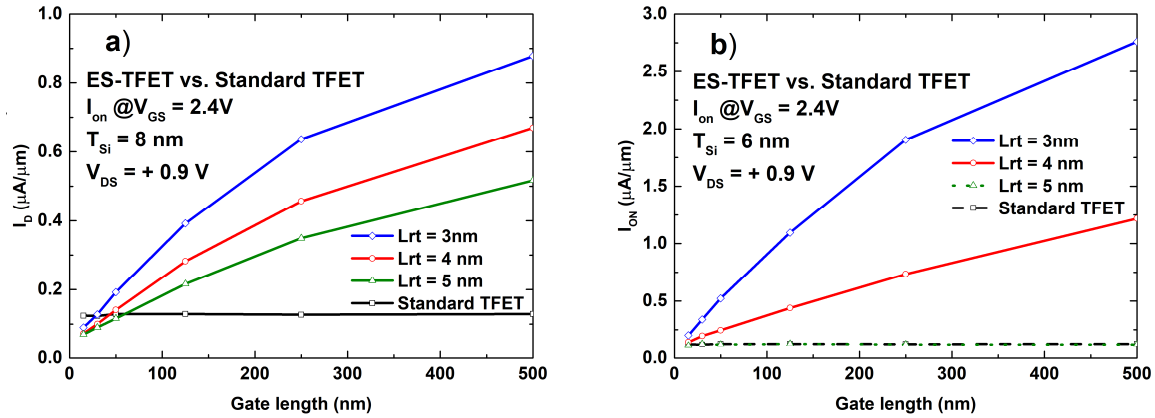

Figure 10. $I_{ON}(L_G)$ for standard and ES-TFET with different thickness. (a) T_{Si} = 8 nm: the benefits of vertical BTBT are extended down to 30 nm, (b) T_{Si} = 6 nm: vertical BTBT dominates even for very short gate lengths.

4. Pure Boron TFET architecture

4.1. Impact of silicon body thickness

The Pure Boron TFET (PB-TFET) with a doping of 10^{20} cm^{-3} in the thin bottom layer (Figure 11) shows a complex trend when the silicon body thickness is thinned down from 11 nm to 4 nm. At first there is a progressive sharpening of the slope when reducing T_{Si} down to 7 nm, and from that point on, further thinning the SOI layer degrades the subthreshold slope. An enhancement of the drain current for medium gate voltages (up to 1.0 V) is noticeable for intermediate values of T_{Si} and a significant degradation is observed for very thin values (from 6 nm to 4 nm). However, at high gate voltages the tunneling current converges to a single low value regardless of the body thickness. These non-conclusive simulation results are not in line with the prospects of a steeper slope for TFETs with a body thinner than 10 nm. They suggest that a higher doping concentration in the thin bottom layer is required in order to achieve the expected results when using extremely small body thickness.

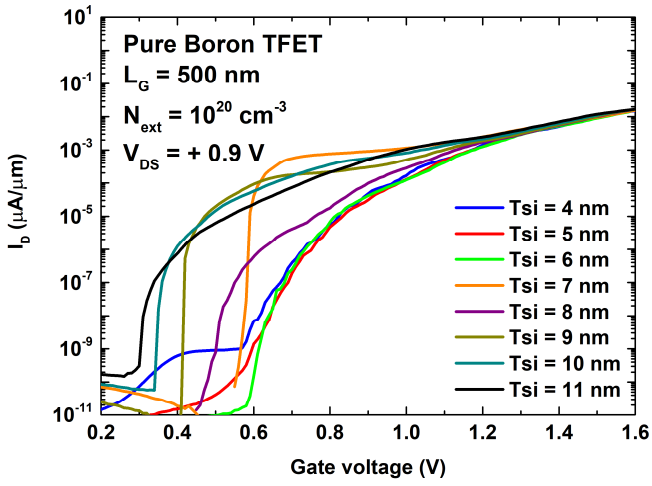

Figure 11. $I_D(V_G)$ curves of PB-TFET architecture with variable body thickness and a Pure Boron doping of 10^{20} cm^{-3} in the thin bottom layer.

Repeating the simulations with an ultrahigh doping concentration of 10^{21} cm^{-3} in the thin bottom layer, the PB-TFET shows an improved electrostatic control for narrow channels (T_{Si} < 7 nm). There is an outstanding performance for T_{Si} = 4 nm (solid blue line) in Figure 12 with a 10-fold I_{ON} increase with respect to the ES-TFET with L_{rt} = 3 nm. When increasing the body thickness it is possible to maintain good transfer characteristics until T_{Si} = 6 nm is reached. For thicker channels the performance begins to be significantly degraded due to the larger tunneling distance, which results in a reduction of the interband tunneling probability (less BTBT current) and a less efficient electrostatic control by the front gate with the degradation of the subthreshold slope.

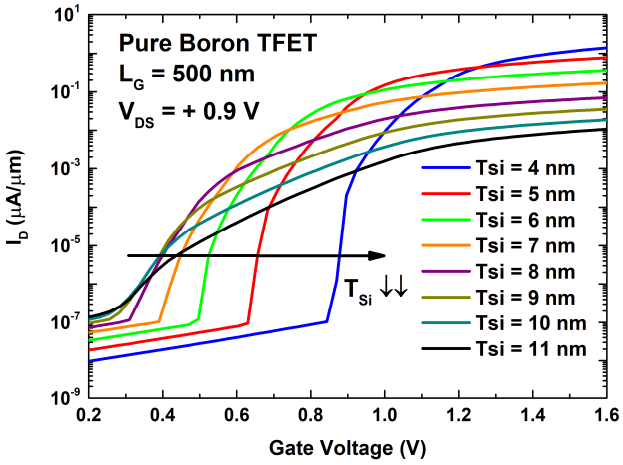

Figure 12. $I_D(V_G)$ curves of PB-TFET architecture for long gate devices (500 nm), different silicon thickness, and a ultrahigh doping concentration of 10^{21} cm^{-3} in the thin bottom layer.

Like the ES-TFET, the PB-TFETs also shows an increase in V_{TH} when body thickness is decreased owing to the ultrahigh P-type doping concentration at the bottom of the channel region. Consequently, it is necessary to apply a higher front gate voltage to create an inversion layer at the top of the channel. The shift in threshold voltage $\Delta V_{TH}/\Delta T_{Si}$ can reach 0.2 V per nanometer.

4.2. Comparison of Pure Boron TFET with Standard TFET

The implementation of a ultrahigh doping concentration of 10^{21} cm^{-3} in thin bottom layer of the PB-TFET improves I_{ON} by more than two orders of magnitude compared to the standard TFET architecture (Figure 13a). However, the main challenge of the PB-TFET is the degradation of V_{TH}, compromising its use for ultra-low power applications. SS reaches values below 60 mV/dec over 4 decades of current (Figure 13b), while for the standard TFET, SS is higher than 60 mV/dec in all the current ranges. The problem is to determine how far is possible to extend this gain in performance in devices with very short gate length, where the tunneling area for the vertical BTBT is constricted.

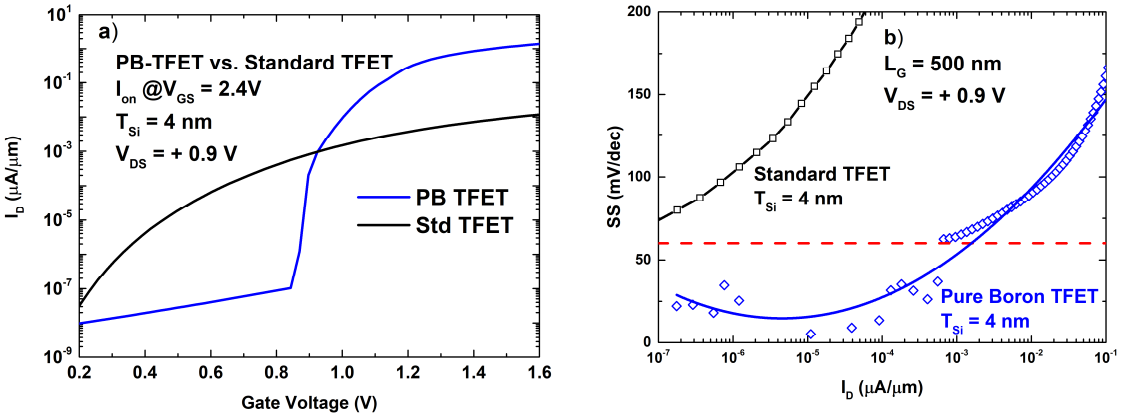

Figure 13. (a) $I_D(V_G)$ curves of PB-TFET and standard TFET architectures with long channel (500 nm) and ultrathin film (T_{Si} = 4 nm). (b) Subthreshold swing versus drain current for standard and PB-TFETs.

4.3. Impact of gate length on drive current

Figure 14a confirms that a heavily doped boron layer combined with an extremely thin body (4 nm, 5 nm and 6 nm) significantly enhances the vertical BTBT for long gate lengths with respect to the standard TFET with T_{Si} = 4 nm. The benefits of Pure boron technology are maximized for extremely narrow channels (T_{Si} = 4 nm). When thickness is increased there is a degradation in performance because the ultrahigh doped layer is further away from the gate and the band bending is not so well controlled. The problem arises when devices are made with shorter gates and the tunneling surface in the channel region is shrunk. Thus, when the gate length is decreased, the tunneling current decreases as well (Figure 14a). However, unlike the ES-TFET, the PB-TFET has better performance than the reference device, even for short gate lengths (L_G < 100 nm). This indicates that it could be a feasible option to obtain a steep slope and a high I_{ON} simultaneously in a future fabrication process. This demands a very small body thickness and from Figure 14a one can see that for T_{Si} thicker than 6 nm it will not be possible to extend the gain of the vertical BTBT for extremely small gate lengths.

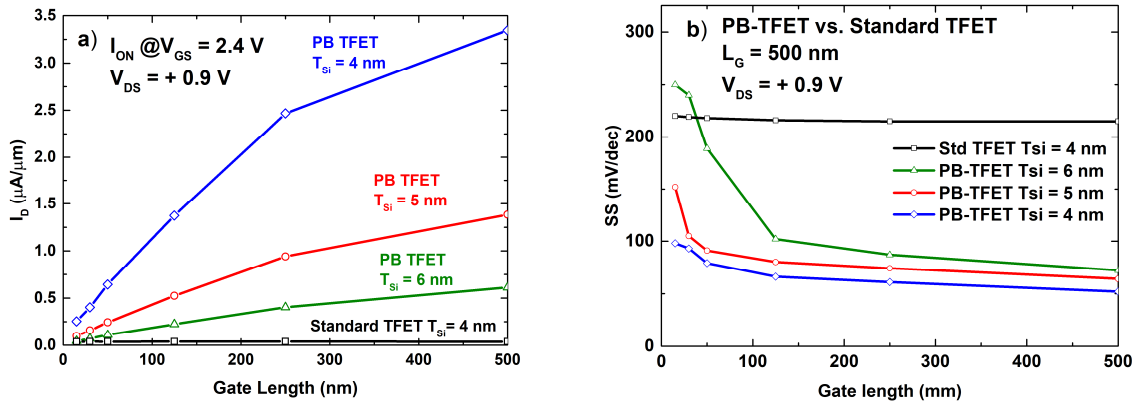

Figure 14. (a) I_{ON} (L_G) for standard and PB-TFET architectures for different T_{Si} values. (b) SS versus drain current for standard TFET (I_D range: 10^{-6} – 10^{-3} μA/μm) and PB-TFETs (I_D range: 10^{-5} – 10^{-2} μA/μm).

The SS extractions as a function of the gate length (Figure 14b) show in the PB-TFET architecture a SS degradation with the reduction of L_G. For PB-TFET with T_{Si} = 4 nm even at short gate lengths (L_G < 100 nm) the SS is beyond 60 mV/dec, but limited to 100 mV/dec (for L_G = 15 nm). However, when increasing the body thickness (5 nm and 6 nm) the electrostatic control is lower and causes a severe increase of the SS still at medium gate lengths. In the standard TFET with T_{Si} = 4 nm, the SS is completely degraded and almost the same values are obtained (~ 215 mV/dec) regardless of the gate length and even with a lower I_D range (from 10^{-6} to 10^{-3} µA/µm) in comparison to PB-TFET (from 10^{-5} to 10^{-2} µA/µm). When lateral tunneling is involved decent SS values are only obtained for very low range current (< 10^{-8} µA/µm).

5. Sharp Tip TFET architecture

5.1. Impact of the silicon body thickness

The comparison of the Sharp Tip TFET architecture (Tip-TFET) for different body thicknesses with respect to the standard TFET (Tsi = 4 nm) in Figure 15a, verifies that the design of a sharp tip in the source junction has no significant impact in I_{ON} (which is only slightly higher than for the standard TFET). The SS follows the same trend in both architectures and it is only better for Tip-TFET for a very low range of drain current (Figure 15b). Besides, in this architecture the location of the tip regarding to the front gate and the extension into the channel region are main parameters. Thus, for a given body thickness the right combination of these parameters must be achieved to maximize I_{ON}. However, for this TCAD study and for the sake of simplicity we have used the same tip parameters regardless of the thickness of the body region.

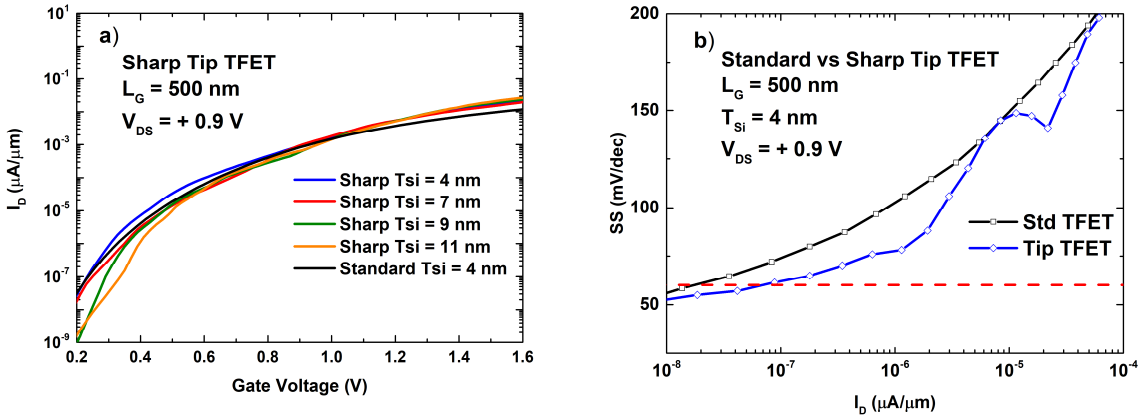

Figure 15. (a) $I_D(V_G)$ curves of Tip-TFET for different body thickness compared with standard TFET (T_{Si} = 4 nm). (b) SS versus drain current for Tip-TFET and standard TFET (T_{Si} = 4 nm).

The 2D mapping of the electric field (Figure 16a) and the BTBT generation rate (Figure 16b) show that the tip causes a shift in the position of the maximum electric field. The BTBT rate is improved only where the overlap of this field and the P^+ region takes place. It was thought that this enhanced electric field would break a

great number of covalent bonds on the P^+ region, enabling more electrons to participate in the interband tunneling process from the valence band of the P^+ region to the conduction band of the channel region. However, results from Figure 15a show that the benefit of this tip junction is marginal. Despite the fact that the electric field is increased the tunneling area is not magnified, explaining why the current is not significantly increased as it is for the ES-TFET and PB-TFET architectures.

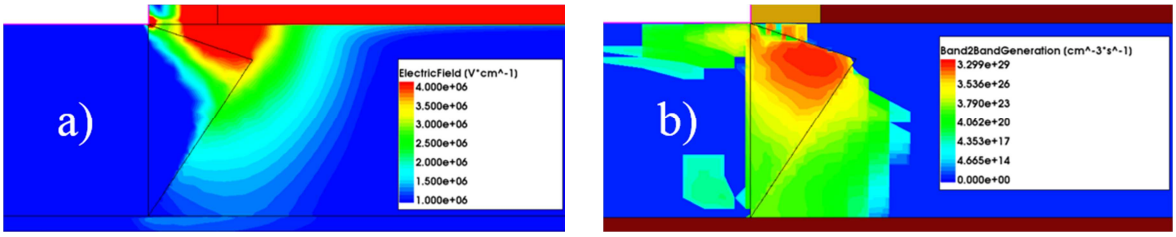

Figure 16. 2D mapping of Sharp Tip-TFET with T_{Si} = 11 nm and a gate length of 500 nm: (a) Maximum electric field and (b) BTBT generation. In both cases applied polarization is V_G = 2.4 V and V_D = 0.9 V.

5.2. Impact of gate length on drive current

From the 2D mapping of the BTBT generation in Figure 16b it is confirmed that the Tip-TFET architecture produces only lateral BTBT and not vertical BTBT. This is definitely verified in Figure 17, which illustrates I_{ON} for different gate lengths. The Tip-TFET presents the same behavior as the standard TFET, indicating that the current is independent on gate length. For a particular body thickness (T_{Si} = 4 nm), the Tip-TFET shows a slightly increase of I_{ON} in comparison to the standard TFET due to the presence of the embedded tip source. However, for both architectures the tunneling current is considerably smaller than in the ES-TFET and the PB-TFET for long gate devices (L_G > 100 nm) and in the same range for short gate devices (L_G < 100 nm). The Tip-TFET exhibits an increase of I_{ON} for larger channel thicknesses, which is related with the electric field peak position (in all the cases 2 nm below the front gate). This set up seems to maximize I_{ON} for a body thickness of 11 nm, but for T_{Si} = 4 nm it is necessary to locate the peak closer to the gate, otherwise I_{ON} is reduced.

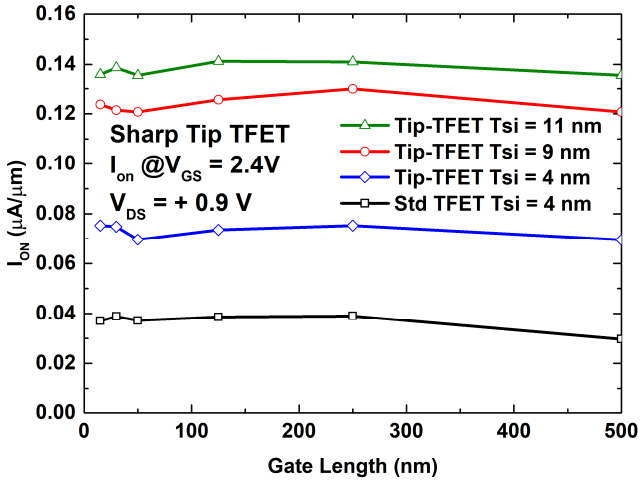

Figure 17. $I_{ON}(L_G)$ for Sharp Tip-TFET with different T_{Si} and standard TFET with T_{Si} = 4 nm.

6. SiGe TFETs

The PB-TFET exhibits the highest on-current among all the simulated architectures. So far the TCAD study was carried out for silicon homojunction structures. In this section additional simulations have been run using SiGe material with different germanium concentrations (30%, 50% and 100%) to evaluate possible performance improvements. TFET TCAD simulations with materials other than silicon are particularly challenging because the effective masses for the valence and conduction bands modify the values of the parameters that set up the BTBT generation rate in the simulator. These new values have been obtained from literature for unstrained SiGe (Ge at 30% and 50%) and pure Ge [47]. For both materials the tunneling direction is [110].

6.1. Pure Boron and Standard TFET

Results in Figure 18 show that using $Si_{0.7}Ge_{0.3}$ instead of silicon significantly increases the drain current in both Pure Boron and standard TFET architectures. In particular for T_{Si} = 4 nm, the performance of PB-TFET is higher and the subthreshold slope is steeper. Simulations are consistent with experimental data already obtained for SiGe TFETs [7]. Due to the relatively wide bandgap, silicon is not the best material to increase the tunneling probability even when architecture boosters are taken into account.

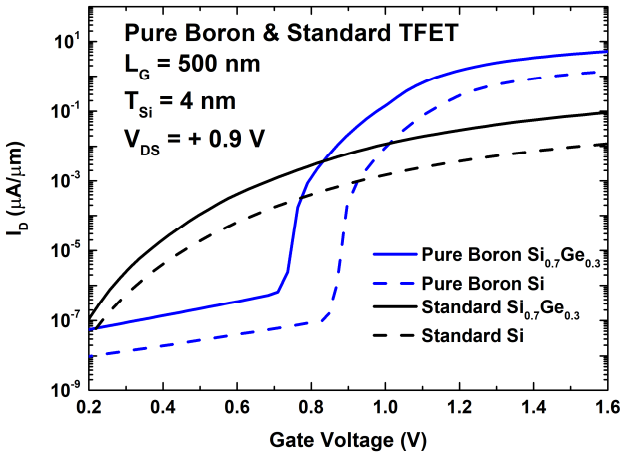

Figure 18. $I_D(V_G)$ curves of PB-TFET and standard TFET for Si and $Si_{0.7}Ge_{0.3}$ (T_{Si} = 4 nm). The tunneling current is enhanced for $Si_{0.7}Ge_{0.3}$ TFET in both architectures.

Simulations for $Si_{0.5}Ge_{0.5}$ TFETs (Figure 19a) show a better I_{ON} due to a reduced bandgap in comparison to $Si_{0.7}Ge_{0.3}$. However, I_{OFF} is also increased because a lower bandgap induces a higher tunneling current in the channel/drain junction. This implies a small I_{ON}/I_{OFF} ratio and a degradation of the subthreshold slope. Using pure germanium shows an outstanding increase of the on-current (Figure 19b). The germanium PB-TFET exhibits an increase by one order of magnitude (drain current higher than 10 µA/µm) and the germanium standard TFET an improvement of two orders of magnitude. Unfortunately, the increase of the off-current is severely pronounced and completely degrades the I_{ON}/I_{OFF} ratio as shown Figure 19b. Our results reveal that in order to enhance the tunneling current it is necessary to reduce the energy bandgap in the source/channel junction and in the extended region into the channel. Also, to avoid the off-current degradation a larger bandgap is suitable in the drain region, which could be achieved with heterojunction architectures. Using materials with a high forbidden bandgap (like silicon) will keep low the off-current and a steeper subthreshold slope will be obtained. Currently, it is possible to obtain standard SiGe TFETs with a germanium concentration of 30% via a well-controlled process fabrication. However, if the germanium concentration is increased beyond 30% the capability of the silicon platform to implement compound materials does not provide enough quality and a large concentration of defects may affect the SiGe layers. Therefore, TAT will increase subthreshold leakage and the SS cannot be lower than 60 mV/dec.

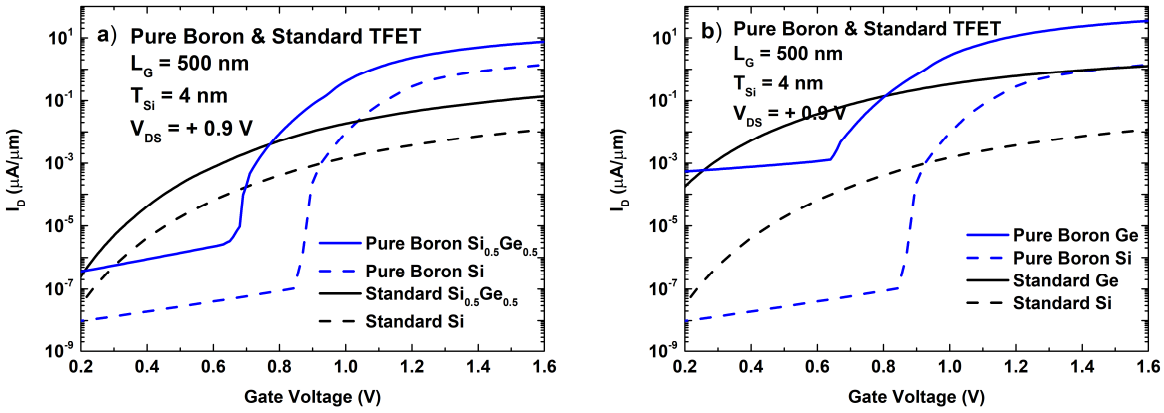

Figure 19. $I_D(V_G)$ curves of PB-TFET and standard TFET (T_{Si} = 4 nm): (a) $Si_{0.5}Ge_{0.5}$ and (b) pure germanium. Tunneling current is enhanced for a higher Ge concentration, but the off-current is degraded.

The SS extractions for standard TFET with different germanium concentrations (Figure 20a) exhibit a shift towards higher drain currents obtaining lower SS with respect to the silicon case. Moreover, for a pure germanium standard TFET SS reaches values below 60 mV/dec until $I_D = 10^{-5}$ μA/μm. In PB-TFET architecture (Figure 20b) there is a shift in the SS for higher drain currents when increasing the germanium concentration. For low I_D values (< 10^{-3} μA/μm) better SS results, below 60 mV/decade, are obtained for lower germanium concentrations. On the contrary, for higher I_D values (> 10^{-2} μA/μm) SS is reduced using pure germanium. However, the range for which SS is lower than 60 mV/dec is minimized. As said for the $I_D(V_G)$ curves in Figure 19b, using in the drain region a material with a larger energy bandgap will enable to reach SS below 60 mV/dec for several decades of current when increasing the germanium concentration in source and channel regions.

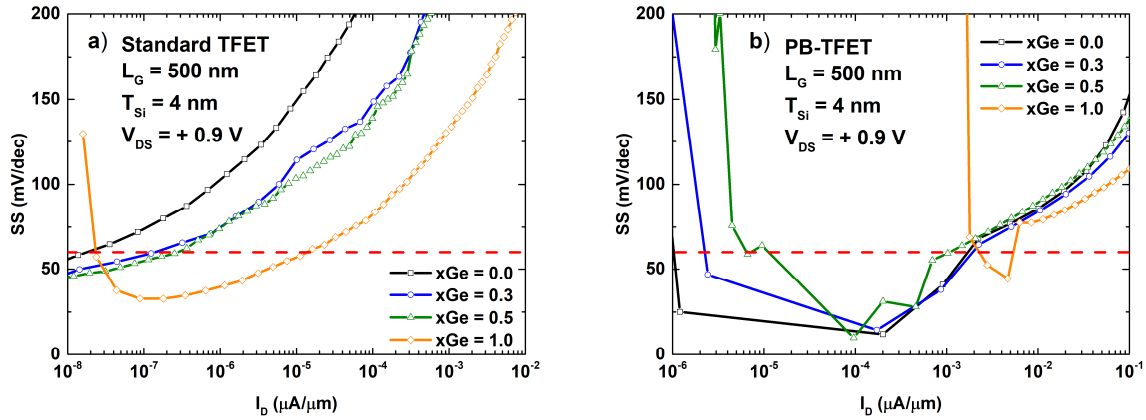

Figure 20. Subthreshold swing versus drain current curves with different germanium concentrations for long gate devices (500 nm) with T_{Si} = 4 nm: (a) Standard TFET and (b) Pure Boron TFET.

6.2. Impact of gate length and body thickness on drive current

Figure 21 shows that for T_{Si} = 4 nm and gate length of 500 nm the silicon PB-TFET presents good performance with I_{ON} current (~3.3 μA/μm). But as explained before, for short gate lengths the tunneling current

decreases due to the reduction of the extended source area. Nevertheless, the excellent electrostatic control due to the narrow thickness allows to extend the benefits of vertical BTBT even at short gate lengths (L_G < 100 nm). For the standard architecture using $Si_{0.7}Ge_{0.3}$ material, there is only a small increase in current. In the PB-TET there is a significantly gain of I_{ON} with respect to the silicon variant. This advantage is visible for all considered gate lengths at T_{Si} = 4 nm (Figure 21).

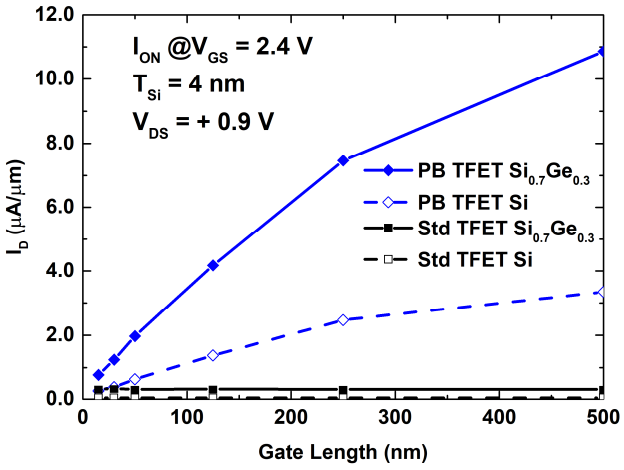

Figure 21. $I_{ON}(L_G)$ for standard and Pure Boron $Si_{0.7}Ge_{0.3}$ TFETs with T_{Si} = 4 nm. Even for short gate lengths PB $Si_{0.7}Ge_{0.3}$ TFET shows higher on-current than the standard TFET.

Increasing the channel thickness from 4 nm to 6 nm implies a wider tunneling length for the PB-TFET, and therefore a reduction of the tunneling current. For silicon PB-TFET the vertical BTBT generation current is still higher than the lateral tunneling of the standard TFET even for short gate lengths (Figure 22a). However, when using $Si_{0.7}Ge_{0.3}$ material, the Pure Boron architecture starts to show a loss of electrostatic control. For shorter gate lengths (L_G < 50 nm), the standard TFET with $Si_{0.7}Ge_{0.3}$ actually shows a higher I_{ON}. This trend is accentuated with T_{Si} = 8 nm (Figure 22b) because the tunneling length is too large and I_{ON} is severely degraded. In the case of silicon, the vertical BTBT of the PB-TFET architecture dominates over the standard TFET only for long gates, but for short gates (L_G < 100 nm) the current is degraded in comparison with lateral tunneling. Using $Si_{0.7}Ge_{0.3}$ material does not improve I_{ON} enough even at L_G = 500 nm where the standard TFET presents the same current as the PB-TFET architecture, simply because the device is too thick.

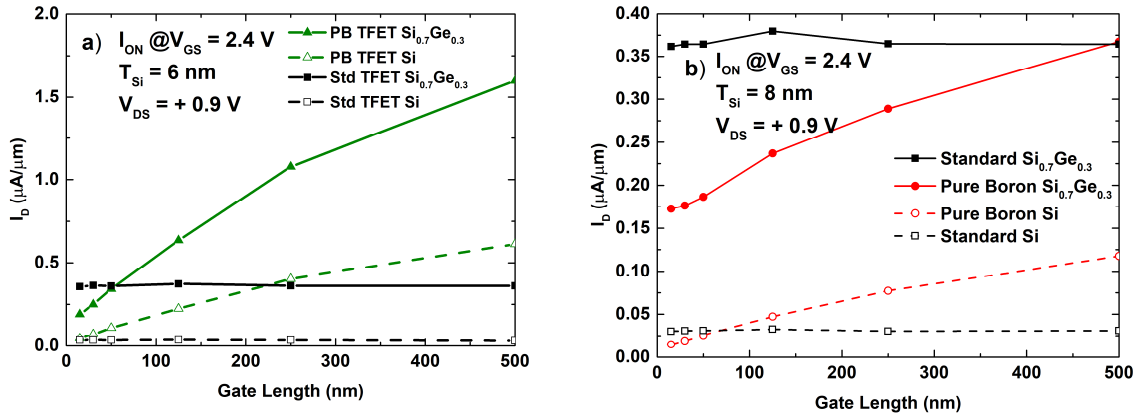

Figure 22. $I_{ON}(L_G)$ for standard and PB-TFET with silicon and $Si_{0.7}Ge_{0.3}$ TFETs: (a) For T_{Si} = 6 nm PB-TFET shows better performance except for shorter gate lengths (L_G < 100 nm) compared to the standard structure. (b) For T_{Si} = 8 nm $Si_{0.7}Ge_{0.3}$ PB-TFET is completely degraded for all gate lengths.

6.3. Impact of gate length for different germanium concentrations

In "relatively" thick 8 nm films using $Si_{0.5}Ge_{0.5}$ compound we obtain better I_{ON} currents in PB-TFETs for gates longer than 250 nm (Figure 23a). On the other hand, for germanium the tunneling current is significantly increased and the vertical component dominates even for gate lengths of 50 nm (Figure 23b). Due to the complexity to fabricate $Si_{0.5}Ge_{0.5}$ or pure germanium layers with low density of defect, we explore the benefit of body thickness, expected to enable higher on-current for reduced germanium concentration.

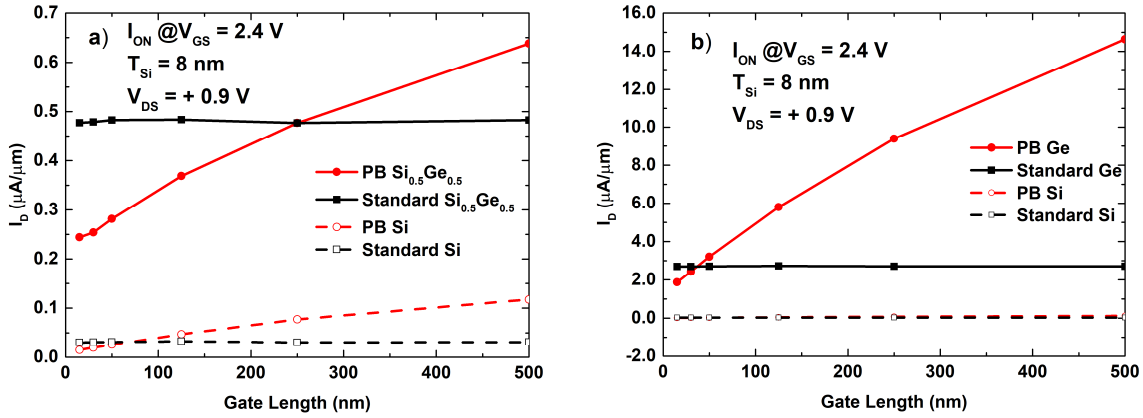

Figure 23. $I_{ON}(L_G)$ for standard and PB-TFET architectures with a body thickness of 8 nm: (a) for a germanium concentration of 50%; (b) for a germanium concentration of 100%.

Thinning down the body from 8 nm to 6 nm results in an increase of the tunneling current for both $Si_{0.5}Ge_{0.5}$ and pure germanium. Nevertheless, for $Si_{0.5}Ge_{0.5}$ it is not possible to extend the prevalence of vertical BTBT below a gate length of 50 nm (Figure 24a). In the case of the Ge PB-TFET, because of the narrow bandgap, vertical tunneling dominates even for extremely short gate lengths (L_G = 30 nm) as shown in Figure 24b.

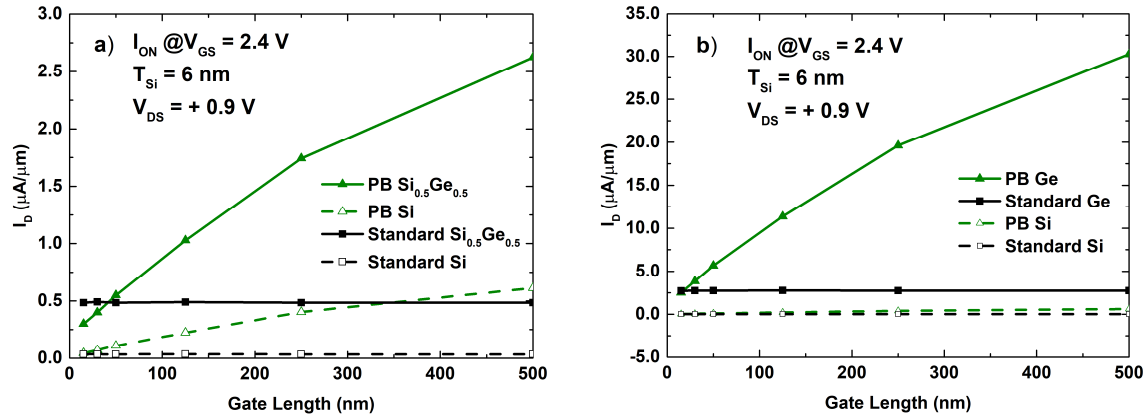

Figure 24. $I_{ON}(L_G)$ for standard and PB-TFET architectures with 6 nm body thickness: (a) with $Si_{0.5}Ge_{0.5}$ material; (b) with pure germanium.

The same trend is obtained for a 4 nm body thickness. It is remarkable that a reduction in thickness by 2 nm leads to 2-6 fold increase of the drive current. The outstanding electrostatic control is responsible of the dominance of vertical BTBT over the lateral tunneling for very short gate lengths (L_G < 50 nm) when using $Si_{0.5}Ge_{0.5}$ material (Figure 25a). For germanium, simulation results are even much better (Figure 25b) for all the studied gate lengths. These results indicate that TFETs with architectures based on vertical BTBT, require an extremely narrow channel thickness (T_{Si} < 6 nm) and a small bandgap in the source and channel regions in order to benefit from increase of the tunneling current.

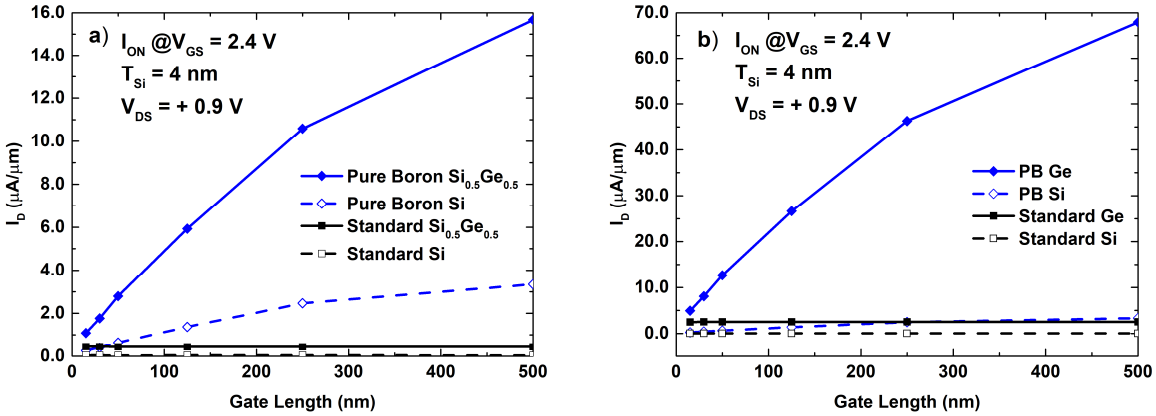

Figure 25. $I_{ON}(L_G)$ for standard and PB-TFET architectures with 4 nm body thickness: (a) with $Si_{0.5}Ge_{0.5}$ material; (b) with pure germanium.

7. Conclusions

Three innovative Tunnel FETs architectures are studied and compared to a standard reference TFET in the search of a better performance. For the Extended-Source TFET (ES-TFET) the innovation consists in optimizing the distance between the extension and the gate oxide (L_{rt}). $I_D(V_G)$ curves show for a "relatively" thick body of 11 nm, a high I_{ON} and a stepper SS below 60 mV/dec for small values of L_{rt} (3 nm, 4 nm and 5 nm). A larger L_{rt} causes a larger tunneling length and I_{ON} degradation owing to a lower effective electrostatic control from the front gate. The ES-TFET shows a better performance than the standard TFET for long and medium gate lengths, but for L_G smaller than 100 nm the reduction of the tunneling surface jeopardizes the on-current enhancement.

The implementation of an extremely thin layer of heavily doped boron (10^{21} cm^{-3}), takes advantage of the Pure Boron technology for small body thickness (T_{Si} < 6 nm) to solve the I_{ON} degradation for small gate lengths (L_G < 100 nm). There is an increase of the vertical BTBT due to a small tunneling length and better electrostatic control. The body thickness is a key parameter for the PB-TFET performance. In thicker channels (T_{Si} > 7 nm) the effect of the Pure Boron layer is attenuated.

The design of a sharp tip in the source junction is based on the fabrication of embedded source and drain junctions developed in CMOS technology to improve the strain characteristic and the performance. However, TCAD results show that this architecture does not significantly impact the I_{ON} and subthreshold slope and the benefit is marginal. Even though the electric field can be increased with this tip configuration, the tunneling area does not increase which explains why similar performance as the standard TFET is obtained.

TCAD simulations based on SiGe compounds and germanium for Pure Boron TFET and standard TFET present an increase of the tunneling current, when compared to silicon. The thinner the body (down to T_{Si} = 4 nm) the higher is I_{ON} for PB-TFETs; furthermore the benefits of the vertical BTBT are extended for short gate lengths (L_G < 50 nm). If the body thickness is increased (6 nm or 8 nm) a higher concentration of germanium is required to compensate a larger tunneling length. However, the complexity of SiGe or Ge device fabrication can produce a higher of defect density, and thus TAT mechanism can preclude the devices from achieving a SS lower than 60 mV/dec.

From this exhaustive TCAD study we can conclude that the most promising architecture for technological implementation appears to be the Pure Boron TFET with the smallest possible body thickness and a heterojunction structure. A reduced bandgap in the source and the channel regions will enhance the on-current and a large bandgap in the drain region will keep a low off-current and good I_{ON}/I_{OFF} ratio.

Acknowledgment

This work is partly funded through NANO 2017 French program and EQUIPEX FDSOI11. Dr. Lis Nanver is thanked for information on Pure Boron layers.

References

[1] W. M. Holt, "1.1 Moore's law: A path going forward," in *2016 IEEE International Solid-State Circuits Conference (ISSCC)*, 2016, pp. 8–13.

[2] J. Wu, J. Min, and Y. Taur, "Short-Channel Effects in Tunnel FETs," *IEEE Trans. Electron Devices*, vol. 62, no. 9, pp. 3019–3024, Sep. 2015.

[3] A. M. Ionescu, "Nano-devices with advanced junction engineering and improved energy efficiency," in *2017 17th International Workshop on Junction Technology (IWJT)*, 2017, pp. 1–6.

[4] S. Takagi *et al.*, "III-V/Ge MOS device technologies for low power integrated systems," *Solid-State Electron.*, vol. 125, pp. 82–102, Nov. 2016.

[5] A. M. Ionescu and H. Riel, "Tunnel field-effect transistors as energy-efficient electronic switches," *Nature*, vol. 479, no. 7373, pp. 329–337, Nov. 2011.

[6] A. Seabaugh *et al.*, "Steep slope transistors: Tunnel FETs and beyond," in *2016 46th European Solid-State Device Research Conference (ESSDERC)*, 2016, pp. 349–351.

[7] C. Le Royer *et al.*, "Fabrication and electrical characterizations of SGOI tunnel FETs with gate length down to 50 nm," *Solid-State Electron.*, vol. 115, pp. 167–172, Jan. 2016.

[8] A. Villalon *et al.*, "Experimental Investigation of the Tunneling Injection Boosters for Enhanced ETSOI Tunnel FET," *IEEE Trans. Electron Devices*, vol. 60, no. 12, pp. 4079–4084, Dec. 2013.

[9] C. Liu *et al.*, "Experimental I-V(T) and C-V Analysis of Si Planar p-TFETs on Ultrathin Body," *IEEE Trans. Electron Devices*, vol. 63, no. 12, pp. 5036–5040, Dec. 2016.

[10] I. A. Young, U. E. Avci, and D. H. Morris, "Tunneling field effect transistors: Device and circuit considerations for energy efficient logic opportunities," in *2015 IEEE International Electron Devices Meeting (IEDM)*, 2015, pp. 22.1.1–22.1.4.

[11] S. Agarwal and E. Yablonovitch, "The low voltage TFET demands higher perfection than previously required in electronics," in *2015 73rd Annual Device Research Conference (DRC)*, 2015, pp. 247–248.

[12] A. C. Seabaugh and Q. Zhang, "Low-Voltage Tunnel Transistors for Beyond CMOS Logic," *Proc. IEEE*, vol. 98, no. 12, pp. 2095–2110, Dec. 2010.

[13] S. M. Sze and K. K. Ng, "Tunnel Devices," in *Physics of Semiconductor Devices*, 3rd Edition., pp. 415–465.

[14] J. Knoch, S. Mantl, and J. Appenzeller, "Impact of the dimensionality on the performance of tunneling FETs: Bulk versus one-dimensional devices," *Solid-State Electron.*, vol. 51, no. 4, pp. 572–578, Apr. 2007.

[15] L. Knoll *et al.*, "Gate-all-around Si nanowire array tunnelling FETs with high on-current of 75 µA/ µm @ V_{DD} = 1.1V," in *2013 14th International Conference on Ultimate Integration on Silicon (ULIS)*, 2013, pp. 97–100.

[16] F. Mayer *et al.*, "Impact of SOI, Si1-xGexOI and GeOI substrates on CMOS compatible Tunnel FET performance," in *2008 IEEE International Electron Devices Meeting*, 2008, pp. 1–5.

[17] M. Kim, Y. Wakabayashi, R. Nakane, M. Yokoyama, M. Takenaka, and S. Takagi, "High Ion/Ioff Ge-source ultrathin body strained-SOI tunnel FETs," in *2014 IEEE International Electron Devices Meeting*, 2014, pp. 13.2.1–13.2.4.

[18] C. L. Royer *et al.*, "Experimental investigations of SiGe channels for enhancing the SGOI tunnel FETs performance," in *EUROSOI-ULIS 2015: 2015 Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon*, 2015, pp. 69–72.

[19] R. Pandey *et al.*, "Demonstration of p-type $In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$ and n-type $GaAs_{0.4}Sb_{0.6}/In_{0.65}Ga_{0.35}As$ complimentary Heterojunction Vertical Tunnel FETs for ultra-low power logic," in *2015 Symposium on VLSI Technology (VLSI Technology)*, 2015, pp. T206–T207.

[20] K. E. Moselund, D. Cutaia, H. Schmid, H. Riel, S. Sant, and A. Schenk, "Complementary III-V heterostructure tunnel FETs," in *2016 46th European Solid-State Device Research Conference (ESSDERC)*, 2016, pp. 403–407.

[21] S. Takagi and M. Takenaka, "III-V MOS device technologies for advanced CMOS and tunneling FET," in *2016 Compound Semiconductor Week (CSW) [Includes 28th International Conference on Indium Phosphide Related Materials (IPRM) 43rd International Symposium on Compound Semiconductors (ISCS)*, 2016, pp. 1–2.

[22] S. Blaeser *et al.*, "Novel SiGe/Si line tunneling TFET with high Ion at low Vdd and constant SS," in *2015 IEEE International Electron Devices Meeting (IEDM)*, 2015, pp. 22.3.1–22.3.4.

[23] Q. T. Zhao *et al.*, “Strained Si and SiGe Nanowire Tunnel FETs for Logic and Analog Applications,” *IEEE J. Electron Devices Soc.*, vol. 3, no. 3, pp. 103–114, May 2015.
[24] P. Zhang, J. Wan, A. Zaslavsky, and S. Cristoloveanu, “CMOS-compatible FDSOI bipolar-enhanced tunneling FET,” in *2015 IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S)*, 2015, pp. 1–3.
[25] Y. Wu, K. Kakushima, and Y. Takahashi, “Formation of magnesium silicide for source material in Si based tunnel FET by annealing of Mg/Si thin film multi-stacks,” in *2017 17th International Workshop on Junction Technology (IWJT)*, 2017, pp. 83–84.
[26] S. Glass *et al.*, “Investigation of TFETs with Vertical Tunneling Path for Low Average Subthreshold Swing,” in *2017 International Conference on Solid State Devices and Materials (SSDM)*, Sendai (Japan), 2017, pp. 227–228.
[27] S. Kim *et al.*, “Investigation of silicide-induced-dopant-activation for steep tunnel junction in tunnel field effect transistor (TFET),” *Solid-State Electron.*, Oct. 2017.
[28] H. Lu and A. Seabaugh, “Tunnel Field-Effect Transistors: State-of-the-Art,” *IEEE J. Electron Devices Soc.*, vol. 2, no. 4, pp. 44–49, Jul. 2014.
[29] K. Jeon *et al.*, “Si tunnel transistors with a novel silicided source and 46mV/dec swing,” in *2010 Symposium on VLSI Technology*, 2010, pp. 121–122.
[30] R. Gandhi, Z. Chen, N. Singh, K. Banerjee, and S. Lee, “CMOS-Compatible Vertical-Silicon-Nanowire Gate-All-Around p-Type Tunneling FETs With -mV/decade Subthreshold Swing,” *IEEE Electron Device Lett.*, vol. 32, no. 11, pp. 1504–1506, Nov. 2011.
[31] D. E. Nikonov and I. A. Young, “Benchmarking of Beyond-CMOS Exploratory Devices for Logic Integrated Circuits,” *IEEE J. Explor. Solid-State Comput. Devices Circuits*, vol. 1, pp. 3–11, Dec. 2015.
[32] C. Diaz Llorente *et al.*, “New insights on SOI Tunnel FETs with low-temperature process flow for CoolCube™ integration,” *Solid-State Electron.*, vol. 144, pp. 78–85, Jun. 2018.
[33] E. Memisevic, J. Svensson, M. Hellenbrand, E. Lind, and L. E. Wernersson, “Vertical InAs/GaAsSb/GaSb Tunneling Field-Effect Transistor on Si with S = 48 mV/decade and Ion = 10 μA/μm for Ioff = 1 nA/μm at Vds = 0.3 V,” in *2016 IEEE International Electron Devices Meeting (IEDM)*, 2016, pp. 19.1.1–19.1.4.
[34] “Sentaurus Device user guide. Sypnosys Sentaurus TCAD ver. L-2016.03.”
[35] Hraziia, A. Vladimirescu, A. Amara, and C. Anghel, “An analysis on the ambipolar current in Si double-gate tunnel FETs,” *Solid-State Electron.*, vol. 70, pp. 67–72, Apr. 2012.
[36] Y. Morita *et al.*, “Experimental realization of complementary p- and n- tunnel FinFETs with subthreshold slopes of less than 60 mV/decade and very low (pA/μm) off-current on a Si CMOS platform,” in *2014 IEEE International Electron Devices Meeting*, 2014, pp. 9.7.1–9.7.4.
[37] S. Blaeser *et al.*, “Line Tunneling Dominating Charge Transport in SiGe/Si Heterostructure TFETs,” *IEEE Trans. Electron Devices*, vol. 63, no. 11, pp. 4173–4178, Nov. 2016.
[38] A. Revelant *et al.*, “Electron-Hole Bilayer TFET: Experiments and Comments,” *IEEE Trans. Electron Devices*, vol. 61, no. 8, pp. 2674–2681, Aug. 2014.
[39] S. Cristoloveanu, S. Athanasiou, M. Bawedin, and P. Galy, “Evidence of Supercoupling Effect in Ultrathin Silicon Layers Using a Four-Gate MOSFET,” *IEEE Electron Device Lett.*, vol. 38, no. 2, pp. 157–159, Feb. 2017.
[40] L. K. Nanver *et al.*, “Pure-boron chemical-vapor-deposited layers: A new material for silicon device processing,” in *2010 18th International Conference on Advanced Thermal Processing of Semiconductors (RTP)*, 2010, pp. 136–139.
[41] L. Qi and L. K. Nanver, “Conductance Along the Interface Formed by 400 °C Pure Boron Deposition on Silicon,” *IEEE Electron Device Lett.*, vol. 36, no. 2, pp. 102–104, Feb. 2015.
[42] X. Liu, L. K. Nanver, and T. L. M. Scholtes, “Nanometer-Thin Pure Boron Layers as Mask for Silicon Micromachining,” *J. Microelectromechanical Syst.*, vol. 26, no. 6, pp. 1428–1434, Dec. 2017.
[43] L. Zhang and M. Chan, “SPICE Modeling of Double-Gate Tunnel-FETs Including Channel Transports,” *IEEE Trans. Electron Devices*, vol. 61, no. 2, pp. 300–307, Feb. 2014.
[44] C. Auth *et al.*, “45nm High-k + metal gate strain-enhanced transistors,” in *2008 Symposium on VLSI Technology*, 2008, pp. 128–129.
[45] P. Packan *et al.*, “High performance 32nm logic technology featuring 2nd generation high-k + metal gate transistors,” in *2009 IEEE International Electron Devices Meeting (IEDM)*, 2009, pp. 1–4.
[46] U. E. Avci *et al.*, “Study of TFET non-ideality effects for determination of geometry and defect density requirements for sub-60mV/dec Ge TFET,” in *2015 IEEE International Electron Devices Meeting (IEDM)*, 2015, pp. 34.5.1–34.5.4.
[47] K. H. Kao, A. S. Verhulst, W. G. Vandenberghe, B. Soree, G. Groeseneken, and K. D. Meyer, “Direct and Indirect Band-to-Band Tunneling in Germanium-Based TFETs,” *IEEE Trans. Electron Devices*, vol. 59, no. 2, pp. 292–301, Feb. 2012.