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Comparison between i_g Integration and v_{gs} Derivation methods dedicated to fast Short-Circuit 2D-Diagnosis for Wide Band Gap Power Devices

Yazan Barazi · Nicolas Rouger · Frédéric Richardeau

Abstract This paper presents and compares two original high speed protection circuits, i_g integration and v_{gs} derivation methods against Short Circuit (SC) types, Hard Switch Fault (HSF) and Fault Under Load (FUL). Since the gate-drain capacitor C_{gd} of a power device depends on v_{ds}, it can become an original native sensor to monitor the switching operation and so detect unwanted v_{ds} transition or absence of v_{ds} transition by monitoring only v_{gs}. Using only low-voltage monitoring is an essential step to integrate fast and embedded new detection methods on an ASIC gate driver. This C_{gd} capacitor plays a major part in the two detection methods. The first method is based on dedicated two-dimension monitoring of the gate charge transferred in a time interval combined with gate voltage monitoring. The second method consists of the reconstruction of the dv_{gs}/dt by means of a capacitive current sensing to provide the v_{gs} derivation combined with the v_{gs} monitoring. Comparison and simulation of the methods based on a *C2M0025120D* SiC MOSFET device under LTspice™ are made to verify the validity of the methods. In terms of detection speed of the SC, a detection time of 300ns is obtained for both methods. Both methods are easy to design, and to integrate. However, the robustness and the speed of detection trade-off of all these methods will be analyzed and compared relatively to the critical functionalities.

1 Introduction

Wide band gap semiconductor materials, such as Silicon Carbide (SiC), have shown a tremendous evolution. However, power semiconductor devices such as Insulted Gate Bipolar Transistors (IGBT) and MOSFET Super Junction (SJ-MOSFET) silicon devices are limited, in terms of maximum switching speeds. Consequently, Silicon power devices have, higher switching losses, large and expensive thermal management systems. On the other hand, SiC MOSFETs are promising power semiconductor devices for high density converters, with low conduction and switching losses, high temperature stability[1]. However, the short circuit delay time capability for SiC MOSFETs is lower than silicon devices [2].

Power semiconductors devices are used in various industrial applications (Motor Drives, Battery Chargers, Switch Mode Power Supplies, Converters, …). They are exposed to several types of Short Circuit. HSF (SC type I) and FUL (SC type II) are the two main fault behaviors. Safety is necessary for those typical applications. Several ways of protecting circuits have been presented for either Silicon IGBT's or MOSFET's [3]. Most of the previous proposed techniques rely on the drain-source voltage or current. This is clearly a limiting approach due to the high voltage diode or additional current sensor used, such as MOSFET-sense-current in non-standard dies [4-5-6-7].

In SiC MOSFETs; the drain current i_{ds} is controlled by the gate voltage v_{gs}. Since most Wide Band Gap (WBG) power FETs exhibit a low robustness and a typical fail-to-short behavior, they must be turned-off softly in a few hundreds of nanoseconds, after fault-detection. Good management of the gate voltage results in the best compromise between losses - EMI - safety. The reverse transfer capacitance "C_{rss} = C_{gd}" of a SiC MOSFET also known as the Miller capacitance, is one of the most important parameters in switching performance for unipolar devices. This capacitance is a nonlinear function of voltages v_{gs} and v_{ds} and it provides a feedback between the output voltage v_{ds} and the input v_{gs} of the device.

In this article, detailed analyses and comparisons between the SC detection methods are presented. LTspice™ simulated results are presented in the view of verifying the SC detection methods to further protect SiC MOSFETs.

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2 i_g Integration detection method

2.1. Normal Turn-On "NTO"

A useful parameter from the circuit design point of view is the gate charge Q_g, in which the gate charge Q_{gd} related to C_{gd} can be predominant. Fig. 1 presents the qualitative typical switching waveforms and the different contributions to the total gate charge during Normal Turn On NTO. The first gate charge amount Q_1 is defined where $1/C_{issmin}$ is its slope (1), in the first time interval $[t_0 - t_2]$. Q_2 is the second gate charge amount, between $[t_2 - t_3]$ during the Miller plateau where v_{ds} drops from v_{bus} to approximately (v_{gs}-v_{th}) slightly lower than $R_{dson}.I_{load}$ while v_{gs} stays constant and C_{gd} or C_{Miller} starts to discharge, allowing the fast voltage change across the Drain-Source terminals. In the presence of a SiC transistor, a short inversion channel is generally used to reduce the losses in the on-state. This property causes a dependence of $v_{gsplateau}$ to variations in drain voltage than it can be in vertical silicon device (ex. SJ-VDMOS, IGBT…); a slight slope appears instead of the plateau [8] (2). The third time interval began at t_3 with v_{gs} increasing back, until it reaches v_{Drv+}, and gate charge amount Q_g reaches Q_{gTot} (4), with $1/C_{issmax}$ as a slope of the third amount of gate charge Q_3 (3). At the end of this time interval, the two capacitance C_{gd} and C_{gs} fully charged [9-10].

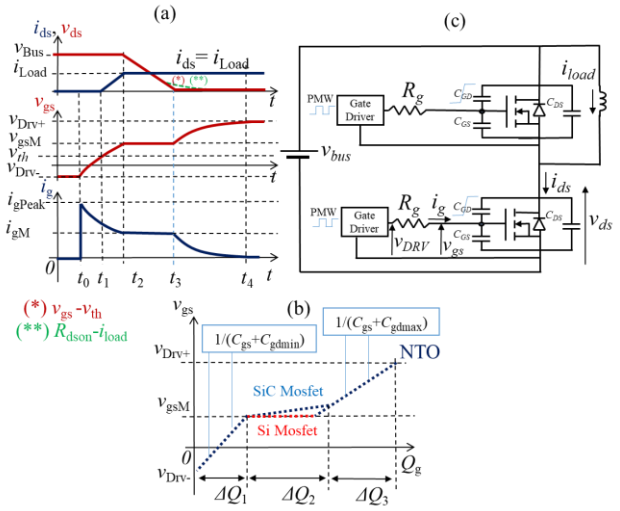


Fig. 1 (a). Turn-on switching characteristics of SiC MOSFET under NTO condition. (b). Gate Charge characteristics "NTO". (c). Equivalent circuit of the half bridge. *Note (Fig. 1-3): For the purposes of a simple graphical representation, C_{gs} and C_{gd} capacitors are taken here as constant values. The voltage drops in on-state of the components (diode and transistor) are also not taken into account for the switching study. A constant Miller plateau is also assumed in the figures. Neither the reverse recovery nor the parasitic inductances are taken into account.

$$\Delta Q_1 = C_{issmin}.(v_{gs} - v_{Drv-}); \qquad v_{gs} \in [v_{Drv-}; v_{gsM}[\quad (1)$$

$$\Delta Q_2 = \int_0^{v_{gsM}} C_{gdmax}.dv_{gd}{}^{(*)} + \int_{v_{th}}^{v_{bus}+v_{body}-v_{gsM}} C_{gd}(v_{gd}).dv_{gd} \quad (2)$$

$$\Delta Q_3 = C_{issmax}.(v_{gs} - v_{gsM}); \qquad v_{gs} \in]v_{gsM}; v_{Drv+}] \quad (3)$$

$$Q_{gTot} = \Delta Q_1 + \Delta Q_2 + \Delta Q_3 \quad (4)$$

$$C_{iss} = C_{gs} + C_{gd} \quad \& \quad v_{gsM} = v_{gsplateau} \quad (5)$$

* In (2) the first integration is added to include the changes of C_{gd} from t_0 to t_2 Fig. 1; t_2 the beginning of the Miller plateau, the non-included integral when v_{ds} starts to fall.

2.2. Hard switch Fault "HSF"

Contrary to fault condition type I, when v_{gs}=v_{gsM} at t_2, v_{gs} and i_{ds} continue to increase until v_{gs} reaches v_{Drv+} and i_{ds} overcurrent, t_3, i_{ds}=$i_{sat\text{-}channel}$. v_{ds} stays at the v_{bus} value, which causes the transistor to operate in its saturation regime, as shown in Fig. 2(a). Such a regime can be sustainable only for a couple of µs, as presented in [11]. The amount of gate charge is $Q_{SC\text{-}HSF}$ with a $1/C_{issmin}$ slope, exhibiting no change in the charging rate of the input capacitance. In this SC operation, there is no discharge of the Miller capacitance. As a consequence, a significant difference appears in the Q_g characteristic between NTO and HSF, as shown in Fig. 2(b).

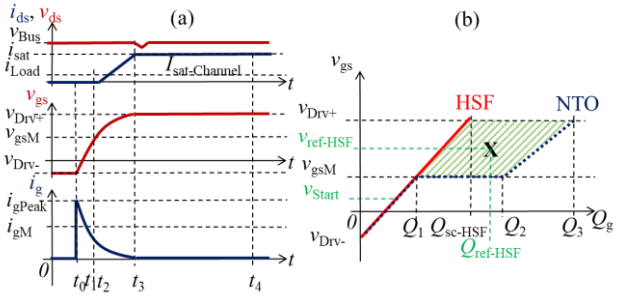


Fig. 2 (a). Turn-on switching characteristics of SiC MOSFET under HSF. **(b).** 2D representation of the Gate Charge characteristics "HSF" and detection zone with v_{gs}.

An HSF can be detected by monitoring v_{gs} and the amount of Q_g, whereas the assessment of the time variable is not directly required. Then, a detection method based on the gate charge is proposed. As mentioned previously, a significant difference appears in the Q_g amount, as shown in Q_g characteristics, Fig. 2(b). A detection selectivity criterion can be introduced by the ratio S=($Q_{SC\text{-}HSF}$)/(Q_{gTot}).

Table 1 Ratio of different technology

Technology	Designer	v_{rating}	v_{bus}	v_{gs}	S
Gan-GS6516	GanSystems	650V	400V	0/6 V	0.70
SiC-C2M160120	WolfSpeed	1200V	800V	-5/20	0.47
Si-IKW40N120	Infineon	1200V	960V	0/15V	0.18

For a better detection, the threshold level of v_{ref} and Q_{ref} need to be in the hatched trapezoid {(Q_1, v_{gsM}); (Q_2, v_{gsM}); (Q_{SC}, v_{Drv+}); (Q_3, v_{Drv+})} of the Fig. 2(b). Hence, this detection method is a two-dimension diagnosis. Most of the time, this Q_g characteristic figure is given in the data-sheet under NTO. The choice of the threshold detection levels v_{ref} and Q_{ref} can then be assessed from the data-sheet. The method is naturally robust against variation in switching delay time due to variation in threshold voltage or current operating point of the load. With a constant threshold level and sense resistor R_s, the detection will simply be a matter of blocks design to obtain the gate charge Q_g [12-13].

2.3. Fault Under Load (FUL)

Fault condition type II on the other hand appears after the three normal time intervals are accomplished, namely after t_4, where the MOSFET is in on-state ohmic mode $v_{gs}=v_{Drv+}$. In this fault condition, i_{ds} increase to $i_{ds\text{-}sat}$ (which can be calculated by the trans-conductance curve $i_{ds}=f(v_{gs})$ at v_{bus}), which in turn raises v_{ds} to the bus voltage v_{bus}, due to the MOSFET entering the saturation regime Therefore, a reverse current flows into the gate $i_g<0$ through C_{gd}, due to the Miller coupling; and the capacitance C_{gd} decreases. All these phenomena lead to the increase of v_{gs} towards a larger value v_{gsov}, see Fig. 3(a). The amount of gate charge is $Q_{SC\text{-}FUL}$, which also corresponds to a higher gate voltage v_{gsov}, Fig. 3(b). A FUL can be detected by monitoring v_{gs} and the amount of Q_g, but for different threshold levels of v_{ref} and Q_{ref}, whose value need to be in the hatched triangle of Fig. 3(b).

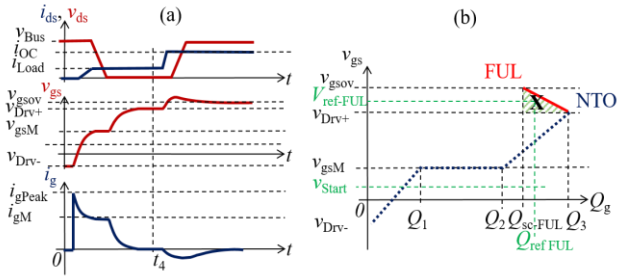


Fig. 3 (a). Turn-on switching characteristics of SiC MOSFET under FUL. **(b).** 2D representation of the Gate Charge characteristics "FUL" and detection zone with v_{gs} above v_{Drv+}.

2.4. Detection circuit based on gate charge monitoring

The proposed method is based on a gate charge characteristic as listed in this paper as the integration method also known as the gate charge method. In general, the charge transferred in time interval is obtained by integrating the current (6). Since the charge needed in this work is the gate charge, the gate current i_g under NTO, HSF or FUL is integrated and the gate charge is then calculated for each condition. Using the reference levels v_{ref} and Q_{ref} presented on the equations below (7-11), the detection of the SC is possible without setting a detection time window [14].

$$Q_g = \int i_g\, dt \tag{6}$$

$$v_{ref-Start} = p.v_{Drv+} \tag{7}$$

$$v_{ref-HSF} = k.v_{Drv+} \tag{8}$$

$$Q_{ref-HSF} = k'.Q_{Tot} \tag{9}$$

$$v_{\text{ref-FUL}} = (1+\text{r}).v_{\text{Drv+}} \tag{10}$$

$$Q_{ref-FUL} = r'.Q_{Tot} \tag{11}$$

With *p, k, k', r, r'* ponderation multipliers needed for the appropriate position of the reference levels.

Table 2 2D diagnosis algorithm for HSF

Comparator	Output Diagnosis
If $Q_g>Q_{ref\text{-}HSF}$ **AND** $v_{gs}>v_{ref\text{-}HSF}$ then	NTO
If $Q_g<Q_{ref\text{-}HSF}$ **AND** $v_{gs}>v_{ref\text{-}HSF}$ then	HSF

Table 3 Diagnosis algorithm for FUL

Comparator	Output Diagnosis
If $Q_g>Q_{ref\text{-}FUL}$ **AND** $v_{gs}<v_{ref\text{-}FUL}$ then	NTO
If $Q_g<Q_{ref\text{-}FUL}$ **AND** $v_{gs}>v_{ref\text{-}FUL}$ then	FUL

Tabs. 2-3 simplify the aforementioned figures about the gate charge characteristics and also bring guidance to the detection circuit below [7], gathering all the data to design the detection circuit. A comparator with $v_{ref\text{-}Start}$ (7) activates the detection circuit. A Differential amplifier at the R_S terminals (sensing resistance integrated on the gate driver, $R_s<<R_g+R_{int}$) is needed, to create the image of the current i_g from the voltage across the sense resistor R_s and then amplify it for a better integration. With those two main blocks (Diff. Amp. Followed by Integrator) we obtain the gate charge Q_g, which is then further compared with the threshold $Q_{ref\text{-}HSF}$ and $Q_{ref\text{-}FUL}$ levels. Before that, to make sure that the detection is at the right moment, two additional comparators with $v_{ref\text{-}HSF}$ and $v_{ref\text{-}FUL}$ are used to activate the monitoring - see Fig. 4.

For HSF, Tab. 2, when the output of the $v_{ref\text{-}HSF}$ comparator reaches a logic state '1' (non-priority value of the AND gate), this signal goes through the first input of the AND-HSF gate. The second input will decide the state of the detection circuit: if the calculated Q_g is below the $Q_{ref\text{-}HSF}$, then the second input (the output of the $Q_{ref\text{-}HSF}$) of the AND-HSF gate goes high '1' logic state. The output of the AND-HSF gate goes high as well, which generates a flag for further SC protection. On the other hand, if one of those two inputs; the two outputs of the $v_{ref\text{-}HSF}$ and $Q_{ref\text{-}HSF}$ comparators; is in a '0' logic state there is no flag, and no detected SC. For FUL, the same method is applied where both $v_{ref\text{-}FUL}$ and $Q_{ref\text{-}FUL}$ comparators outputs need to have a '1' logic state.

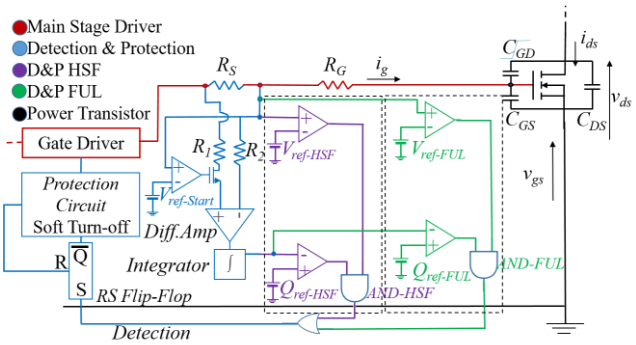


Fig. 4 Fast 2D-diagnosis and protection circuit based on gate charge. Note: Rs=1Ω, R1=R2=20KΩ, other blocks are considered ideals.

This principle will be more sensitive and robust for lower $Q_{SC\text{-}HSF}/Q_{gTot}$ ratios. This constraint is far from assured for WBG devices where the C_{gd}/C_{gs} ratio is voluntarily minimized by designers to reduce the cross-talk phenomenon in inverter leg operation. As mentioned in Tab. 1, some commercially available SiC devices will be more suitable than others. Commercially available High Voltage GaN power transistors seem poorly adapted to this technique. Higher $v_{ref\text{-}HSF}$ values lead to a more robust

diagnosis, albeit with longer delay times. Nevertheless, it remains a general principle, also named "2D-adaptive-detection", only combining two low-voltage waveforms or signals without resorting directly to time measurement. One can note that this method can be easily integrated in a low voltage ASIC which would not be allowed with a classical high voltage detection V_{dssat} (Saturation Voltage). Moreover, the Q_g method is an integral technique which will introduce less SNR.

3 Derivation detection method

3.1. Behavior and characteristic

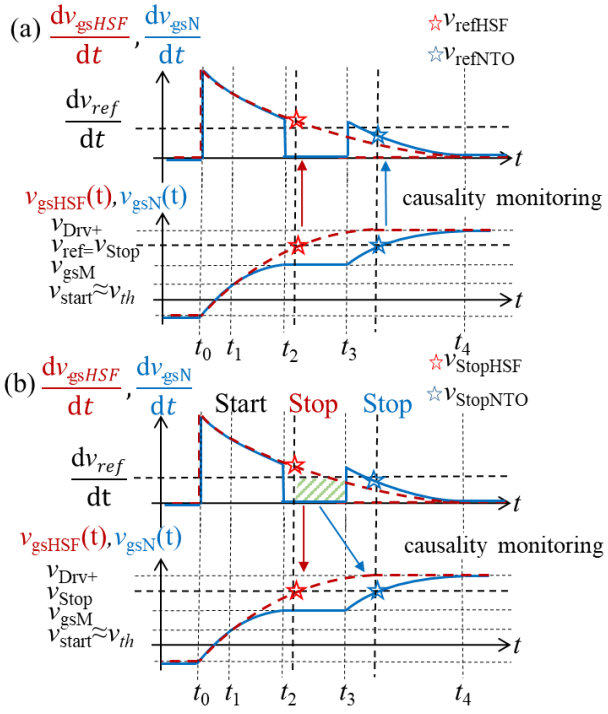


Fig. 5 dv_{gs}/dt characteristics under "NTO" and "HSF". (a) Slope detection approach, (b) Dip detection approach. the stars represent the levels obtained for the same gate-voltage, $v_{gs}=v_{ref}=v_{stop}$, with $v_{ref} > v_{gsM}$ for the slope approach, and for the dip approach $v_{gs}=v_{stop}$ is not a reference level for comparison.

Even with optimized detection thresholds, the previous method based on the gate-current integration over the gate-voltage range may not be fast enough for SC protection. The following methods provide a more direct quasi-instantaneous detection without the need for gate charge method. The impact of the capacitance C_{gd} in the switching behavior is demonstrated also on a new detection method based on monitoring the quasi-derivation of v_{gs}. There are three important time intervals on the behavior of v_{gs} as explained above. The first one has a slope of C_{issmin}, followed by the Miller plateau where C_{gd} is involved and the last one has a slope of C_{issmax}. Using this alteration of slopes, a significant impact appears on their time derivatives. Fig. 5 shows the dv_{gs}/dt signal (slightly filtered) under NTO and a SC conditions, where two distinctive changes of slope can be observed. Time interval $[t_0, t_2]$, in Fig. 5 dv_{gs}/dt signal present, a high peak "$C_{issmin}<C_{issmax}$" followed by a decrease until reaching a dip presenting the plateau period $[t_2, t_3]$. A smaller peak occurs at t_3 to present C_{issmax}. The dv_{gs}/dt signal under SC is quite straight forward, where there is only C_{issmin} as a slope for v_{gs} signal, from t_0 to t_4 dv_{gs}/dt is the derivation of the slope C_{issmin}, the dip or the smaller peak is not present. Fig. 5(a) and Fig. 5(b) introduce two different ways to analyze the derivation signal. Other approaches [15].

From this analysis two detection approaches can be concluded; the first one is based on the changes of the dv_{gs}/dt waveforms, where a threshold level dv_{ref}/dt is needed to be fixed for dv/dt signal, to distinguish between C_{issmax} for NTO and C_{issmin} for HSF at the threshold level $v_{gs}=v_{ref}$. This threshold level v_{ref} is used to activate the lecture of the comparison, as well as, the SC detection, Tab. 4. Fig. 5(a) shows the importance of the v_{ref} level (represented by stars), while removing any direct dependence with time. Indeed, the v_{ref} detection is indirectly reflected in different times for NTO and HSF. Therefore, the difference between the slopes define the NTO or HSF detections. The second detection approach is based on the detection of the dip in the derivation signal, the presence of Miller plateau. A threshold level dv_{ref}/dt is needed as well. Under SC condition, the two approaches do not have any difference detecting at v_{ref} the presence of C_{issmin} or a non-presence of a dip. The approach is to detect the signal above dv_{ref}/dt before reaching $v_{ref,}$ Tab. 4-5. On the other hand, under NTO condition, the two approaches are almost similar, both of them being based on the detection of the signal below dv_{ref}/dt. The only difference is to detect before $v_{gs}>v_{ref}$ when the dip is quickly detected or at $v_{gs}=v_{ref}$ detecting C_{issmax} slope changes.

Table 4 2D diagnosis for HSF, v_{gs} Slope approach

Comparator	Output
If $v_{gs}=v_{ref}$ **AND** $dv_g/dt<dv_{ref}/dt$ then	NTO
If $v_{gs}=v_{ref}$ **AND** $dv_g/dt>dv_{ref}/dt$ then	HSF

Table 5 2D diagnosis for HSF, Dip approach

Comparator	Output
If $dv_g/dt<dv_{ref}/dt$ **AND** $v_{gs}<v_{ref}$ then	NTO
If $dv_{gs}/dt>dv_{ref}/dt$ **AND** $v_{gs}<v_{ref}$ then	HSF

Both approaches can be accurate and robust because they are based on 2D-detection $dv_{gs}/dt \sim i_{Ciss}$ combined with v_{gs}. The second approach may be faster in NTO operation, where dip detection is before reaching v_{ref}. More importantly, the 2nd approach may help the robustness of the detection by allowing a lower dv_{ref}/dt; consequently, a wider discrimination range for a SC detection is offered, avoiding the small critical zone whenever v_{gsNTO} & v_{gsSC} have similar values. The different threshold voltages must be defined from key parameters extracted from the datasheet, operating conditions and experimental results.

3.2. Detection circuit based on derivation monitoring and simulation behavior

The proposed method is based on the derivation method. As known, the current that runs through a capacitor is given by the voltage/current relationship (12), where C_s is the sensing capacitor at the gate of the power device. Using this voltage/current relationship gives the derivative of v_{gs}.

$$\frac{dv_{gs}}{dt} = \frac{i_{Cs}}{c_s} \qquad (12)$$

Fig. 6 presents the detection circuit for a constant R_g. The capacitor C_s connected in parallel with the gate is a sense capacitor, sensing the derivation of the voltage v_{gs}. This sense capacitor must be much smaller than the minimum input capacitor of the power transistor (C_s << C_{issmin}). The i_{cs} current passing through C_s is further amplified and converted in a voltage, which is then compared with dv_{ref}/dt. Two others comparators with v_{gs} signal are used to create a monitoring window for the readout and detection. Flip-Flops are added for both approaches, the purple parts being the dip detection circuit, and the green ones are the slope detection circuits.

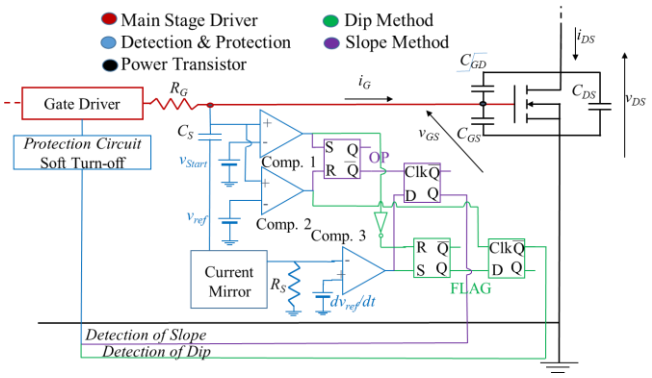


Fig. 6 Detection and protection circuit based on slope and dip approaches (input Smith triggered gate are not represented). Note: C_s=100pF, R_s=100Ω, other blocks are considered ideals.

4 Simulation result

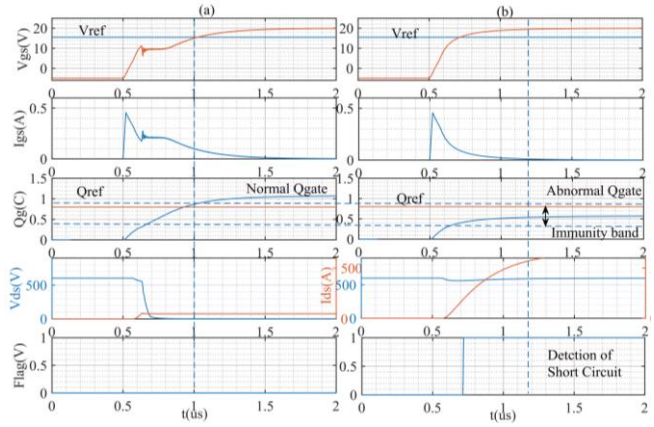


Fig. 7 Waveform characteristics using LT-Spice at V_{bus}=600V, I_{load}=50A. under (a) NTO and (b) HSF, *NB: Protection is not taken into consideration.

Simulations using LT-Spice are performed to verify the validity of the proposed detection circuits. The parameters used in the simulations are a power device C2M0025120D, v_{bus}=600 V, i_{load}=50 A, v_{Drv}= ±5/20 V and R_g=50 Ω. Gate loop and power loop parasitic inductances were included to better reproduce experimental waveforms. The value of R_g is deliberately chosen high for representation purposes. For lower values of R_g, the detection must be faster.

4.1. Detection and protection circuit simulation based on 2D gate charge monitoring

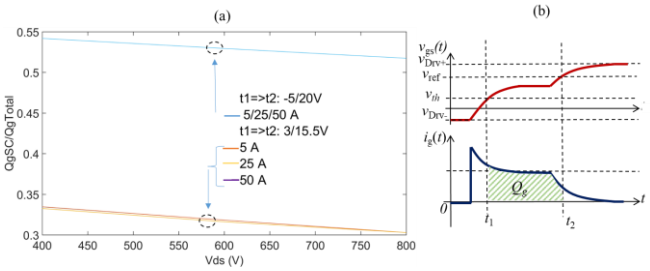


Fig. 8 (a). Variation of the Amount of charge for different v_{ds}, i_{ds}, and v_{gs}. **(b)** v_{gs}, i_g characteristic to present integration period.

Fig. 8 introduces the robustness [17-18-19], highlighting the effect of different integration windows. Fig. 8 (a) presents the ratio of $Q_{SC\text{-}HSF}/Q_{gTot}$ for different v_{ds} and i_{ds}. The integration window can be calculated between v_{gs}=-5/+20V or +3/+15.5V. This latter setting offers a smaller $Q_{SC\text{-}HSF}/Q_{gTot}$ ratio, which reduces the stress on Q_g detection threshold. The lower the ratio, the easier the detection.

4.2. Detection and protection circuit simulation based on 2D derivation monitoring

Fig. 9 presents the simulation voltage signal v_{gs} and its derivative under NTO and HSF conditions. Fig. 11 takes further the NTO condition into different i_{ds} and v_{ds} values.

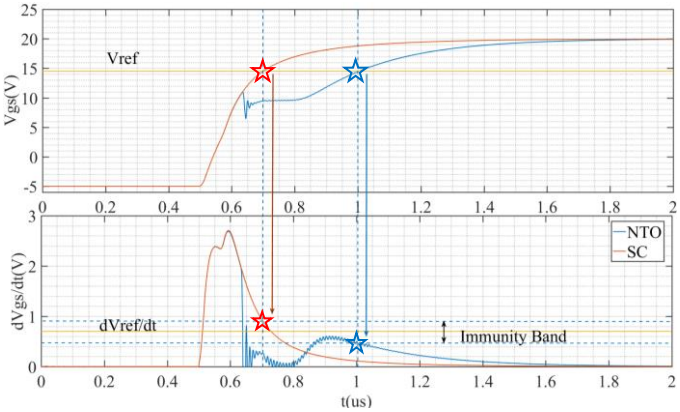


Fig. 9 Simulation Waveforms under NTO and HSF condition without the protection circuit.

As shown in Fig. 10, both methods are independent of time. The detection time for both methods is below 300ns due to the same reference gate voltage v_{ref} 15.5V. Fig. 11 presents how important v_{ref} should be early for the detection of SC. With an early $v_{ref,}$ an early detection will take place and probably v_{ref} interfering with the second peak in NTO mode,

causing a false detection. To overcome this interference, the dip method will not take into consideration the second peak, even if there are interferences. Fig. 11 represents a variation of i_{load} and v_{bus} in the circuit, under HSF. Where we can see the oscillation reaches dv_{ref}/dt, for low i_{ds} & v_{ds}. Under SC, dv/dt does not show any oscillation.

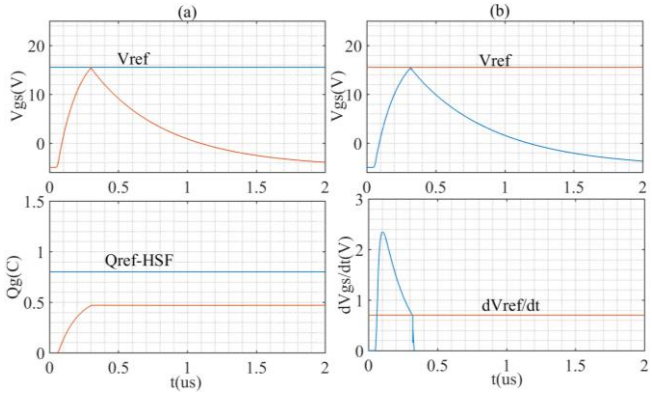


Fig. 10 Simulation Waveforms under HSF condition with the protection circuit. (a) Derivation method, (b) Gate charge method.

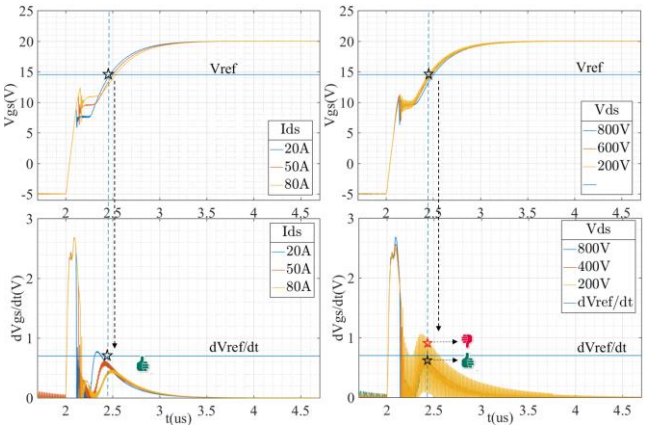


Fig. 11 Simulation Waveforms under NTO condition for different i_{ds} and v_{ds} without the protection circuit.

5 Conclusions and Comparison

This paper introduces two 2D detection method circuits, both of them being time independent. Both methods protect the power circuit in the event of a SC. The gate charge method exhibited a fast detection and protection capability and introduces less SNR under NTO and HSF. The reference levels are the critical values for both methods. The derivation method was presented with two approaches. With the slope approach, oscillation can slightly distort the detection, if the detection is at a critical v_{ref} (dv_{ref}/dt interfering with dv_{gs}/dt). On the other hand, the dip approach is better due to the dip presence, under NTO condition, even with dv_{ref}/dt interfering with dv_{gs}/dt, the detection of a dip occurs before the interference of the second peak. Under HSF, no oscillations are present for both approaches.

For robustness and a fast detection, the highest dv_{ref}/dt and the lowest v_{ref} the better. In other words, setting dv_{ref}/dt higher, will prevent interferences. Defining a low v_{ref}, allows an early detection.

These techniques will be implemented experimentally and compared with the simulations. Several limitations must be particularly addressed, such as the precise assessment of the threshold voltages with the dip method, the effects of parasitic elements and non-ideal circuits.

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