Gate leakage-current, damaged gate and open-circuit failure-mode of recent SiC Power Mosfet

Overview and analysis of unique properties for converter protection and possible future safety management

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***Abstract*— The silicon carbide MOSFETs tend to become the standard for high-performance medium voltage power electronics in terms of compactness and efficiency. Although the weakness of its gate-oxide and the relatively low short-circuit time capability are known limitations, this device reveals interesting unique properties. In this paper the authors explore the gate leakage-current behavior in normal and pre-damage operations as well as the conditions for obtaining an atypical and very interesting fail-to-open mode which has never been observed with silicon dies. These properties may be used for dedicated and innovative protection techniques for safer converter.**

Keywords—Mosfet; SiC; reliability; short-circuit; fault-management, fail-safe operation

I. INTRODUCTION

Power electronics require increasingly efficient components to meet the antagonistic challenges of a high level of integration and high energy efficiency. Among these components, the SiC MOSFET family becomes unbreakable in the voltage range from 600V to 1700V. These devices can be used as a discrete chip for medium power auxiliaries and as multi-chips power modules for automotive and railway traction applications for example. However, the presence of a thin gate-oxide (typically 50nm against 100nm in silicone [1]) and a high gate-bias voltage, to compensate the low electron mobility in the channel [1], causes the gate oxyde to undergo an very high electric field (400V/µm compared to about 1kV/µm for the electric field breakdown). Aside from the SiO_2-SiC interface fault issues, it is clear that the oxide region is much more stressed in SiC MOSFET than those in silicon, especially, in presence of a high short-circuit current density leading to a lower short-circuit duration capability [2]–[5] (often lower than 5µs against at least higher than 10µs in silicon). Although these last limitations are well known and have been the subject of numerous publications, the SiC MOSFET reveals others unique properties which need to be better understood and exploited, in order to make the disadvantages into clear advantages, typically for a diagnosis approach. In these conditions, the authors specifically explore the gate leakage-current behavior and the modelling of the SiC MOSFET in normal and pre-damaged operations as well as the conditions for obtaining an original and safe fail-to-open mode of the power devices after a short-circuit fault. This last property is expected as a major property for a native protection of a voltage source inverter-leg in shoot-through mode as depicted in Fig. 1.

Note that the conditions under which destructive SiC MOSFET failure modes occur have been even less studied than the electrical characterization of gate leakage-current. However, references [6] – [9] can be noted. In [6], an electrothermal modelling is proposed to estimate the junction temperature of planar and trench devices just before failure; in [7], a very interesting correlation is proposed between the thermal dynamics at the top of the die and the type of failure; in [8], a parametric study of the short-circuit robustness to failure is proposed and in [9], elements of physical understanding on the origin of the thermal runaway leading to a destructive latch-up effect is proposed. Note finally that technological analysis of the destruction are even less studied in literature justify why we present at the end of the article some elements from ours tests.

This paper is organized in four sections. Section II is dedicated to the gate-leakage current analysis and PLECS™ electrical modelling including damage operation and failure analysis. Section III summarizes a Comsol™ - Matlab™ - PLECS™ 1D electro-thermal modelling of the gate-source and drain-source current evolutions in short-circuit operations. Finally, section IV explains the conditions for obtaining the safe fail-to-open behavior of the SiC MOSFET devices by the analysis on the previous thermal modelling and the physical analysis of the failed die top-metal.

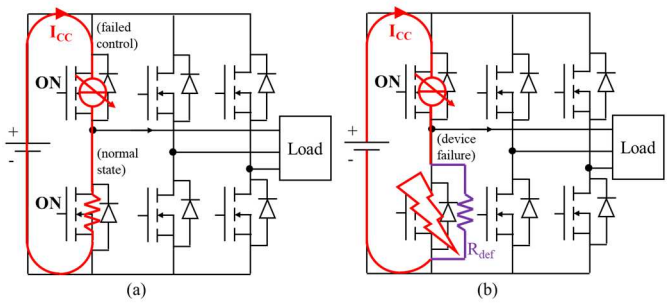


Fig. 1. Inverter-leg shoot-through operation : (a) by control signals. (b) by electrical breakdown of one of the power devices.

II. GATE LEAKAGE CURRENT AND DAMAGE

A. Experimental Gate leakage analysis

Short-circuit effect analysis is not only used to evaluate the extreme robustness of power devices but also to detect specific physical properties of the device in relation with its architecture. To this end, commercial discrete SiC MOSFET (1.2kV/80mΩ@25°C - TO247 package) were evaluated in short-circuit operations as described in Fig. 1a through a dedicated lab set-up. Fig. 2 represents one of the results for planar gate structure in a non-destructive mode. Gate voltage, gate current and saturation current for different voltage supplies of the gate-driver (V_{driver}) are illustrated.

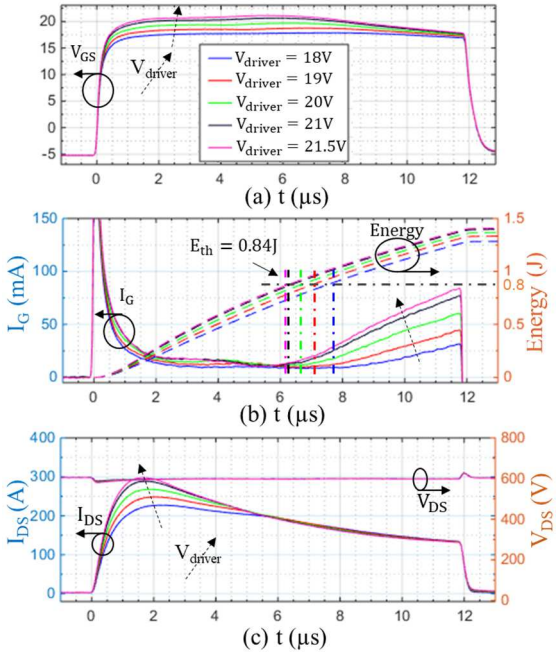


Fig. 2. Experimental waveforms in controlled short-circuit operation. (V_{DS} = 600V ; V_{driver} = ⟦18V; 21.5V⟧; T_{case} = 25°C; R_G = 47Ω; (a) Gate-source voltage. (b) Gate-source current (c) Drain-source current (saturation current) and drain-source voltage.

Fig. 2a clearly show a decrease of the gate to source voltage during the short circuit which is more significant for high gate driver supply voltage. Fig. 2b, shows that this drop voltage is directly related to a high gate leakage-current through the external gate-resistor. This property is therefore directly conditioned by electric field stress in the oxide combined with high temperature in the channel. The same figure reveals that the rise of this leakage current begins for the same thermal energy dissipated in the die whatever the voltage applied by the gate driver. These observations thus highlights a new criterion of threshold energy (here $E_{th} \cong 0.84J$ or $E_{th}/S_{active\ die} = 5.9J/cm^2$). It is clear that such a great and dynamic value of the gate leakage-current (several dozens of mA in a few microseconds) is an opportunity to imagine a fully integrated protection in the gate-driver without measuring the drain-source high voltage.

B. Damaged gate and reverse elements

The physical origin of the gate leakage-current is still under study by authors, but it is assumed to be related to indirect tunneling effect at medium electric field and high temperature (Schottky emission). This topic will not be presented in this article. However, a gate-damaged phenomenon following repeated short-circuits under nominal operating gate voltage-bias and nominal or reduced operating drain-source voltage is presented.

Fig. 3a highlights that for a reduced number of cycles and for some devices, the gate leakage-current increases irreversibly with the repetition of SC cycles and can be observed permanently as shown on Fig.3 before short-circuit event at cycles 38 and 39 when a negative gate to source voltage is applied by the gate driver.

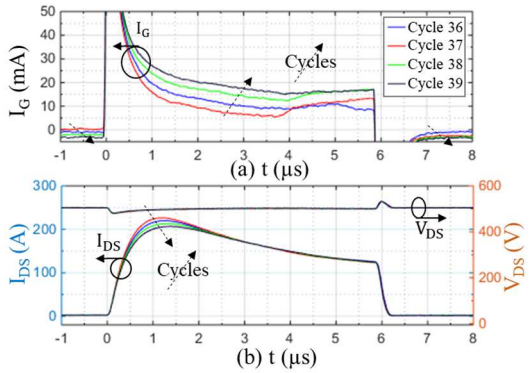


Fig. 3. Permanent degradation of the gate during repetitive SC operations. Evolution of (a) I_G and (b) V_{DS} and I_D during short-circuit. Each color represents a SC. (V_{DS} = 500V ; V_{driver} = 21V/−5V; T_{case} = 25°C; R_G = 100Ω.

In normal operation, care must be taken with such a permanent gate leakage-current and the risk of depolarization of the gate-voltage that could occur, in both on-state and off-state, if a high gate-resistor is used.

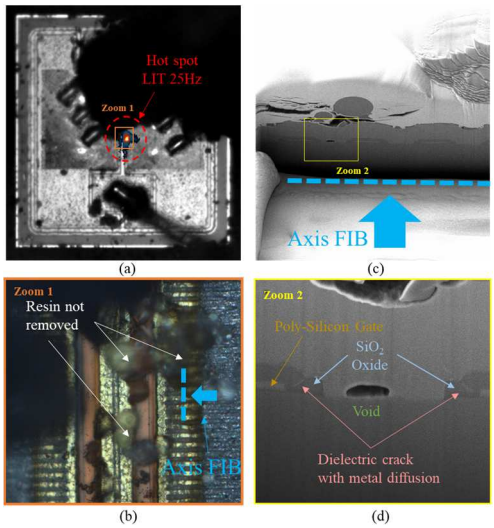


Fig. 4.: (a) Lock-in thermography image of the damaged chip (b) optical image of the hot spot (c) Scanning electron microscope images of the damaged gate zoom (d) zoom.

It is then interesting to make a link between this electrical gate-damaged signature and a physical analysis of the die. Using lock-in thermography, Fig. 4 a reveals a main current path at the center of the die with a focus point along the central gate finger. Fig. 4d shows that this current path probably results to the formation of cracks between the Al top metal and gate-polysilicon through the $Si0_2$ oxide, some of which are filled with metal. In Fig. 4 (d) voids can be seen and are probably caused by the metal displacement due to partial and local reflow of metallization at high temperature.

III. ELECTROTHERMAL MODELLING

Thermal and electro-thermal modelling of the die is an essential topic in extreme operations in order to correlate electrical signatures of ageing with die temperature, particularly in the region close to the gate-oxide.

A. Electrical modelling of the gate-leakage current

A first step concerns the electrical modelling of the gate-leakage current as a function of the dissipated thermal energy and which can be parameterized by the drain-source voltage value which also has an influence on the electric field in the gate oxide. In anticipation of a physical model being studied, a numerical model based on the fitting of a response surface in Matlab™ is proposed. The shape of the model is given by relations (1), (2) and (3).

$$I_g = a_1(E_n).V_{GS} + a_2(E_n) \quad (1)$$

$$a_1(E_n) = p_{01} + p_{11}E_n + p_{21}E_n^2 \quad (2)$$

$$a_2(E_n) = p_{00} + p_{10}E_n + p_{20}E_n^2 + p_{30}E_n^3 \quad (3)$$

where, E_n is the dissipated energy given by the integration of the product V_{ds} by I_{ds} for $E > E_{th}$ and $(p_{00}, p_{01}, \dots)$ are linear functions of the drain to source voltage. Functions values are given in table I after a parametric identification.

I. ESTIMATED FACTORS FUNCTION OF V_{DS}

p00	$174.2161 - 0.5505.V_{ds}$
p10	$192.8417 - 0.5720.V_{ds}$
p01	$-11.8436 + 0.0356.V_{ds}$
p20	$52.8609 - 0.1482.V_{ds}$
p11	$-13.7143 + 0.0386.V_{ds}$
p30	$-0.9317 + 0.0026.V_{ds}$
p21	$-4.1480 + 0.0111.V_{ds}$

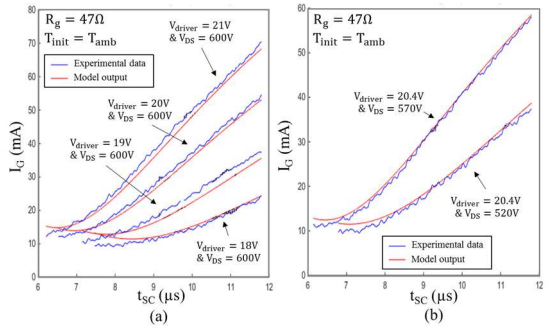


Fig. 5. Electrical gate leakage-current modelling after parametric identification and comparison with experimental results.

Fig. 5a shows the very good matching of the model to the measurement curves of the device for different driver voltages while Fig. 5b proves the robustness of the proposed model with drain to source voltage.

B. Electrothermal modelling

A second step concerns the electro-thermal modelling of the device in order to obtain an estimation of the temperature near the oxide region. Due to the very fast transient regime, it is assumed that the temperature of the upper face of the chip does not significantly evolve. The heat is thus confined into the chip. Assuming an homogeneous power density (W/m^2) and neglecting 2D effects, a distributed 1D model of the chip is sufficient [10].

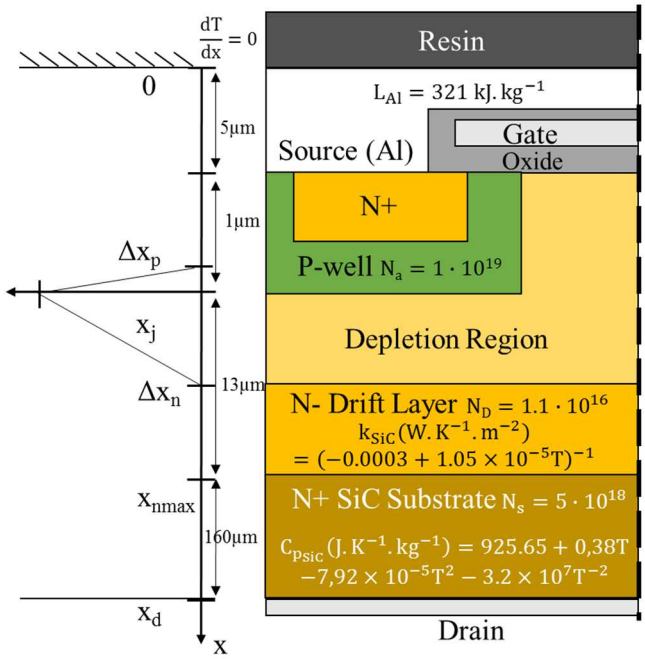


Fig. 6. 1D thermal model of the SiC MOSFET including the doping layers and the thermal sensitive laws used.

The proposed model is depicted in Fig. 6 : N+, N- and P+ layers of the device are discretized. Thereafter, the electric field in the depletion regions P+ / N- is calculated and distributed using the Poisson's law, the doping concentration values in these layers [11] and the total drain-source voltage across the device. The width and doping of the N- layer has been estimated assuming that this drift layer is completely depleted for $V_{DS} = V_{BR}$.The power density (W/m^3) is then calculated for each geometry and each time step by the scalar product between the local electric field and the instantaneous current density as given by relation (8) [4].

$$Q(x,t) = \frac{E(x) \cdot I_{DS}(t)}{S_{chip}} \quad (4)$$

where E(x) is the electric field in the depletion region, $I_{DS}(t)$ the drain current in short-circuit operation, S_{chip} the active area of the chip and Q(x,t) the power density (W/m^3) dissipated within the chip.

Q(x,t) is the source term used with 1D heat equation in Comsol™ to numerically obtain the space-time distribution of the temperature rise within the chip. $I_{DS}(t)$ is derived from the drain-source electrical model part (see in the second part of the flowchart in Fig. 7) and the chip is thermally isolated at the boundary conditions except to the bottom surface where ambient temperature is fixed. To improve the accuracy and the validity range of the model the temperature dependence of the thermal conductivity and mass heat of SiC as well as the phase transition energy of the Al top-metal have been modelled.

The flowchart of the electro-thermal calculation of the temperature is summarized in Fig. 7. Note that a Cauer thermal model with R_{th}, C_{th} distributed circuit elements has also been used in a circuit simulator in order to estimate the temperature and the results of this model has been confirmed with the COMSOL model [12]. In this chart, the first part is dedicated to the thermal calculation alone whereas the second part is devoted to the calculation of time and temperature dependent electrical variables $I_{ds}(t, T_j)$ and $I_{gs}(t, T_j)$ of the electrical model in short-circuit operation. The 1D thermal model and the electrical model are coupled with the maximum junction temperature calculated at the interface of P+/N- layers. This set constitutes a real 1D electro-thermal model.

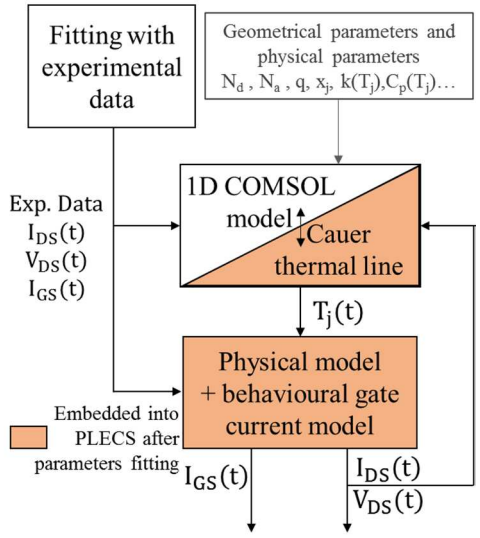


Fig. 7. Flowchart of the SiC MOSFET Electrothermal model building.

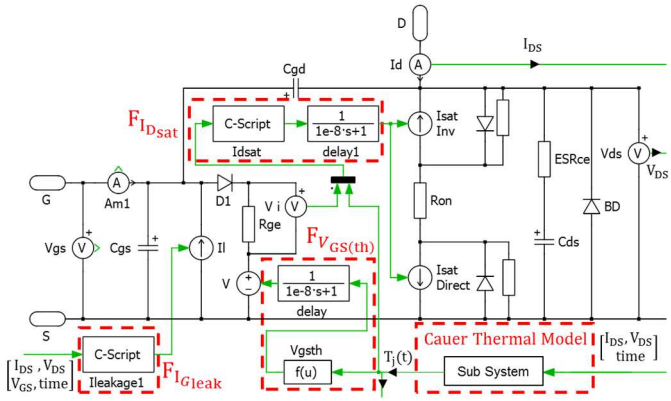


Fig. 8. Proposed 1D SiC MOSFET electro-thermal model in PLECS™ software.

Fig. 8 depicts the electro-thermal model defined in PLECS™ software. In this model, all the electrical parameters are dependent to T_j which is estimated from the 1D thermal model. V_{gsth} is the threshold voltage included in the block $F_{VGS(th)}$, and I_{sat} is the saturation current included in the block F_{IDsat}. A controlled current source was included as an equivalent two-pole device in parallel with the gate-source to emulate the gate leakage current as described in section II. The temperature modelling is given by the following relations (5), (6) and (7), well known for the MOSFET device, especially the Matheissen's law of the global electron mobility in the channel [13].

$$I_{Dsat}(T_j) = \frac{K_{gm}(T_j)}{2} \cdot \left(V_{gs} - V_{gs(th)}(T_j)\right)^2 \quad (5)$$

with :

$$K_{gm}(T_j) = \frac{\mu_n(T_j) \cdot C_{ox} \cdot Z}{L} \quad (6)$$

$$\mu_n(T_j) = \frac{\mu_{a0}\left(\frac{T_j}{T_0}\right)^a}{1 + \frac{\mu_{a0}}{\mu_{b0}}\left(\frac{T_j}{T_0}\right)^{b-a} + \frac{\mu_{a0}}{\mu_{c0}}\left(\frac{T_j}{T_0}\right)^{c-a}} \quad (7)$$

Physical parameters have been fitted in relation to the overall experimental drain – source current behavior to : a=1.48, b=4.8 and c=2.56.

In a first step, x_1, x_2 and K_{gm}(Tj) were fitted from different electrical results using the *fit* function in Matlab over the range [300K, 1300K]. In a second step, a, b and c thermal sensitivity coefficients were numerically fitted to extract the mobility function over the previous range. Results are presented in table II.

II. FITTED THERMAL SENSITIVITY COEFFICIENTS

x_1	x_2	$\frac{\mu_{a0} \cdot C_{ox} \cdot Z}{2L}$	$\frac{\mu_{a0}}{\mu_{b0}}$	$\frac{\mu_{a0}}{\mu_{c0}}$
0.025	15.4	2.325	0.789	$1.2 \cdot 10^3$

Fig. 9 provides an overview of the validity of the electro-thermal model in relation with the experimentation over a wide range of gate voltage-bias and temperature. Transient simulated gate leakage-current, drain saturation current and dissipated energy are compared with experimental curves and prove the validity of the electrothermal model. The thermal model will be used in the next section to estimate the temperature in failure mode.

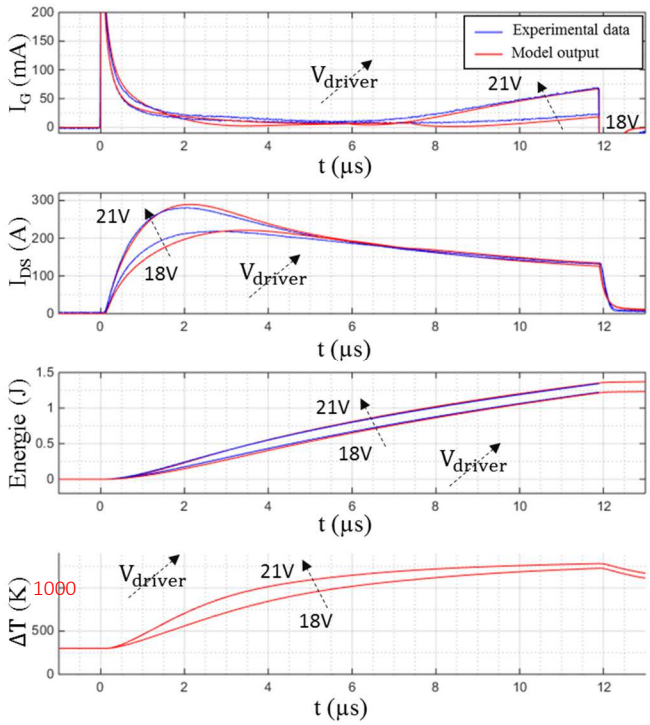


Fig. 9. Validation of the proposed PLECS 1D electrothermal model for two gate voltage-bias (@Vds=600V, Tj_{init}=298,15K (25°C) and R_{gate} = 47Ω).

IV. Fail-to-Open Mode Properties

If the short-circuit is not detected in time or too late, the component begins an irreversible process until failure. The knowledge of the electrical failure mode is important for a system approach around the device. All silicon power devices present a fail-to-short mode and additional fuses or breaker must be introduce on the DC supply of the converter to keep application requirements safe of operation. It is shown in this section that the SiC MOSFET failure mode can be the same as the silicon or an opposed one, under certain conditions. Fig. 10 shows a permanent short-circuit obtained by a long pulse of the gate control with a low DC voltage (225V). For V_{DS} = 300V the saturation current exhibits a thermal runaway after 35µs which is also visible on the gate leakage-current by a great slope variation. This fast thermal dynamic is followed by the chip fusion and a fail-to-short (FTS) drain-source mode. The component cannot sustain voltage under these conditions after failure. It is remarkable to observe that for a low reduction of the drain-source voltage V_{DS} to 225V during the short-circuit operation, the thermal runaway disappears leading to a short between the gate-source electrodes and then a safe turn-off of the channel current. It can be noted that the component can sustain the total voltage under these conditions after failure, such a behavior is named fail-to-open (FTO) mode. Most SiC MOSFET components present this failure mode on condition that a voltage derating and therefore a power dissipation derating is applied during the short-circuit event.

Fig. 11 highlights the gate area failure in FTO mode. A current focalization appears between the end of a gate finger and the source Al top-metal [14]. It is very likely that this path is produced by the metal fusion between the two electrodes below the nitride or polyimide passivation on the die. However this interpretation should not exclude either the presence of cracks under the top metal in the thickness of the oxide as presented in Fig. 4. The range of the gate-source resistance in FTO mode is typically between 100mΩ and 10Ω which means that the component could still be controlled if a great gate current could be supplied by the driver or if an additional gate resistor is included limiting the overload gate-current.

To better understand the physical origin of the FTO mode occurrence and the selectivity between FTO and FTS modes, the transient thermal model presented in section III is used. Considering the same instantaneous power density from the experiment, Fig. 12 clearly shows a threshold temperature above which the thermal runaway rapidly produces FTS mode. Below this threshold, FTO mode is likely to occur when the thermal dynamics are slow enough to allow the top metal to diffuse and form a stable metallic short-circuit between the gate and the source. It is therefore possible to define a power density threshold to select between these two failure modes. Most components today require a strong voltage derating and therefore in power density to select the FTO mode. The work in progress by the authors now focuses on a particular component that would allow this mode without any voltage derating.

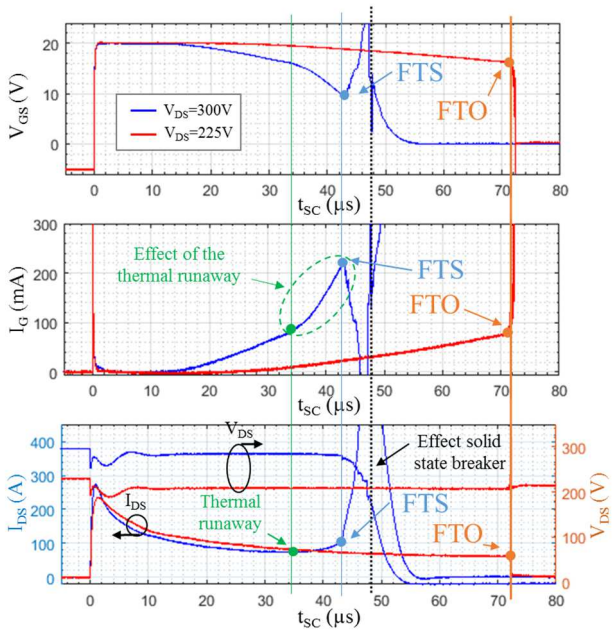
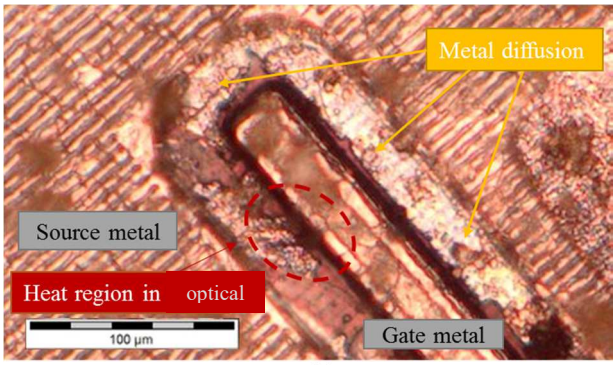
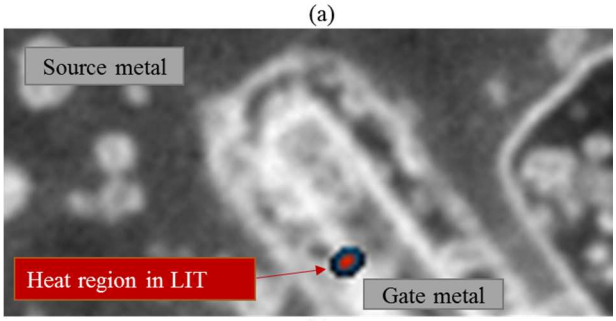


Fig. 10: Experimental waveforms during short-circuit (V_{DS} = 225/250V, $V_{buffer(on/off)}$ = +20V/−5V; T_{case} = 25°C; R_G = 47Ω).



(a)



(b)

Fig. 11: Images of the damaged area on the device (a) Optical microscope. (b) Lock-in thermography.

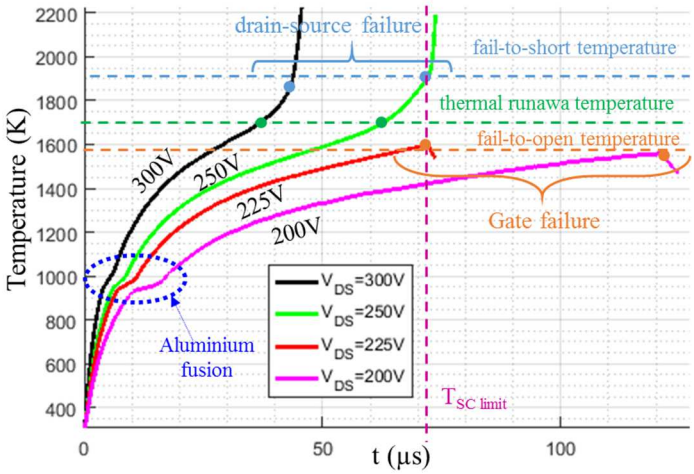


Fig. 12: Estimated junction temperature for differents drain bias.

V. Conclusion

This article highlights two rather poorly known properties of SiC MOSFET in extreme short-circuit operation until failure. Physical understanding elements and electro-thermal modelling approaches are proposed to support the analysis and extract the main conclusions. The first property concerns the occurrence of a high gate leakage-current that can be used for short-circuit detection integrated into the gate-driver without the use of external and intrusive high-voltage components. A permanent gate leakage-current is also visible for repeated cycles causing damage to the gate oxide. The second property concerns the possibility of an atypical drain-source fail-to-open mode provided that a power density derating and therefore a drain-source voltage derating are applied. These two properties combined suggest very useful safety techniques for critical applications. The authors' future work focuses on the implementation of these properties and the study of a component that would present a fail-to-open mode without any voltage derating.

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