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Scaling Trend of CMOS based RF circuits

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Abstract: With the cutting edge of technology, the number of portable devices using wireless equipment is increasing significantly and therefore, design and implementation of high performance 4G digital system is in high demand and challenging task. Radio frequency (RF) circuits are the interface devices between wireless equipment and antenna. In the past, RF circuits were made with large analogue components such as transistors, coils etc. By development of Complementary metal–oxide–semiconductor (CMOS) technology, CMOS transistors came to function. However, scaling of devices was accelerated due to using simple CMOS technologies. The scaling trend was continued therefore current leakage, power consumption usage became undeniable issues, and hence, this review paper is considering the research being took place in CMOS scaling based RF modules in recent years [1-22]. The review paper shows changing parameters in CMOS technology is not efficient solution for transistor fabrication and innovations on materials and structure are required to address the fabrication problems.

With the advance, CMOS based RF technology, high efficient digital system formulated and designed in terms of chip size and low power consumption. Yet the trend showed a narrow improvement until 2003 that the chief technology Officer of IBM Microelectronics announced the scaling is dead [4]. Certainly, in CMOS based RF circuit design, reducing the size of transistor beyond 22nm not only had not sufficient efficiency but also had harm effects on the circuit performance such as power dissipation and lessen the throughput [5]. Therefore, Advanced CMOS technologies are in high demand to overcome the challenging task. There are some concepts such as silicon on insulator (SOI), strained silicon, high-k (advanced dielectric materials), and multi gate transistors that can help the scientist to face with the problems associated with scaling [6, 7].

2. PARAMETERS FOR CMOS BASED RF CIRCUITS

2.1. CMOS RF Performance

Transit frequency \( f_t \) is one the foremost known parameters of transistors. It is defined by drain current divided by gate current when \( v_{ds} \) is zero. In other word \( f_t \) is the frequency where the small-signal-current-gain of device drops to unity while source and drain terminals are grounded.

The impact of parasitic output (parallel) and input (series) of transistor is ignored due to the definition \( v_{ds} = 0 \). This definition is suitable for transistors where has a low drain source small-signal output (conductance\( g_{ds} \)) towards the load (admittance\( g_t \)). However, literatures showed that \( v_{ds} \) in very large scaled CMOS transistors is much higher than the\( g_t \). Hence, small-signal voltage gain is not achievable. The coefficient \( ghm/gds \) (high intrinsic voltage gain) can control and limit the maximum voltage gain in the circuits [8]. As far as researches concerned, this coefficient is not compatible with lots of high-speed structures witch functionally roles on voltage gain.

1. INTRODUCTION

By developing the wireless technologies during recent years, the great impact of wireless equipment can be felt due to amazing growth of mobile devices. In other words, wireless circuits have become the fundamental of many telecommunication instruments such as laptops, cell-phones, home security tools, industry monitoring goods and biomedical tools [1-3]. Clearly, the wireless equipment is consisting of radio RF circuit, which is the interface between antenna and wireless equipment. In conventional RF products, bipolar and gallium arsenide (GaAs) components have been used in the variant frequency ranges, however, recently the CMOS technology is able to make RF circuits for any of this frequency ranges.
Hence, using just \( f_t \) for designing the RF circuits is meaningless due to having large \( g_{ds} \). Therefore in addition to \( f_t \) another parameter is required to characterize the design. One parameter is \( \frac{g_m}{g_{ds}} \) coefficient and another one is maximum frequency of oscillation \( (f_{max}) \) which is the frequency where power gain drop to 0 dB [9]. \( f_{max} \) is vary from \( f_t \).

2.2. CMOS Scaling

The trend of scaling CMOS circuits from 350\( \text{nm} \) to 10\( \text{nm} \) is shown in Fig.1 (1997 - 2020).

From 350\( \text{nm} \) until around 45\( \text{nm} \), equ. (1) is utilizing for scaling:

\[
f_t \approx \frac{1}{L_g}
\]

where \( L_g \) is correspond to length of the gate. Equ. (1) provides the concept of reverse relation between length of the gate and transit frequency due to saturation effect and short length channel.

Equ. (1) is changed to \( f_t \approx \frac{1}{L_g} \) around 45\( \text{nm} \) and for more scaling (around 10\( \text{nm} \)) the equation will be \( f_t \approx \frac{1}{L_g^n} \) where \( 0 < n < 1 \). Hence, decreasing the gate length is not efficient way for designing the transistors by scaling below 45\( \text{nm} \) due to high electrical field in short channel.

To avoid the effect of electrical field in the channel the efficient way is to decrease \( V_{ds} \) alternatively by reducing \( L_g \); until \( V_{ds} \) reach approximately 0.5V. Lessen \( V_{ds} \) has some disadvantages such as reducing the out coming power of RF. In addition, since 250\( \text{nm} \) to 45\( \text{nm} \), the coefficient \( \frac{g_m}{g_{ds}} \) is decreasing by 34% and worst case is that by reducing the scale to 10\( \text{nm} \) the coefficient \( \frac{g_m}{g_{ds}} \) descend to unity approximately that is harm for RF system module. Furthermore, there is fabrication problem of 10\( \text{nm} \) scaling such as gate oxide layer thickness; It must be below 1\( \text{nm} \) to control the channel sufficiently, which cause the current leakage between gate and source or drain and lead to more power dissipation[10]. Hence, this paper results by changing this parameters it is impossible to design an efficient RF amplifier and innovations on materials and structure are required to address the problems.

3. ADVANCED TECHNIQUES FOR CMOS SCALING USING IN RF MODULES

As it discussed, scaling CMOS is a challenging task and there are several techniques to mitigate the issues as such: A) Strain Silicon (SiS)

Strained silicon is a practical way to improve electron and hole motilities of the channel region. This method improves the transistor current (\( I_{on} \)), and therefore, helps factories to scale the transistors by keeping the gain performance. Power consumption reduction of CMOS transistors using SSI technique leads to reduce power dissipation [11, 12].

When silicon atoms are stretched more than common inter atomic length, the generated structure is called strained silicon. This structure is created by deposition a small layer of silicon-germanium (SiGe) on the surface of the silicon to make the virtual layer, then a thick layer of Si are grown on the virtual surface to make the strained structure, which has higher carrier mobility. Fig.2 shows the strained silicon structure.

![Illustration of strained silicon structure](image)

Lower fan-out, lower power consumption and higher speed are some advantages of this structure due to having more carrier mobility [13].

3.1. B) Silicon on isolation (SOI) Technology
SOI is an efficient method for CMOS scaling. In this method, thin layer of insulator such as separates active layer and substrate from each other SiO$_2$. Therefore, this combination makes the transistor relax of enhancing $L_g$ during scaling [14]. SOI offers high performance due to separation of active layer and substrate, high resistivity can be selected without any affect on $V_{th}$, low power consumption due to reduce the leakage current and higher speed compared to traditional silicon components [15]. Fig.3 presents the SOI structure.

However, tunneling in a small layer of oxide can cause the current leakage when, scaling down ($T_{ox}$) the transistor. Leakage can cause higher noise generation in circuit and reduce the performance of RF circuit. This problem is addressing by using high dielectric materials (high barrier gate oxide) such as zirconium (ZrO$_2$) or hafnium oxide (HfO$_2$). Unfortunately, impurities and traps affect these materials, which influence the RF performance. Therefore, these materials are not suitable for using in RF circuits [16, 17].

3.2. C) Complementary Of SOI and Strained Silicon

The complementary structure has both advantages of SOI and strained silicon due to effect of insulator under the active region. Insulator separate active layer and buried insulator under active channel from each other, therefore, these regions do not have any effect on the other one [18].

There are many structures, which used both strained silicon and SOI techniques together. Most of the structures are based on the epitaxial growth of SiGe followed by another layer to generate SiGe-on insulator structure. Then strained silicon is grown on the surface to make the finale structure [19, 20]. Fig.4 shows the structure of the strained silicon on SiGe insulator.

3.3. D) Multi-gate CMOS Transistor

The popular technique that influences the performance, scaling and speed of the CMOS based RF modules is multi-gate transistor. Fig.5 shows the double gate (DG) metal–oxide–semiconductor field-effect transistor (MOSFET). Clearly, the structure has two gates, one at bottom and another one at top. By acting field at both sides, controlling the transistor has been take placed efficiently. In addition, it is possible for more scaling the transistor, when two channels are interfaced in parallel and more current can be flown through the channel at given gate source voltage.

In double gate transistors, delay of both gates must be perfectly the same to modulate the channel in phase. It is difficult to fabricate these transistors horizontally. This issue can be addressed by applying laterally aligned gates. A upright illustration of this issue is DG-Fin-FETs and vertical double gates [22] which can be seen in Fig. 5a and 5b. By full depletion of Fins, more $g_m/g_{ds}$ is achievable.
More enhancements are reachable by using tri-state or ring gate structures, which is presented in Fig.6a and 6b. These processes are costly instead.

To conclude, Table 1 shows comparison between Strained Silicon, SOI and strained silicon-OI. As shown in Table 1, strain silicon on insulator has benefits of both strain silicon and SOI together. Hence, this technique can be a practical method to make an efficient RF module. Beyond that performance of all these techniques is improved by multi gate method.

### Table 1: Comparison Among Strained Silicon, SOI and strained silicon-OI

<table>
<thead>
<tr>
<th>Properties</th>
<th>SOI</th>
<th>Strain silicon</th>
<th>Strain silicon SOI</th>
</tr>
</thead>
<tbody>
<tr>
<td>Circuit speed</td>
<td>fast</td>
<td>Very fast</td>
<td>Very fast</td>
</tr>
<tr>
<td>Power consumption</td>
<td>very low</td>
<td>low</td>
<td>Very low</td>
</tr>
<tr>
<td>Capacitance parasitic</td>
<td>low</td>
<td>high</td>
<td>low</td>
</tr>
<tr>
<td>Current leakage</td>
<td>low</td>
<td>high</td>
<td>low</td>
</tr>
<tr>
<td>Channel length scaling</td>
<td>good</td>
<td>good</td>
<td>good</td>
</tr>
<tr>
<td>Innovation</td>
<td>Structure innovation</td>
<td>Material innovation</td>
<td>Both material and structure innovation</td>
</tr>
</tbody>
</table>

### References


