Parallel Amplifiers Technique for LNA Design

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Abstract

A new design method for low noise amplifier (LNA) based on using parallel amplifiers to improve the linearity and output power is proposed in this paper.
Noise parameters including minimum noise figure and optimum noise impedance and R_n (sensitivity coefficient) of this topology are calculated. The effect of parallel path to overall noise figure(NF) and input matching is also considered. Electro magnetic (EM) simulation result for the designed 10-12 GHz LNA with the 0.1-µm pseudomorphic GaAs HEMT model is reported to support proposed theories.

Analysis

Noise model of two parallel paths of IDCS amplifiers is shown in Fig. 1.
Through the calculation of the transfer function of noise sources, noise parameters can be obtained.

$$NF_{\min} = 1 + \frac{2\gamma R_g C_{gs}^2 \omega^2}{g_m} - 2\gamma C_{gs} M \omega^2 + \frac{4\gamma C_{gs}^2 \omega^2}{g_m} \sqrt{\frac{R_g^2}{4} + \frac{M^2 g_m^2}{4C_{gs}^2} + \frac{g_m R_g}{4C_{gs}^2 \omega^2} - M\frac{g_m R_g}{2C_{gs}}}$$

$$Z_{s,opt} = \sqrt{\frac{R_g^2}{4} + \frac{M^2 g_m^2}{4C_{gs}^2} + \frac{g_m R_g}{4C_{gs}^2 \omega^2} - M\frac{g_m R_g}{2C_{gs}}} + j\frac{1}{2}\left(\frac{1}{C_{gs}\omega^2} - L_s + M\right)\omega$$

$$R_{n\text{-}p}\Big|_{M=0} = \frac{1}{2}R_{n\text{-}s} = R_g + \frac{\gamma}{g_m}(1 - L_s C_{gs}\omega^2)^2$$

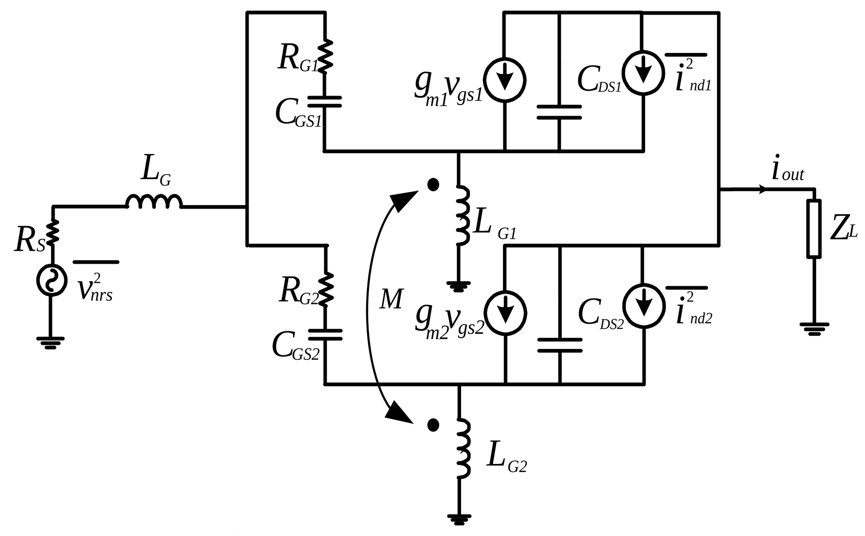


Fig1. Parallel amplifiers noise model

Parallel amplifier technique is known for linearity enhanced behavior

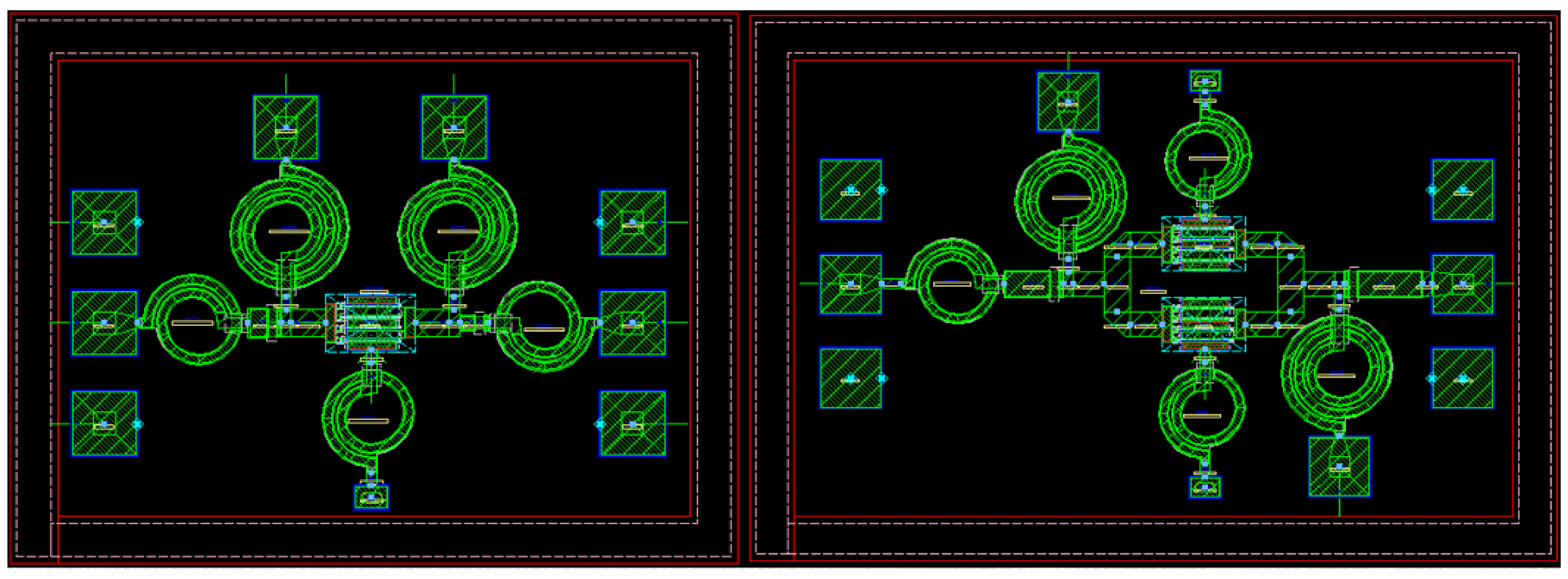
Theoretical calculations show this method can also be practical for desensitized LNAs

Low sensitivity causes this method to be considered as a wideband LNA topology

Results

Two different LNA are designed with bandwidth of 2 GHz for input and output matching better that -10 dB and 8 dB gain with the 0.1-µm pseudomorphic GaAs HEMT model.
First LNA is a single path amplifier and second one is a parallel amplifier with two similar paths.
Results shows that :

- ✓ S_{11} and S_{22} of parallel amplifier are better than single path LNA.
- ✓ It also represents that R_n of parallel amplifier is less than single path and contrary to what we expected it causes NF of this amplifier to be lower.
- ✓ Parallel LNA topology can improve NF because of a second order factor. R_n minimization causes amplifier to have less sensitivity to source impedance and decrease LNA's dependency to input matching circuit.
- ✓ The output power versus input power behavior of both amplifiers shows that p-1dB of parallel amplifier is 3-dB better than single path LNA.



(a) (b)

Fig2. Layout micrography of LNAs (a) Single stage LNA (b) Parallel LNA

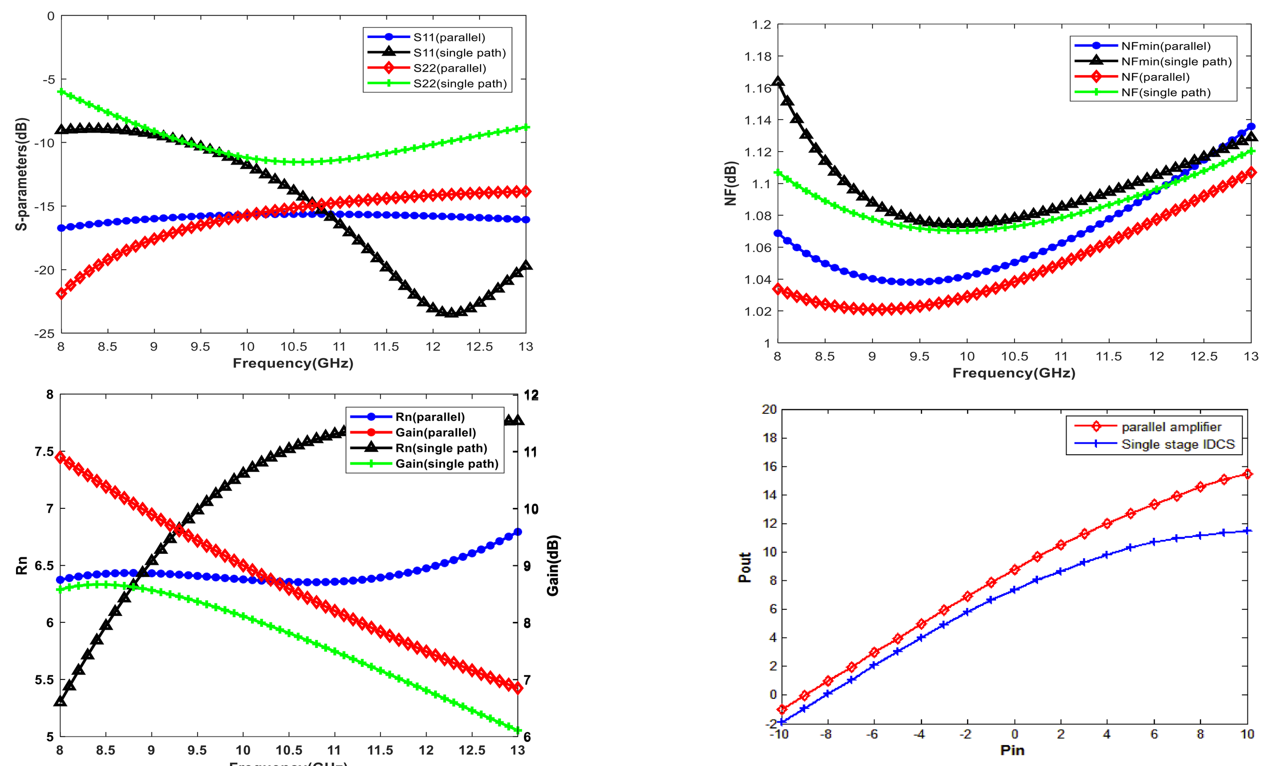


Fig3. S-parameter, Gain, Rn, NF and P1-dB Result of designed LNAs

Conclusions

- The parallel LNA exhibits the gain of 11 dB at 8 GHz with 3-dB gain bandwidth of 8-11.5 GHz, with input and output impedance matching better than -14 dB
- This topology can be considered as wideband topology with low sensitivity to source impedance and high P1-dB.
- Simulation results shows NF_{min} almost remains the same.
- On contrary to what we expected of NF to increase due to input divider's loss it decreases because of reduction in amplifiers sensitivity to input impedance.

References

[1] A. Alizade, M. Forounchi and A. Medi, ”On Design of Wideband Compact-Size Ka/Q-Band High-Power Amplifiers”,IEEE Trans. Microw. Theory Tech., vol. 64, no. 6, pp. 1831–1842, 2016.
[2] S. Narayanan, ”Application of Volterra series to intermodulation distortion analysis of transistor feedback amplifies”, IEEE Trans. Microw. Theory Tech., vol. 17, pp. 518–527, 1970.
[3] T. W. Kim, B. Kim and K. Lee, ”Highly linear receiver front-end adopting MOSFET transconductance linearization by multiple gated transistors”,IEEE Journal of Solid-State Circuits, vol. 39, pp. 223–229, 2004.
[4] Y. Ding and R. Harjani, ”A +18 dBm IIP3 LNA in .35 um CMOS”, IEEE International Solidstate Circuits Conference, 2001.
[5] T. S. Kim and B. S. Kim, ”Post-linearization of cascode CMOS LNA using folded PMOS IMD sinker”, IEEE Microwave Wireless Component Letters, vol. 16, pp. 182–184, 2006.
[6] N. Kim, V. Aparin, K. Barnett, C and Persico, ”Acellular-bandCDMA 0.25 um CMOS LNA linearized using active post-distortion”,IEEE Journal f Solid-State Circuits, vol. 41, pp. 1530–1534, 2006.
[7] H. Zhang and E. Snchez-Sinencio, ”Linearization Techniques for CMOS Low Noise Amplifiers: A Tutorial”,IEEE Trans. Circuits Syst., vol. 58, pp. 22-37, 2011.
[8] B. Razavi, ”RF Microelectronics”, Prentice Hall, 1998.
[9] J.Kim, S.Hoyos and J.S.Martinez, ”Wideband Common-Gate CMOS LNA Employing Dual Negetive Feedback With Simultanous Noise, Gain, and Bandwidth Optimization”,IEEE Trans. Microw. Theory Tech., vol. 58, pp. 2334–2351, 2010.
[10] H. G. Han, D. H. Jung and T. W. Kim, ”A 2.88 mW +9.06 dBm IIP3 common-gate LNA with dual cross-coupled capacitive feedback”, IEEE Trans. Microw. Theory Tech., vol. 63, pp. 1019–1025, 2015.
[11] A. Liscidini, M. Brandolini, D. sanzogni and R. Castello, ”A 0.13 um CMOS front-end for DCS1800/UMTS/802.11b-g with multi-Band positive feedback low noise amplifier”, in IEEE VLSI Circuits Symp. Dig. Tech. Papers, 2005.
[12] A. Liscidini, G. Martini, D. Mastantuono and R. Castello, ”Analysis and design of configurable LNAs in feedback common-gate topologies”, IEEE Trans. Circuits Syst. II: Express Briefs, vol. 55, pp. 733–737, 2008.
[13] A. Nieuwoudt , T. Ragheb , H. Nejati and Y. Massoud, ”Numerical design optimization methodology for wideband and multi-band inductively degenerated cascode CMOS low noise amplifiers”, IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 56, no. 6, pp. 1088–1101, 2009.
[14] D. K. Shaeffer, ”A 1.5-V, 1.5-GHz CMOS low noise amplifier”, IEEE J. Solid-State Circuits, vol. 32, no. 5, 1997.
[15] M. S. Heins, J. M. Carrol, M. KAO, J. Delaney and C. F. Campbell, ”X-band GaAs mHEMT LNAs with 0.5 dB NF” ,Microwave Symposium Digest, vol. 1, pp. 149–152, 2004.
[16] T. Nguyen, C. Kim, G. Ihm, M. Yang and S. Lee, ”CMOS low noise amplifier design optimization techniques”, IEEE Trans. Microw. Theory Tech., vol. 52, pp. 1433–1443, 2004.

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