Hybrid-DBT: Hardware Accelerated Dynamic Binary Translation
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Overview of Hybrid-DBT

→ The VLIW core executes applications.
→ The L1 Instr. cache stores RISC-V instructions.
→ The HW Decoder decodes RISC-V into VLIW ISA.
→ The DBT Processor analyses and optimizes RISC-V binaries, using the HW Accelerators.
→ Those binaries are stored in the Translation Cache.

Hybrid-DBT: Hardware Accelerated Dynamic Binary Translation

Heterogeneous multi-core systems present key advantages compared to their homogeneous counterparts. They allow a dynamic balancing between performance and energy efficiency. Current implementations are limited to a single ISA to easily migrate tasks from one core to the other.

To further improve the current systems, specialized cores such as VLIWs can be added. To handle the ISA differences between the cores, a layer of Dynamic Binary Translation is associated to the specialized cores. DBT translates the instructions from a given ISA to another one as they are being executed on the target core. To lessen the overheads introduced by the use of DBT, we present Hybrid-DBT: a HW/SW Co-Designed DBT system which uses several hardware accelerators to reduce the costs of DBT [3][4].

References


Contacts

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https://github.com/sroicki/HybridDBT