Heterogeneous multi-core systems present key advantages compared to their homogeneous counterparts. They allow a dynamic balancing between performance and energy efficiency. Current implementations are limited to a single ISA to easily migrate tasks from one core to the other. To further improve the current systems, specialized cores such as VLIWs can be added. To handle the ISA differences between the cores, a layer of Dynamic Binary Translation is associated to the specialized cores. DBT translates the instructions from a given ISA to another one as they are being executed on the target core. To lessen the overheads introduced by the use of DBT, we present Hybrid-DBT: a HW/SW Co-Designed DBT system which uses several hardware accelerators to reduce the costs of DBT [3][4].

Hyper-Perf CPU
Low-Power CPU
Low-Power CPU
VLIW D B T

## Context - Heterogeneous Multi-cores

![Graph showing performance vs. energy efficiency for different execution modes.](image)

- **Out-of-Order (ISA 1)**
- **In-Order (ISA 1)**
- **VLIW (ISA 2)**
- **Power consumption (mW)**
- **Performance (Gops)**

### Translation flow

1. **Opt. level 0**
   - Native Binaries
   - RISC-V

2. **Translation**
   - Instruction Translation
   - No ILP
   - VLIW Binaries
   - 01000000010

3. **IR**
   - Solving branches
   - Updates VLIW binaries
   - Exploit ILP

4. **IR Builder**
   - Insertion of profiling instr.
   - Building CFG

5. **IR Scheduler**
   - Inter-block optimization
   - Data flow graphs

6. **Data & Control flow graphs**
   - Details on the Intermediate Representation (IR)
   - In-memory data

## Experimental Results

- **Improvement vs. software**
  - First-Pass Translation
  - IR Generation
  - IR Scheduling

- **Performance**
  - In-Order
  - Hybrid-DBT
  - OoO

- **Energy efficiency**
  - Hybrid-DBT
  - OoO

## References

2. Booga et al. *Denver: NVidia’s First 64-bit ARM Processor*
3. Rokicki et al. *Hybrid-DBT: HW/SW DBT targeting VLIW*
4. Rokicki et al. *Supporting Runtime Reconfigurable VLIW’s Cores through Dynamic Binary Translation*

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