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To cite this version:
Simon Rokicki, Erven Rohou, Steven Derrien. Hybrid-DBT: Hardware Accelerated Dynamic Binary Translation. RISC-V 2019 - Workshop Zurich, Jun 2019, Zurich, Switzerland. pp.1. hal-02155019

HAL Id: hal-02155019
https://hal.archives-ouvertes.fr/hal-02155019
Submitted on 13 Jun 2019

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Hybrid-DBT: Hardware Accelerated Dynamic Binary Translation

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Context - Heterogeneous Multi-cores

Heterogeneous multi-core systems present key advantages compared to their homogeneous counterparts. They allow a dynamic balancing between performance and energy efficiency. Current implementations are limited to a single ISA to easily migrate tasks from one core to the other.

To further improve the current systems, specialized cores such as VLIWs can be added. To handle the ISA differences between the cores, a layer of Dynamic Binary Translation is associated to the specialized cores. DBT translates the instructions from a given ISA to another one as they are being executed on the target core. To lessen the overheads introduced by the use of DBT, we present Hybrid-DBT: a HW/SW Co-Designed DBT system which uses several hardware accelerators to reduce the costs of DBT.

Previous work on HW/SW Co-Designed Machines:

→ Transmeta Crusoe (x86 on VLIW) [1]
→ NVIDIA Denver (ARMv8 on VLIW) [2]

Overview of Hybrid-DBT

→ The VLIW core executes applications
→ The L1 Instr. cache stores RISC-V instructions
→ The HW Decoder decodes RISC-V into VLIW ISA
→ The DBT Processor analyses and optimizes RISC-V binaries, using the HW Accelerators.
→ Those binaries are stored in the Translation Cache.

Experimental Results

Translation flow

- The VLIW core executes applications
- The L1 Instr. cache stores RISC-V instructions
- The HW Decoder decodes RISC-V into VLIW ISA
- The DBT Processor analyses and optimizes RISC-V binaries, using the HW Accelerators.
- Those binaries are stored in the Translation Cache.

References


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https://github.com/srokicki/HybridDBT