Hybrid-DBT: Hardware Accelerated Dynamic Binary Translation
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Hybrid-DBT: Hardware Accelerated Dynamic Binary Translation

Simon Rokicki, Erven Rohou, Steven Derrien
Univ Rennes, Inria, CNRS, IRISA

Context - Heterogeneous Multi-cores

Heterogeneous multi-core systems present key advantages compared to their homogeneous counterparts. They allow a dynamic balancing between performance and energy efficiency. Current implementations are limited to a single ISA to easily migrate tasks from one core to the other.

To further improve the current systems, specialized cores such as VLIWs can be added. To handle the ISA differences between the cores, a layer of Dynamic Binary Translation is associated to the specialized cores. DBT translates the instructions from a given ISA to another one as they are being executed on the target core. To lessen the overheads introduced by the use of DBT, we present Hybrid-DBT: a HW/SW Co-Designed DBT system which uses several hardware accelerators to reduce the costs of DBT [3][4].

### Translation flow

- **Opt. level 0**: Native Binaries
- **Opt. level 1**: Instruction Translation
- **Opt. level 2**: IR Builder

Translation flow

**Hardware opt.**

- **IR Builder**
- **IR Scheduler**
- **Building CFG**
- **Inter-block optimization**

**Software opt.**

- **Data & Control flow graphs**
- **Details on the Intermediate Representation (IR)**

**Univ Rennes, Inria, CNRS, IRISA**

**Simont-Rokicki@irisa.fr**

https://github.com/srokicki/HybridDBT

### References


### Experimental Results

- **Performance**
- **Energy efficiency**

### Contacts

simon.rokicki@irisa.fr

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**System**

- High-Perf CPU
- Low-Power CPU
- VLIW DBT

**NVidia Denver (Armv8 on VLIW)**

**Transmeta Crusoe (x86 on VLIW)**

**Large enough Executed often**

- Data & Control
- In-memory data
- Details on the Intermediate Representation (IR)