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4H-SiC P-N junctions realized by VLS for JFET lateral structures

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Device integration is a key step for industrial and scientific research to improve performance and reliability of power electronics. Silicon carbide (SiC) offers excellent properties in terms of maximum electrical field, cooling effort and temperature operation. By integrating in SiC, the size of converters can be radically reduced inducing faster switching operation with low power losses. Several demonstrators of monolithically integrated SiC active devices such as VJFET and JBS diodes [1] or vertical and lateral BJT [2], have been already fabricated. Nevertheless the high residual doping of SiC substrates and the high resistivity of the p-type layers still block the development of this monolithic technology. During the last years our investigations [3] have revealed that the Vapor-Liquid-Solid (VLS) selective epitaxy can be an interesting method to locally p-type dope SiC, leading to considerable reduction of the p-type resistivity and of the resistance of the ohmic contacts formed on it (with specific resistances as low as 1.3×10^{-6} $\Omega.cm^2$).

For the present work we investigated the possibility of using these P^+ SiC layers obtained by VLS as functional layers in lateral SiC JFET. We fabricated lateral JFET transistors with N and P-type channels integrated monolithically in the same SiC wafer. The VLS P^+ wells were utilized as source and drain for the P-JFET and gate for the N-JFET.

The transistors have been fabricated on commercial 4H-SiC wafers with CVD epitaxial layers grown on N^+ substrate. These CVD epilayers have been used for the N and P-type channels of the JFET (figure 1). The different structures are isolated by dry RIE etching [4]. Compared to the N-JFET structures described in ref [5] we preferred an N^+ substrate instead of a semi-insulating one allowing us to have an additional electrode which can be biased at a fixed potential. The N^+ wells for the gate (P-JFET), source and drain (N-JFET) electrodes are realized by nitrogen ion implantation and 1700°C post-annealing with a C-cap [6]. The P^+ wells are created by VLS buried selective epitaxial growth from Al-Si liquid phase [7]. Transfer Length Methods (TLM) structures were in particular added in order to test the ohmic contacts and the resistivity of the different doped layers (N^+,P^+ and channels). The overall structure including doping and thicknesses of the different layers and a complete technological process will be detailed in the final paper.

The fabricated N and P JFET transistors have been characterized by current-voltage measurements. Typical I_{DS}-V_{DS} characteristics plotted as a function of V_{GS} are presented in figure 2 for both N and P JFET. By comparing with the N-type channel, the resistivity of the P-one is higher due to the poorer mobility but we remark that even in that case we obtain a modulation of the channel resistivity by varying the V_{GS} gate-source bias. Note that the V_{GS} range is positive for the P-JFET and negative for the N-JFET.

Trying to block the N-JFET by increasing the absolute value of V_{GS} (figure 2), we observed a shift of I_{DS}-V_{DS} characteristics from the origin of the spectra. This is due to a premature leakage current through the transistor structure when the V_{GS} is increasing in reverse bias.

I_{GS}-V_{GS} characteristics are presented in figure 3 for a large number of N and P-JFET. Normally in each case the characteristic of a typical 4H-SiC bipolar diode should be obtained. Nevertheless a threshold of ~3V in forward bias is obtained only for the JFET with a P-type channel. Comparing the structure of the two JFET transistors we can observe that between the gate and the source, the P/N junction is formed between the CVD P type channel and N implanted gate well in the case of the P JFET whereas for the N JFET the P/N junction is created directly between the P^+ VLS gate layer and the CVD N-type channel. Thus, it seems that the cause of the premature leakage current observed in the case of N-type JFET is probably the quality of the VLS/CVD interface that is still not compatible with the formation of a perfect bipolar P/N junction. Studies are in progress to solve this problem.

The results we obtained will be discussed further in the final paper comparing with complementary measurements performed on test structures as TLM. The present work revealed mainly that the P^+ VLS layers could already be utilized to improve the resistance access on bipolar and unipolar SiC devices by decreasing significantly the specific contact resistance on P-type SiC layers.

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[1] R. Radhakrishnan and J.H. Zhao, IEEE Electron Device Letters, 32 n° 6 785 (2011).
[2] L. Lanni et al., IEEE Electron Device Letters 35 n°4 428 (2014)
[3] N. Thierry-Jebali et al., Mater. Sci. Forum. 778-780 639 (2014).
[4] M. Lazar et al., Mater. Sci. Forum. 679-680 477 (2011)
[5] K. Fujikawa et al., SEI TECHNICAL REVIEW 61 77·(2006)
[6] E. Oliviero et al., Nucl. Instrum. Meth. B 257 265 (2007)
[7] D. Carole et al, Mater. Sci. Forum. 717-720 169 (2012)

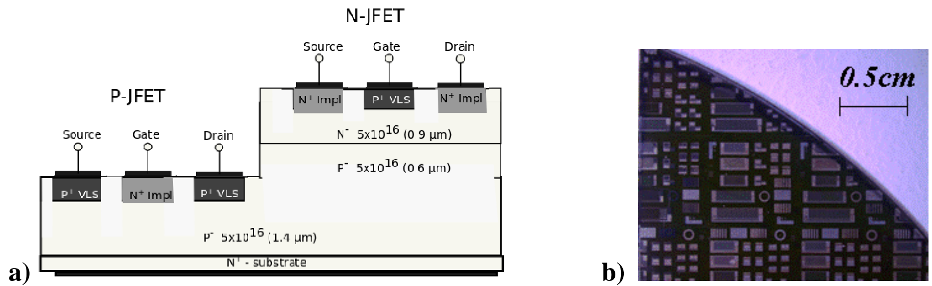

Fig. 1. Cross-sectional structure of the integrated P and N lateral JFET (a), optical micrographs recorded after the technological fabrication process (b)

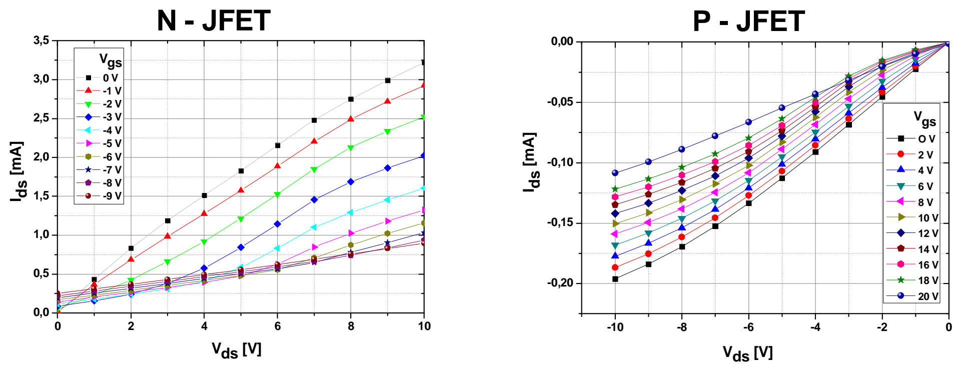

Fig. 2. Typical I_{DS} - V_{DS} characteristics of the N and P JFET fabricated with buried P^+ layers created by VLS selective epitaxy growth.

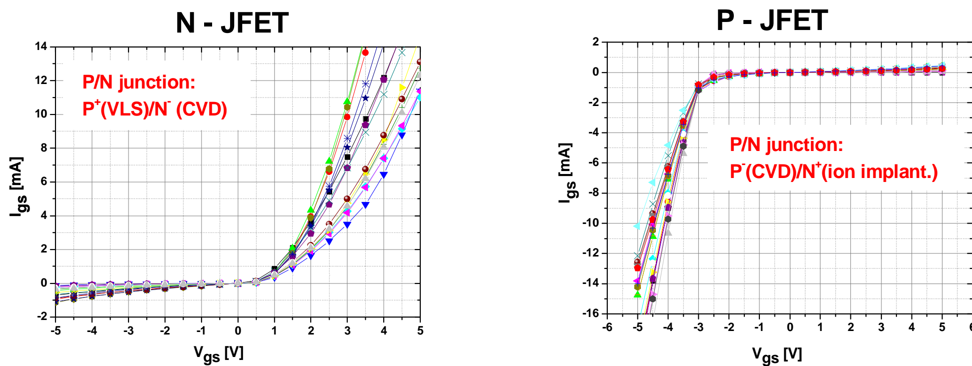

Fig. 3. I_{GS} - V_{GS} characteristics of a consistent number of N and P JFET fabricated with buried P^+ layers created by VLS selective epitaxy growth.