Packaging Solution for SiC Power Modules with a Fail-to-Short Capability

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***Abstract*—Fail-to-short packages, which can still carry current after the failure of their semiconductor devices, are required for HVDC applications. However, all existing solutions are dedicated to silicon components. Here, a fail-to-short package is proposed for SiC devices. Its manufacturing process is described. 4 modules are built and submitted to intense short circuit currents (up to 2000 A). It is found that they offer a stable short-circuit failure mode, providing that the modules are mechanically clamped to prevent separation during the surge current test.**

I. Introduction

High Voltage Direct Current (HVDC) converters rely on the series connection of many power modules. To prevent the failure of a single module from stopping the operation of a whole converter, a fail-to-short behavior is expected [1], so that the failing power modules basically "disappear" from the series string. Fail-to-short power modules have been demonstrated for silicon devices [2], [3], [4]. They are all based on massive interconnects (such as in press-packs [5]), as opposed to the wirebond interconnects used in standard power modules (wirebonds act as fuses, resulting in an open-circuit behavior in case of failure). Schematically, the fail-to-short behaviour is achieved by the rise in temperature of the semiconductor devices up to their melting point, and the subsequent formation of a conductive alloy between the silicon and the surrounding metal interconnects.

The metallurgy of SiC is very different from that of Si, because SiC remains basically inert up to more than 2500 °C. Recently, it has been demonstrated that while SiC devices do not melt in case of failure, the SiC dies shatter and the surrounding metal interconnects can infiltrate in the cracks, forming a conductive path [6]. Based on this observation, a multi-chip power module is proposed in this article. Section II briefly presents the concept of the presented package; section III describes its manufacturing; the experimental results are given in section IV.

II. Power Module Design

As demonstrated in [6], interconnects made of copper or silver offer the best performance (lower resistance) for a fail-to-short package. Here, the interconnects are provided using a "sandwich" structure, where the semiconductor dies are placed between two direct bonded copper (DBC) tiles (Fig. 1). Protruding features are etched in the inner copper layers of the sandwich to match the pattern of the SiC dies (25 mΩ, 1200 V MOSFETs from Wolfspeed) as well as to directly secure both DBC tiles together [7].

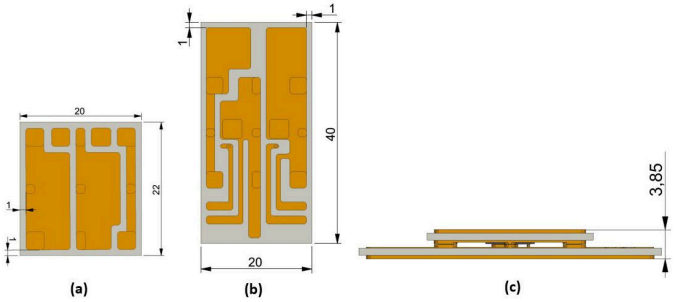


Fig. 1: front view of the top substrate (a), bottom substrate (b) and side view of the assembly (c), with dimensions (in millimeters). Protruding features ("posts") are formed on the copper layer for interconnection.

The structure is then assembled using silver sintering for the die attach (top and bottom) as well as for the DBC-to-DBC bonding. This ensures a good performance interconnection (silver sintering offers excellent thermal and electrical conductivity [8]). Furthermore, as presented in [6], silver was found to be a suitable contact material to achieve fail-to-short behaviour with SiC devices. It is worth noting that no additional element (spacer, balls, etc.) is used for the interconnects: the height of the protruding structures is carefully controlled to match the thickness of the SiC devices and that of the silver joints.

The patterns visible in Fig. 1 form a half-bridge module, with one SiC transistor per switch position. This topology was chosen because it demonstrates a multi-chip module, but allows to test both switches independently. The tiles in Fig. 1a and 1b have different sizes to give access to the exposed terminals of the bottom tile in the assembled module (the top tile is only used as a redistribution layer and is connected to the drain pads of the SiC MOSFETs).

III. Manufacturing

The first manufacturing step consists in patterning blank DBC mastercards (Rogers-Curamik, 500 µm Cu/250 µm HPS Al_2O_3/500 µm Cu). To perform the 2-level copper etching with a sufficient resolution to contact small features such as the gate

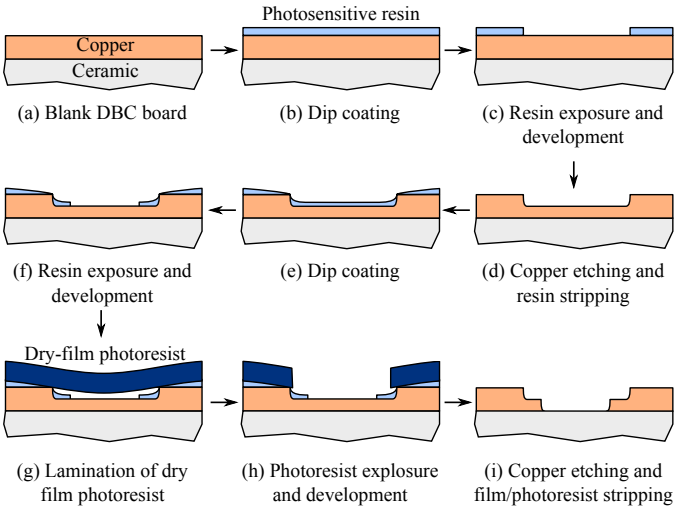


Fig. 2: Process flow for the two-step etching

pad of the SiC MOSFETs (500 µm by 800 µm), an etching technique was developed [9], [10].

The principle of the two-step etching technique is presented in Fig. 2, and fully detailed in [10]. Starting with a blank DBC substrate (a), a coat of photosensitive resin (MC Dip coating, Microchemicals) is applied by dip-coating (b). This layer is then patterned using standard UV photolithography (c) and the exposed copper is etched using ferric chloride in a spray etcher (d). This forms the protruding features, and the etching time is used to control the height of the protrusions. The photosensitive resin is then stripped and a new coat is applied (e) and patterned (f). Because of surface tension effects, the resin was found not to provide a sufficiently thick coating on the crests of the protrusions. As a consequence, a layer of thick (75 µm) photosensitive dry-film (Dupont Riston PM275) is added (g) and patterned using UV lithography (h). Note that this dry film could not be used alone, as it is too rigid to conform to the flanks of the protrusions. Finally, the exposed copper is then etched all the way down to the ceramic, and the layers of photoresist are stripped away (i).

Some photographs are visible in Fig. 3. The DBC "mastercards" are actually limited to $50\times50\,\mathrm{mm}^2$ because of the size limitation of our lithography equipment (a mask aligner designed for 3 in wafers). This allows only 2 bottom tiles (or 4 top tiles) to be processed simultaneously. Fig. 3a presents a "mastercard" at stage (d) in Fig. 2 for the bottom tiles. Fig. 3b presents a bottom tile after completion of the etching process and singulation (using a wafer saw). A silver electroless plating is then applied to improve the strength of the assembly steps (see below) (Fig. 3c).

The SiC dies used (Wolfspeed CPM2-1200-0025B) have an Al top finish and Ni/Ag backside finish [11]. While Ni/Ag is compatible with silver sintering, it is not the case of Al. Therefore, the SiC dies must be re-processed by e-beam evaporation of Ti (50 nm) and Ag (150 nm) through a shadow mask. This process is described in [10], and was found to provide a satisfying adhesion to the dies. Obviously, such re-

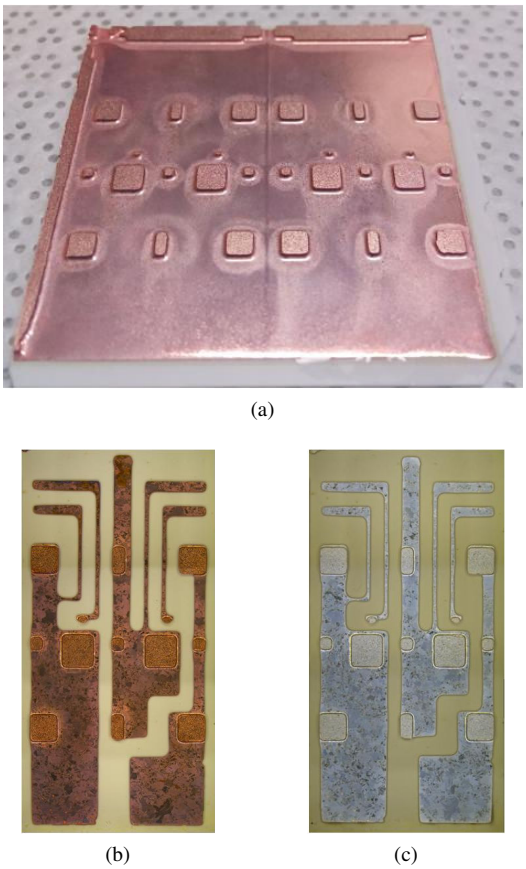


Fig. 3: (a) Photograph of one of the DBC substrates after the first copper etch step, showing the protrusions used to contact the two SiC MOSFETs and to bond both substrates together. This $\approx 50 \times 50\,\mathrm{mm}^2$ substrate will produce two bottom tiles after singulation; (b) one of the tiles after the second etching step and singulation; (c) the same, after silver plating.

processing would not be acceptable for industrial production, and dies with a suitable finish would be required instead. This, however, should not have consequences on the failure behaviour of the package described here.

The two DBC tiles and the two SiC MOSFETs are then assembled using silver sintering, as depicted in Fig. 4. First, some silver paste (Heræus ASP 295) is printed on the bottom tile using a 50 µm stainless steel stencil. The paste is slightly dried for 2 min at 85 °C in an oven to make it harder while retaining some tackiness (Fig. 4a). The SiC dies are placed (with the source and gate pads facing down) using a die bonder for proper alignment, and sintered with the following profile: temperature ramp-up at $3\,^{\circ}\mathrm{C\,min}^{-1}$ up to 170 °C, soak for 30 min, fast ($40\,^{\circ}\mathrm{C\,min}^{-1}$) ramp-up to 240 °C, and soak for 1 h, followed by natural cooling down to room temperature. A 2 MPa pressure is applied when the temperature reaches 120 °C and is maintained until the end of the process (Fig. 4b).

In parallel, some silver paste is printed on the top tile (Fig. 4c) and slightly dried in an oven (85 °C, 2 min). This tile is placed in the bottom pocket of a custom alignment jig

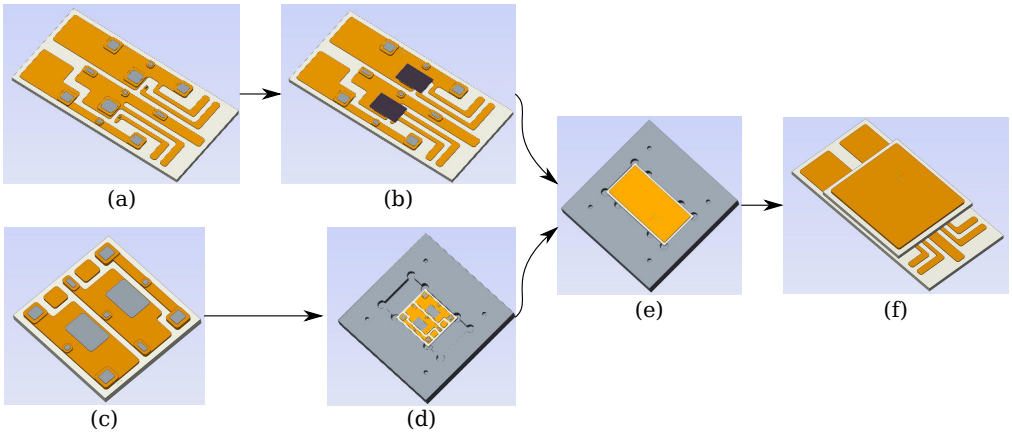


Fig. 4: Assembly process: (a) stencil-printing of silver paste on bottom substrate; (b) Die positioning and sintering of the silver paste; (c) stencil printing of silver paste on top substrate; (d) positioning of top substrate in the lower pocket of the alignment jig; (e) positioning of the bottom substrate in the upper pocket of the alignment jig; (f) final module after the second silver sintering step.

Sample	Encapsulant	Clamping	Switch	E [J]	R_{init} [mΩ]	R_{final} [mΩ]	Failure mode
Module A	None	Yes	MOS 1	–	186	77	SC
			MOS 2	8.8	201	128	SC
Module B	Silicone	Yes	MOS 1	20	165	120	SC
			MOS 2	1	188	167	SC
Module C	Epoxy	No	MOS 1	9.7	–	–	OC
			–	–	–	–	–
Module D	Silicone	Yes	MOS 1	2.24	180	158	SC
			MOS 2	–	–	–	–

TABLE I: Summary of the tests. For module A, an error during the test prevented the failure energy to be recorded. For module C, the first test resulted in the separation of the tiles, hence the absence of tests for MOS 2. For module D, the gate of MOS 2 was found not to be connected after manufacturing, so this transistor could not be tested.

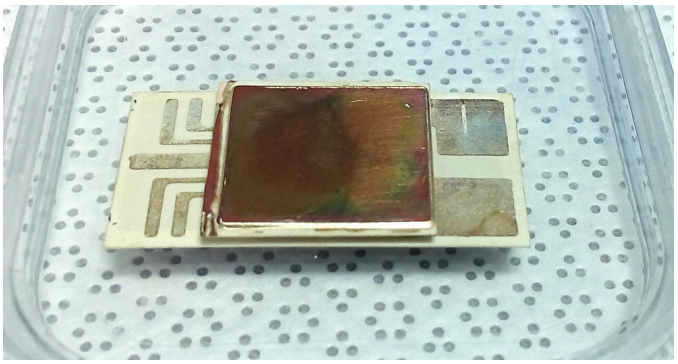


Fig. 5: Photograph of one of the sandwich modules after assembly.

(d) made out of aluminium. The bottom tile (populated with the SiC dies) is then placed on top (e) for a second (and identical) sintering process. The sandwich structure can then be removed from the alignment jig (f). A photograph of one of the 4 power modules tested here is shown in Fig. 5.

Three encapsulation configuration are investigated:

- no encapsulation (the module is tested directly after assembly). This is the simplest case and is used as a reference;
- encapsulation in a silicone gel (Wacker SilGel 612). This silicone gel is commonly used in power modules;
- encapsulation in a rigid epoxy resin (Duralco 133), for evaluation of the consequences of using a hard encapsulant.

The silicone gel is prepared according to the manufacturer's specifications. The two components are weighted and mixed. The mix is degassed under vacuum until the bubbles collapse and is poured into the module. A new degassing step is performed once the module has been filled. The gel is cured by placing the module in an oven at 100 °C for 15 min.

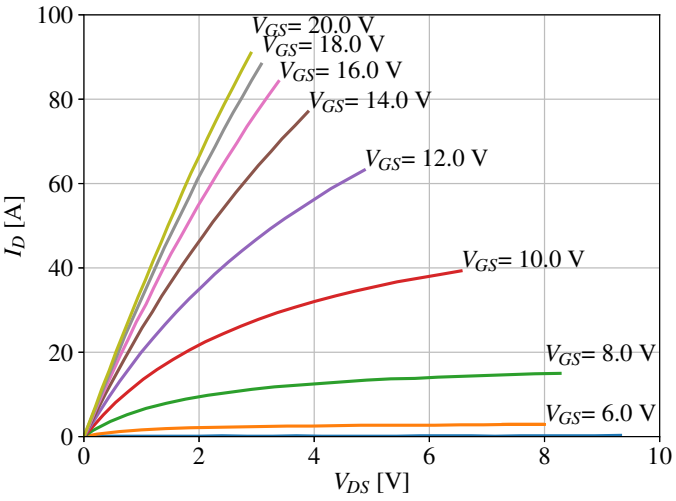
For the epoxy encapsulation, the two components are mixed together, but no vacuum degassing is performed as the mix is very viscous. The module to be encapsulated is placed on an aluminium plate, its two DBC tiles touching a lump of epoxy resin. During the cure (100 °C), the resin becomes much more fluid and infiltrates between the DBC tiles by capillarity effect, filling the sandwich entirely.

The modules tested in this article, along with their encapsulation configuration, are listed in Tab. I.

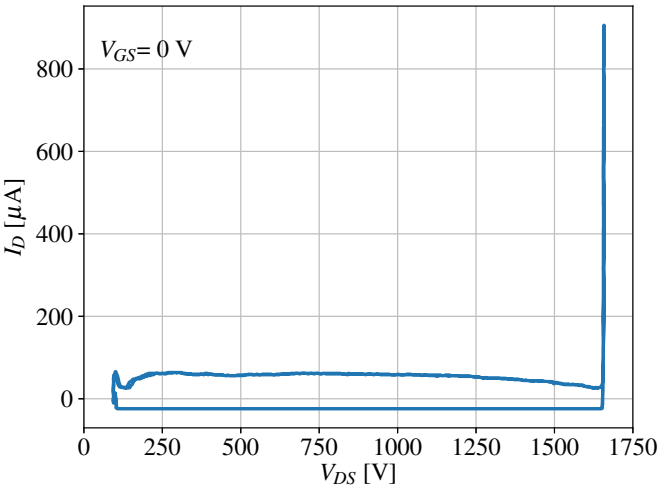
IV. Test

A. Test Protocol

After manufacturing, the power modules are tested electrically using a Tektronix 371A curve tracer in 4-point configura-



(a)

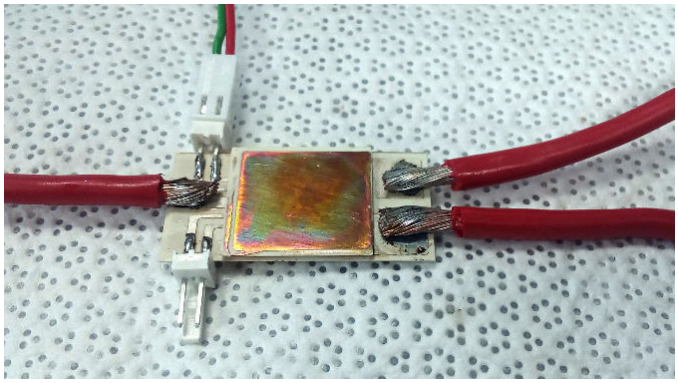


(b)

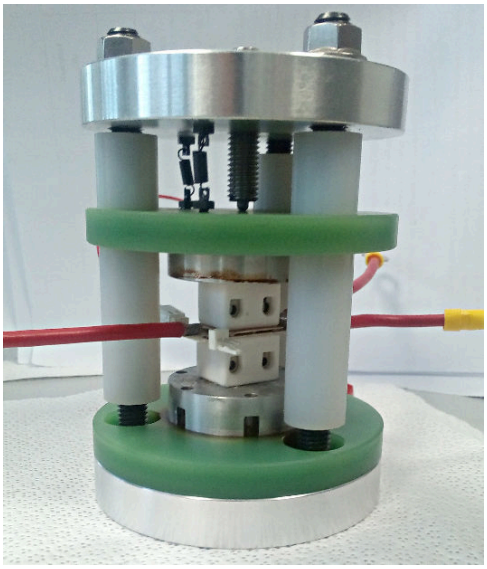
Fig. 6: Static characteristic of one of the SiC MOSFETs after packaging, measured using a Tektronix 371A high power curve tracer: (a) forward voltage for various gate-to-source voltages; (b) breakdown voltage in the off-state (the resolution of the curve tracer is relatively coarse, hence the "loop" visible before the breakdown).

tion. An example of static characteristic is presented in Fig. 6a. It shows that the MOSFET exhibits a $R_{DS_{on}}$ of 27 mΩ, which is consistent with the datasheet of the components (25 mΩ). During these tests, one MOSFET (MOS 2 from module D) is found not to have any gate contact, and therefore cannot be tested in short-circuit. For the encapsulated modules, the breakdown voltage of the transistors is found to be much higher than their voltage ratings (1600 V vs. 1200 V, see Fig. 6b), which is consistent with previous observations.

For short-circuit testing, 6 mm^2 wires are soldered onto the terminals of the modules (Fig. 7a). A clamp (Fig. 7b) is also used for modules A, B and D during the short-circuit tests and during the endurance tests described below. For module



(a)



(b)

Fig. 7: (a) the power module connections: 6 mm^2 soldered wires for the power, and Molex connectors for the gate driver; (b) test fixture, used to clamp the modules under test (the wires of the modules are visible).

C, because it is encapsulated in epoxy and therefore expected to be stronger, no clamp is used.

Each packaged MOSFET is then submitted to a surge current test, using the circuit depicted in Fig. 8a (and detailed in [6], [12], [13]). An example of the current and voltage waveforms acquired during the surge test is presented in Fig. 8. In this graph, it can be seen that the current rises rapidly to almost 2000 A. At this point (t=80 µs), the protection system is triggered, and the gate voltage of the protection switch S is reduced, resulting in a reduction of the the current across the DUT (t=100 µs), before the protection switch is turned-off completely at t_{end}=230 µs.

The failure energy E is computed from the waveforms as:

$$E = \int_0^{t_{end}} V_{DS} \cdot I_D dt \tag{1}$$

After the surge test, the transistors which failed in short-

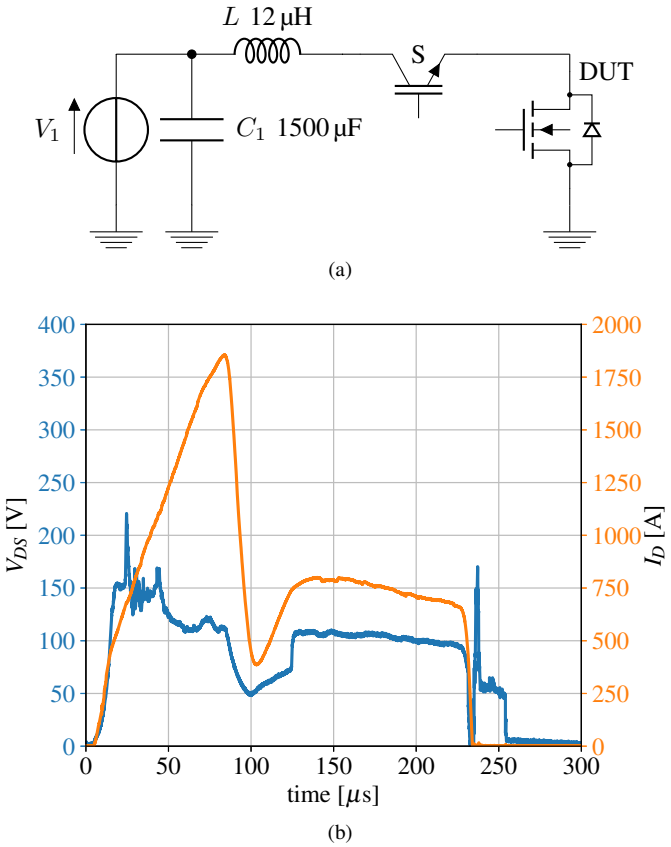


Fig. 8: (a) Simplified diagram of the test circuit: a capacitor C_1 stores the energy to be used during the test; a protection switch S controls the current flow; the stray inductance L is not required, but it must be considered because it is large due to the physical size of the test system. (b) example of voltage and current waveforms acquired on a packaged MOSFET (module B) during a short-circuit test which resulted in a failure of the device (short-circuit) with an energy of 20 J.

circuit are connected to a 10 A current source for 6 h to monitor the stability of the contact. Their drain-to-source resistance is monitored, and the values measured at the beginning (R_{init}) and at the end (R_{final}) of this 6-h period are given in Tab. I. Note that the test current is kept low compared to the current ratings of the MOSFETs (50 A) because the modules are maintained in the clamp from Fig. 7b, which does not provide cooling.

Finally, the DBC tiles are separated mechanically, and the dies are observed using optical and electron microscopes.

B. Test Results

A summary of the results is presented in Tab. I. It shows that all the modules which were clamped in the fixture from Fig. 7 exhibit a fail-to-short behaviour, with a failure resistance of usually less than 200 mΩ, independently of the energy which caused the failure. On the contrary, despite being encapsulated in a solid material (epoxy), the un-clamped module (C)

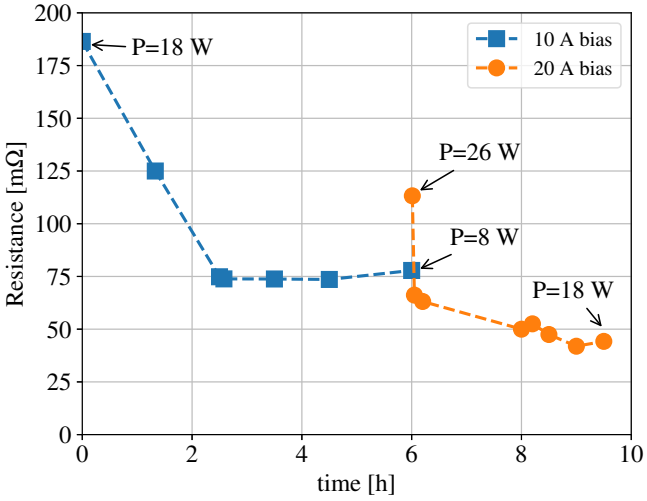


Fig. 9: Evolution of the resistance of MOS 1 in module A during the endurance test. After 6 h the bias current was increased to 20 A to evaluate its effect on the resistance.

separated during the surge current test, resulting in an open-circuit.

This means that the fail-to-short behaviour requires two key elements: a large, solid interconnect system (standard wirebonds can only manage a very low energy levels [4]), but also a strong mechanical support to prevent the module from exploding.

As described above, the modules which exhibit fail-to-short behaviour are then tested for stability, by monitoring their drain-to-source resistance over 6 h under current bias. The results in Tab. I show that for all MOSFETs the resistance reduced over the test period, which indicates a stable behaviour. The measured resistances tend to be high compared to the $R_{DS_{on}}$ of the MOSFETs (25 mΩ). This was also observed on single die tests [6], and is related to the metallurgy of SiC: for Si devices, the failure test causes the semiconductor material to melt and form a conductive alloy [3]. SiC does not melt. Instead, the die shatters and the fail-to-short behaviour is achieved because the metals around the die evaporate and infiltrate the cracks. This results in thinner and more resistive paths being formed. Nevertheless, the endurance tests demonstrate that these paths tend to become stronger over time, resulting in a gradual reduction in resistance.

Furthermore, as depicted in Fig. 9, for some modules, the endurance test was extended beyond the 6 h-arbitrary limit. In the case of the test in Fig. 9, the current was raised from 10 to 20 A. As a consequence, the resistance of the package is found to drop even further, down to less than 50 mΩ, not far from the $R_{DS_{on}}$ of the MOSFETs before they fail.

At the end of the endurance tests, the DBC tiles are separated and observed. An example is given in Fig. 10, and shows an extensive damage. This is due to the short-circuit test, which caused the dies to break (both DBC tiles have fragments of the dies attached). It is also due to the endurance tests, in which a high (non measured) temperature was reached

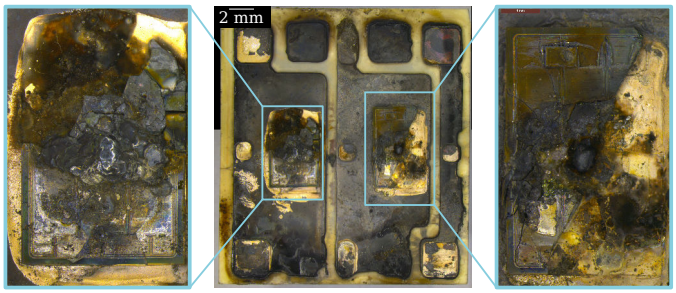


Fig. 10: Optical photograph of the top tile of power module A (center) after short-circuit test, 6 h current biasing, and separation of the ceramic tiles. An enlargement of each die is also provided (right and left). One can observe that dies are largely broken, and that the materials strongly changed in color.

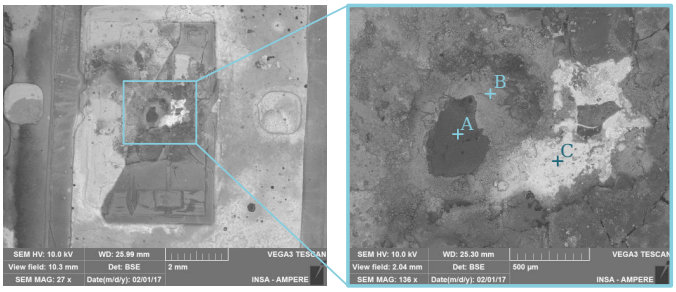


Fig. 11: SEM image of one of the dies from Fig. 10. The chemical composition at point A is Si 12 at%, Ag 75 at%, Cu 5 at%; at point B Si 62 at%, Ag 5 at%, C 27 at% Cu 4 at%; at point C Pb 76 at%, Sn 1 at% and O 10 at%.

because the power module were not attached to a cooling system. This probably caused the metal parts to oxidize.

An SEM observation (Tescan Vega 3) of the same module is given in Fig. 11, along with three element analyses (Brucker Quantax Energy-dispersive spectroscopy). While the elements found in in points A and B are expected (Si, Cu, Ag, C), point C exhibits a large Pb content (and some Sn). This element most probably comes from the solder used to attach wires to the modules. An hypothesis is that some of the solder migrated during the endurance test (the temperature might have been close to the solder melting point). This might in part explain the reduction in resistance observed, e.g. in Fig. 9. Note that previous tests [6] performed on different structures (without any Pb) also exhibited some reduction in resistance, so the presence of Pb is not the only factor in this phenomenon. Further investigations are required to determine whether a low melting point metal placed close to the die (ideally Sn rather than Pb) could actually help reducing the resistance of the fail-to-short package after failure.

V. Conclusion

In this paper, a fail-to-short packaging solution was proposed for SiC dies, based on a "sandwich" structure and silver sintering. The manufacturing process was described. 4 modules were submitted to large current pulses, causing the semiconductor devices to fail. Providing that the modules were mechanically clamped to prevent their tiles from separating, they were found to provide a satisfying fail-to-short behaviour, which remained stable after 6 h of current biasing. This demonstrates that although SiC and Si have very different metallurgies, SiC fail-to-short modules can be made.

Acknowledgment

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References

[1] H. Chen, W. Cao, P. Bordignon, R. Yi, H. Zhang, and W. Shi, "Design and Testing of the World's First Single-Level Press-Pack IGBT Based Submodule for MMC VSC HVDC Applications," in *Energy Conversion Congress and Exposition (ECCE), 2015 IEEE*, 2015.

[2] ABB, "StakPak IGBT press-pack modules," ABB, Lenzburg, Switzerland, Tech. document 5SYA2100-01, Apr. 2013.

[3] S. Gunturi, J. Assal, D. Schneider, and S. Eicher, "Innovative Metal System for IGBT Press Pack Modules," in *Proceedings of the International Symposium on Power Systems and Devices (ISPSD)*, Cambridge, UK, Apr. 2003, p. 4. [Online]. Available: https://pdfs.semanticscholar.org/f02f/1d93fc4c1e3ef0a81c9c9d743418bd0919c8.pdf

[4] I. Yaqub, J. Li, and C. M. Johnson, "Dependence of overcurrent failure modes of {IGBT} modules on interconnect technologies," *Microelectronics Reliability*, vol. 55, no. 12, Part A, pp. 2596 – 2605, 2015. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0026271415301761

[5] J. De Warga, "Semiconductor device in a sealed package," United States Patent and Trademark Office, Patent 03489957, 1967. [Online]. Available: http://www.google.com/patents?id=tiRJAAAAEBAJ&dq=3489957

[6] I. Dchar, C. Buttay, and H. Morel, "SiC power devices packaging with a short-circuit failure mode capability," *Microelectronics Reliability*, 2017. [Online]. Available: https://hal.archives-ouvertes.fr/hal-01562547

[7] C. Buttay, J. Rashid, C. Johnson, F. Udrea, G. Amaratunga, P. Ireland, and R. Malhan, "Compact Inverter Designed for High-Temperature Operation," in *Proc. IEEE Power Electronics Specialists Conference PESC 2007*, 2007, pp. 2241–2247.

[8] J. G. Bai, Z. Z. Zhang, J. N. Calata, and G. . Lu, "Low-temperature sintered nanoscale silver as a novel semiconductor device-metallized substrate interconnect material," *IEEE Transactions on Components and Packaging Technologies*, vol. 29, no. 3, pp. 589–593, Sept 2006.

[9] R. Riva, C. Buttay, M.-L. Locatelli, V. Bley, and B. Allard, "Design and Manufacturing of a Double-Side Cooled, SiC based, High Temperature Inverter Leg," in *Proceedings of the High Temperature Electronics Conference and Exhibition, HiTEC 2014*. Albuquerque, NM: IMAPS, May 2014. [Online]. Available: https://hal.archives-ouvertes.fr/hal-00997365

[10] C. Buttay, R. Riva, B. Allard, M.-L. Locatelli, and V. Bley, "Packaging with double-side cooling capability for SiC devices, based on silver sintering," in *44th Annual Conference of the IEEE Industrial Electronics Society (IECON 2018)*, ser. Proceedings of the 44th Annual Conference of the IEEE Industrial Electronics Society (IECON 2018). Washington, United States: IEEE, Oct. 2018. [Online]. Available: https://hal.archives-ouvertes.fr/hal-01895805

[11] Wolfspeed. (2013) CCPM2-1200-0025B Silicon Carbide Power MOSFET Z-FET MOSFET. [Online]. Available: https://www.wolfspeed.com/

[12] I. Dchar, C. Buttay, and H. Morel, "Avalanche robustness of SiC Schottky diode," *Microelectronics Reliability*, Sep. 2016. [Online]. Available: https://hal.archives-ouvertes.fr/hal-01373039

[13] F. Saint-Eve, "Influence des régimes extrêmes de fonctionnement sur la durée de vie de composants à semiconducteurs de puissance," Ph.D. dissertation, Cachan, Ecole normale supérieure, 2004.