Digital electronics for inertial MEMS and space applications

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***Abstract*— This paper presents an electronic platform for driving resonant MEMS in inertial sensors, and possibly other resonant or carrier based sensors. The architecture is fully integrated in a digital programmable device (FPGA), and avoids several critical components when dealing with space qualification.**

The core hardware functions are Direct Digital Synthesis , Sigma-Delta modulation, Time to Digital conversion. These functions are driven by an embedded processor, managing a second level of software functions : synchronous demodulation, Phase-Locked Loop, decimation, digital communications. The specificity of this digital platform is to avoid usual Analog-To-Digital and Digital-To-Analog conversion. All measurements are performed by means of digital delay counting, yet allowing an interesting resolution of 16 bits even on carried signals up to 100 kHz with a frequency resolution better than 1 µHz (11 digits on the frequency).

A prototype of vibrating accelerometer has been integrated and characterized to experience the electronic performance on a real sensor. The results show that the embedded architecture is already close to the performance obtained with separate equipments on the test bench.

Keywords*— *MEMS, accelerometer, gyroscope, resonator, FPGA, frequency synthesis

I. INTRODUCTION

Cubesat activities are growing rapidly and ambitious projects are arising, involving formation flying, orbit control and rising. These missions need (electric) propulsion, which in turn need inertial sensors like accelerometers in the control loop.

ONERA has been developing vibrating MEMS inertial sensors for various applications. For example the VIA cell (Vibrating Beam Accelerometer family) is already in use in the French civil and defense industry (Fig. 1). The VIG cell (Coriolis Vibrating Gyroscope family) has been proposed for space applications, in the frame of low cost assistance gyroscope associated with star trackers on satellite platforms : detumbling, slowing down satellite rotation to allow star tracker acquisition or recovery.

Recent evolution of this accelerometer led to a shorter range but higher resolution device, below µg, which can address the range of electric propulsion. This is achieved mainly by increasing the test mass of the sensor head [4]. All sensors are in the family of Vibrating Beam Accelerometers (VBA), and an important action of the development concerned the Drive & Measurement electronics.

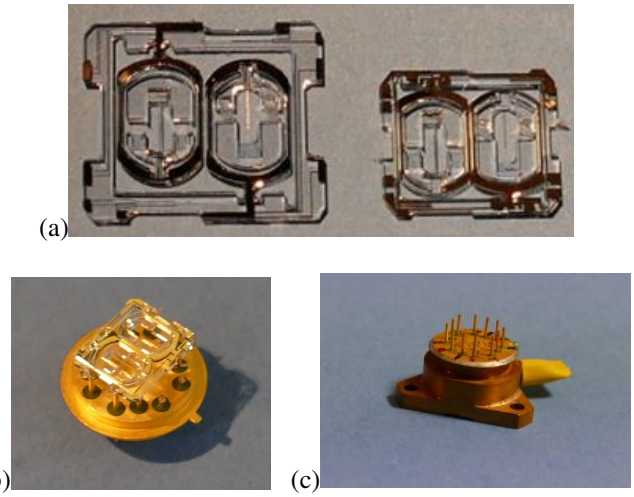

Fig. 1. DIVA accelerometer. (a) Dual sensor head for differential measurement. (b) mounting on socket. (c) packaging in vacuum.

II. HISTORY OF DEVELOPMENT

The initial research team focused on the quartz cell design and etching process. Electronics was limited to discrete component charge amplifiers and local oscillator loop, the signal being acquired by measuring equipment. Digital electronics were introduced from 2008 with a Programmable ROM (PROM) sequencer (sine wave table for DAC, switch sequence for demodulation), followed in 2010 by an ARM CORTEX microcontroller driving external frequency synthesizers and Analog to Digital Converters (ADC). From 2012 these elements have been re-synthesized in an FPGA, including the processor core, leading to the present single chip version.

The gyroscope architecture is shown on Fig. 2, and further described in [2], following a study in the ESA NEOSAT program. The design of an ASIC had been investigated, but prohibitive cost prevented from further development on a space grade. Instead, a first port of the electronics has been achieved

two years ago on a radhard microcontroller delivered by TAS [3].

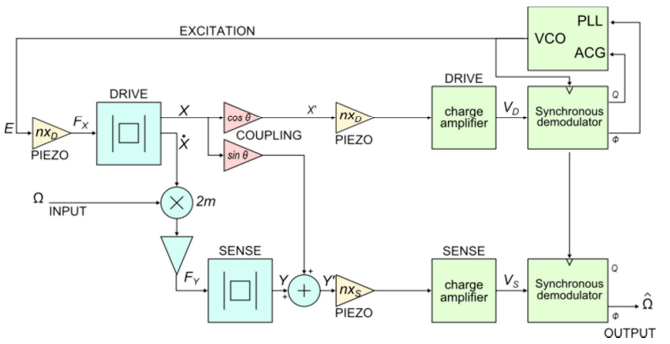

Fig. 2. ONERA Coriolis Vibrating Gyroscope architecture. Sensor quartz cell (blue, yellow, red), and electronic functions (green).

In order to further reduce power and size, we retargeted the development towards all-digital design, synthesizable on FPGA, avoiding mixed signal functions.

III. New Versatile Electronics

Fig. 3 shows the previous accelerometer and gyroscope functions from the FPGA implementation point of view. As expected, all functions are digital, except passive filters and charge amplifiers on the sensor head. They are developed as Intellectual Properties (IP) in VHDL, in order to be portable from one device to another.

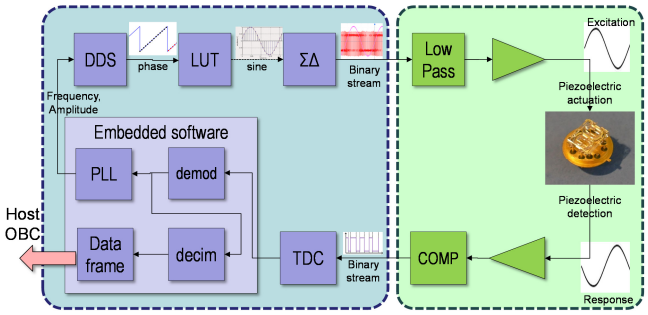

Fig. 3. General architecture. FPGA (left), and analog circuits (right).

A. Direct Digital Synthesis

The first critical function is the frequency synthesizer, based on Direct Digital Synthesis (DDS). Such a synthesizer makes use of a phase accumulator, delivering the instantaneous phase of the desired signal by accumulating at each sampling time a phase increment [4]. In order to get a fine frequency resolution, the phase increment word ΔΦ (Fig. 4) shall be sized with a sufficient number of bits, but the system clock frequency does not need to be increased, as in traditional frequency dividers. In the present design the phase accumulator can be as wide as 48 bits and run at 250 MHz, sweeping frequencies with a resolution smaller than 1 µHz.

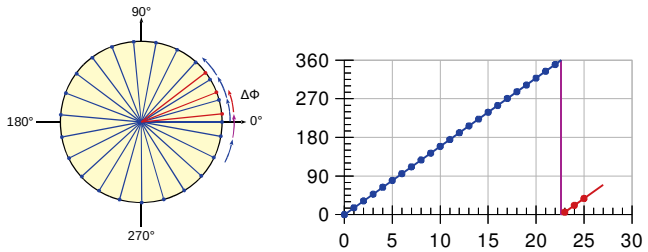

Fig. 4. DDS Phase wheel. One phase turn may not be necessarily an integer multiple of the phase increment, allowing fine frequency resolution.

The phase then enters a Look Up Table (LUT) to get the output waveform, hopefully a pure sine wave, which finally feeds a Digital to Analog Converter (DAC).

B. Sigma-Delta modulation

Actually no multibit DAC is involved in the conversion ; digital sine waves are processed by ΣΔ modulation (Fig. 5a). One-bit ΣΔ modulators (first and second order) have been implemented, according to standard algorithms in the literature [6], with complementary outputs $Q/\bar{Q}$ on differential pairs of the FPGA. The spectrum of the binary stream contains the expected spectral line (Fig. 5b), and no harmonics before higher frequencies close to the sampling frequency. With a ratio of 1000 between the sampling and target frequency, the latter is easily separated with a passive RC filter.

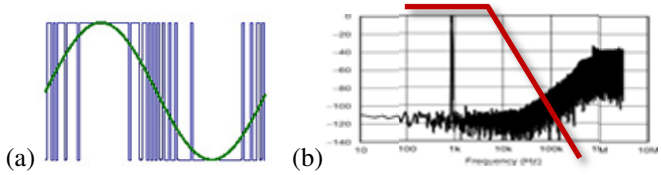

Fig. 5. ΣΔ modulation. (a) binary stream. (b) Spectrum. The signal of interest (sine wave) is easiliy separated from the binary stream with a passive filter.

C. Time to Digital Conversion

The analog to digital conversion for the phase and quadrature components of the sensor outputs is more complex. As all signals in the system are modulated by the same carrier, which is the resonant frequency of the vibrating cell, they are compared with another phase coherent, reference sine waveform provided by the FPGA on a second synthesizer instance (Fig. 6). Crossing events at comparators are time-stamped by the internal system clock (the same which was used for the DDS), and from these data the phase and quadrature components are extracted. It has been demonstrated in a recent patent [1] that the phases corresponding to the time stamps in a measurement cycle can be demodulated (one period in one cycle) to recover the in-phase and quadrature components.

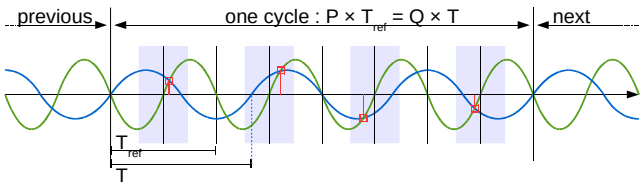

Fig. 6. Measurement cycle with reference signal (green) and measured signal (blue). The red crosing event form a periodic wave over the cycle.On this example, P = 4 and Q = 3.

To further improve the time stamp resolution, the system clock is replicated in a phase tree with eight divisions per clock period, called sub-clocks. When a comparison event occurs, the value of the instantaneous phase in the DDS accumulator is memorized in a register, but the sub-clock state is also memorized, to account for a fractional part (Fig. 7). The TDC resolution is now 0.5 ns, 8 times smaller than the 250 MHz system clock.

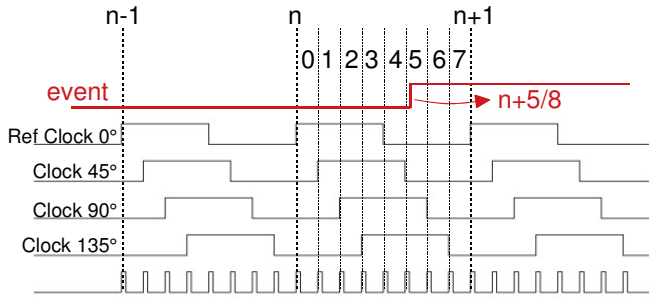

Fig. 7. Sub-clock tree to improve time resolution. The equivalent datation clock is 2 GHz, although it is not achievable on the FPGA gates.

Actually this is not the State of Art in fractional delay implementation on FPGA [7], but the current design is an efficient trade-off and removes the need for more traditional ADC.

Let x_k be a sine signal composed of an In-Phase term XP and a Quadrature term XQ, and sampled at the rate Ts ($\theta = 2\pi.F.Ts$) :

$$x_k = XP \cos k\theta + XQ \sin k\theta \qquad (1)$$

The demodulation of x consists in multiplying it with $\cos k\theta$ and accumulate, to get the Phase term, and with $\sin k\theta$ and accumulate, to get the Quadrature term.

$$\widehat{XP} = \frac{2}{N}\sum_{k=0}^{N-1} x_k \cos k\theta$$
$$= XP + \underbrace{\frac{XP}{2N}\sum_{k=0}^{N-1}\cos 2k\theta}_{\Sigma C2} + \underbrace{\frac{XQ}{2N}\sum_{k=0}^{N-1}\cos k\theta \sin k\theta}_{\Sigma CS} \qquad (2)$$

$\Sigma C2$ and ΣCS will naturally cancel out when $N\theta$ is an exact multiple of 2π (an integer number of periods is covered), which is constantly and rigorously ensured by the two coherent synthesisers ; there are always strictly P periods of the reference in the cycle, and Q periods of the resonator signal. For this reason, measurements are always performed on complete cycles, so that the sampling rate is basically F / Q (or Fref / P, since Fref = P/Q × F).

The next operation, the demodulation process, as well as decimation, are performed by software in the embedded processor core. In the current design, the processor is a “soft core”, i.e. it is synthesised on the gate array. Other Systems on Chip (SoC) from different manufacturers propose hard cores next to the programmable array. They may be used as well since all developed code is ANSI C and thus portable the same way as VHDL design.

At last, the Phase Locked Loop is a pure algorithmic function implemented in software, whose refresh rate is the measurement cycle. Communication with the host is realised by a standard and low cost Universal Asynchronous Receiver Transmitter peripheral (UART). The link is bi-directional, to receive configuration parameters (cycle P/Q ratio, system clock, control loop coefficients…) and transmit data frames from the sensors.

The complete IP (DDS, LUT, ΣΔ, TDC) can be instantiated several times, even on little FPGA like the ARTIX family, including the Microblaze soft core, so that a 6 axes IMU (3 accelerometers and 3 gyroscopes) can be considered on the same FPGA device (Fig. 8). From this design, the IP may be significantly simplified in final applications, since 4 coherent DDS are in place where 3 are needed, 4 TDC are in place where 2 are needed, and numerous optional debug and control registers could be discarded.

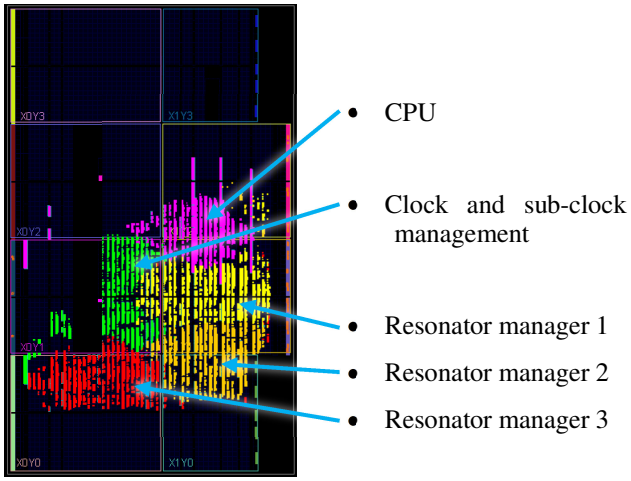

Fig. 8. View of the implemented design on a Xilinx Artix 100 device for the management of 3 resonators. CPU and clock blocks are common to multiple resonator IPs.

IV. Performances

A. *Capabilities*

The frequency range of the synthesizer covers all frequencies up to 100 kHz, with a resolution better than 1 µHz. The DDS phase increment word is configurable during design implementation, and can be extended up to 64 bits instead of 48, while still working at 250 MHz, and leading to a frequency step as low as 10 pico-Hz. The cost of the extension is a larger latency (up to 6 clock periods) in the accumulator, but this is acceptable as long as it is fixed in the design and can be later calibrated as a small phase shift. Only the 32 upper bits of the running phase are later used in the acquisition system, to provide a nano-rd precision in computations, more than what will be ever measured.

B. *Intrinsic electronic performance*

The innovative measurement system based on Time to Digital Conversion can be evaluated by sampling the reference signal with itself, rejecting source clock and source voltage fluctuations. On the following acquisition (Fig. 9, demodulation of phase & quadrature components) the standard

deviation is 30 ppm of the signal, which is equivalent to a 16 bits ADC.

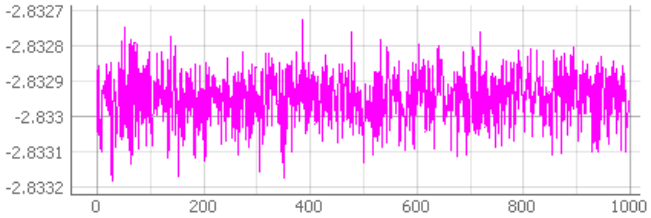

Fig. 9. Measurement noise with the TDC int the FPGA.

When expressed as phase measurement, the resolution of the system is 30 µrd.

C. Integration

The size of the board is 70×30 mm, corresponding to a commercial module for consumer market (Fig. 10). A smaller footprint can be found by some manufacturers, down to 40×30 mm, with the same functionality. The analog board (filters and comparators) can be routed in the same size as the FPGA board, so as to stack the couple of boards together. A single 3.3 V line will supply the system, for a power budget of less than 1 W for a 3-axes system.

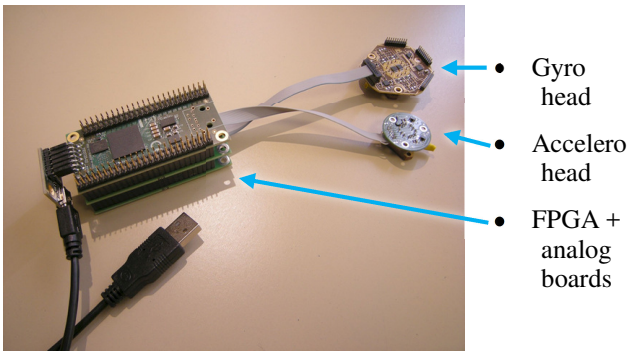

Fig. 10. Current propotype, under characterization at electronic level and instrument level.

D. Performance as instrument

The Quartz Vibrating Beam Accelerometer has been connected to the platform for characterization in instrumental conditions : the accelerometer is set on an horizontal turn table (horizontal axis, vertical tray) to project gravity around its sensitive axis, to extract bias and scale factor. This test bench is inside a thermal chamber to track possible bias and scale factor drift under temperature. The first tests were performed within a slightly reduced range of [-30 +70°C] as a precaution, but no warning finally prevented from running the full [-40 +80°C] industrial temperature range.

Bias evolution during temperature cycles (10°C steps) is presented Fig. 11. The residual after thermal sensitivity modelling is 80 µg rms. Actually a better intrinsic performance of the quartz cell has been observed (33 µg) with a self-sustained oscillator but measured by external frequency meters. Considering the hysteresis on the figure reveals that repeatability is poor at low temperature, especially when becoming warmer from icing temperatures. This is certainly due to the fact that the electronic boards are open to the thermal chamber atmosphere, subject to condensation and frost. Next experiment will be conducted with a closed electronic board (the local charge amplifier is already in a closed, hermetic case), and also under vacuum, as we are encouraged by the repeatability from one thermal cycle to another, which in turn is in the range of 30 µg rms.

Concerning the scale factor stability during the same experiment (Fig. 12), the residual after thermal sensitivity modelling is 24 ppm rms, close to the intrinsic performance of the cell (17 ppm).

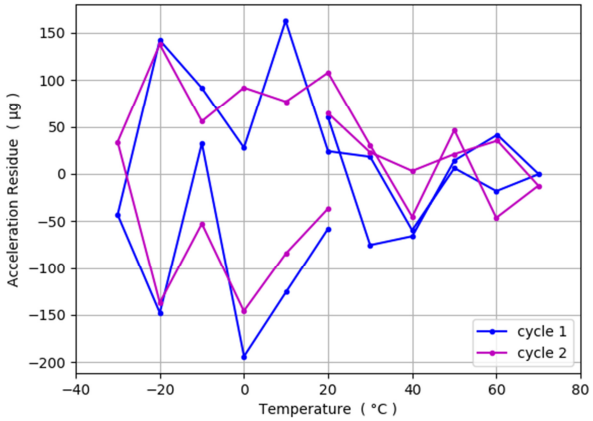

Fig. 11. Accelerometer bias stability over temperature.

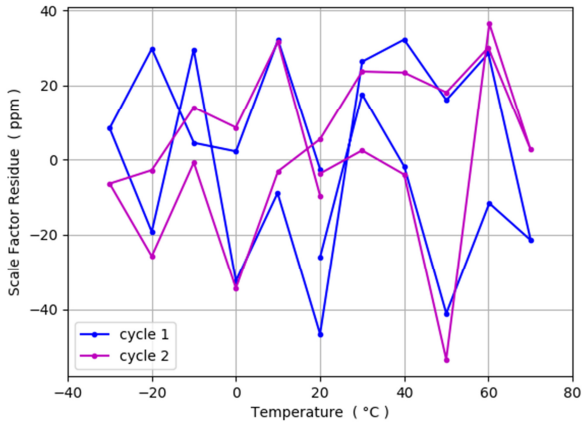

Fig. 12. Accelerometer scale factor stability over temperature.

The last characterization concerns noise. A long sequence is acquired in stabilized conditions : no temperature evolution, no environmental vibrations, so that only the instrument noise is recorded. The Allan variance (in μg^2) or the Allan standard deviation (in µg rms) is plotted versus the integration time, which is the sampling period after decimation (Fig. 13). The basic sample rate of the instrument is only little more than 1 Hz, but is only limited by the large debug data transmitted to the host in each frame, containing of course the frequencies from the synthesizer that are the image of the measured acceleration, but also internal demodulation data, PLL state, and all P samples of the measurement cycle described in §III.C.

When all this monitoring and debug information will be removed from data frame in final applications, the data rate will not be limited up to 100 Hz sampling.

According to the model, the Allan minimum is 0.8 µg and the noise at 10 Hz sampling is 10 µg, which is the current model at the quartz cell level, so that one can conclude that

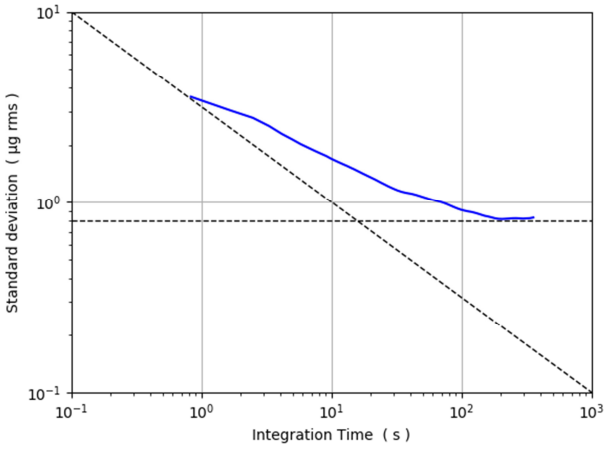

Fig. 13. Allan variance as a function of integration time. Flat asymptot is the Allan minimum at 0.8 µg rms.

V. PERSPECTIVES

The design and implementation of a full digital architecture for resonant MEMS have been presented. In the perspective of qualifying a design for a space application, it is noticeable that this design does not involve any DAC or ADC device, and minimize the use of discrete components, that are reduced to operational amplifiers and comparators.

All necessary functions (DDS, TDC, PLL) have been developed as Intellectual Properties or source code, and are therefore mainly non dependent on the FPGA device. It is also possible to co-synthesize IPs with other functions on the same programmable device.

The current target is Xilinx but both VHDL IP and C algorithms may be ported to other devices by Xilinx, for example to the ZINQ family which is in use in the NINANO space qualified processor board, or other non ITAR space FPGA from emerging European manufacturers.

Concerning the accelerometer, the current performance is close to the one obtained at cell level, and improvements have been identified on the packaging of the electronics. New generations of quartz cell are about to be tested with this electronic platform :

- Optimized vibrating beam for a better factor of merit
- Enlarged proof mass for a better scale factor at cell level

Parallel to that, further developments will now concern our Coriolis Vibrating Gyroscope, whose architecture is closer to the vibrating accelerometer than primarily supposed : the Drive mode resonance loop is the same as the one of the accelerometer, and the Sense output involves a second acquisition channel, parallel to and synchronized with the Drive, which is already part of the IP.

More generally, other vibrating sensors (not only inertial) working at resonance, or simply sensors working at a carrier frequency like differential bridges, may be addressed by the architecture. In most cases, the front end analog electronics are reduced to sensor head pre-amplifiers.

ACKNOWLEDGMENT

The authors wish to thank the Direction Générale de l'Armement (DGA) of the French Ministry of Defense, and the Centre National d'Etudes Spatiales (CNES), for their partial financial support.

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