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A Predictive Hybrid Pulse-Width-Modulation Technique for Active Front-End Rectifiers

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***Abstract*—Nowadays Active-Front-End (AFE) rectifiers are increasingly used as grid connected devices. Their efficiency and performances have become relevant for reducing the overall grid losses. This paper thus introduces a Predictive Hybrid Pulse-Width-Modulation (PH-PWM) technique, adaptable to any Space Vector PWM (SVPWM) controller. As opposed to hybrid PWM techniques based on sector partitioning, the PH-PWM technique selects the appropriate PWM sequence on-line with the help of a predictive algorithm. This selection is based on a cost-function where users can define a trade-off between various criteria, such as the reduction of current distortion and of switching losses, as presented in this paper. The use of the PH-PWM technique increases performances in comparison with the conventional PWM techniques. The simulation and experimental results are presented to confirm the effectiveness of the proposed PH-PWM technique. Aside from the trade-off capacity of the proposed PH-PWM technique, the simulation results validate a reduction of the switching losses for the converter up to 23% as compared with the conventional SVPWM technique.**

***Index Terms*—Bus-clamping PWM, Space Vector PWM, hybrid PWM techniques, Model Predictive Control, Active-Front-End rectifier**

I. Introduction

ACTIVE front-end (AFE) rectifiers are more and more being considered for use as grid-connected devices. When compared to the diode rectifiers, they enable a bi-directional power flow. They also offer a naturally low current distortion and cancel the requirement for heavy inductive filters between the grid and the rectifiers. Therefore, these topologies are increasingly used as active filters, to correct the power factor of loads or to compensate the lack of reactive power in the source grid. Due to good features, AFE rectifiers are the focus of many scientific papers. They aim to produce fast and reliable grid controllers that keep the current distortion low without increasing the size of inductive filters, which at the same time improves the efficiency of the rectifiers.

One possible control structure of an AFE rectifier is the direct controller. At each sample time, it enables the selection of the switching configuration to be applied on the converter. The Direct Power Control (DPC) [1] and the Finite Control Set Predictive-DPC (FCS P-DPC) [2][3][4][5] are both based on this working principle. More recently, a Modified Model Predictive Control (MMPC) was proposed in [6]. However despite its good dynamic performances, the direct controller approach suffers from a variable frequency spectrum and requires a high sampling frequency. Therefore in this study, a controller with a space vector Pulse Width Modulation (SVPWM) generator has been preferred, such as the Voltage-Oriented Control (VOC) [7] or the Predictive - DPC (P-DPC) [8][9]. Those controllers deliver the required dwell-times of the switching configurations to be used and the corresponding sector to the SVPWM generator that produces the switching sequence. For all controllers with a SVPWM generator, the switching frequency is fixed, and the constraint on the sampling time is reduced.

The modulation schemes have in the recent years become the center of a growing number of studies, due to their key role in the development of modern power electronics [10]. In particular, the SVPWM generator enables a precise application of the voltage reference to the AC-side of the converter. Furthermore, in SVPWM, a given voltage reference can be applied by different PWM sequences that lead to the same voltage in an average perspective over the PWM period, but have a specific current distortion and specific switching losses. Therefore, several Hybrid PWM techniques have been detailed in the literature as well as coupled PWM sequences. The by far most popular PWM technique is the conventional space-vector PWM (CSVPWM) because it implies a high line-side voltage and a low current distortion over a large range of modulation indexes [11]. However at high modulation indexes, the bus-clamping PWM (BCPWM) techniques represent good candidates [11] [9]. In one study [12], a hybrid PWM technique using a CSVPWM sequence and BCPWM sequences was developed to reduce the torque ripple linked to the q-axis current component in a permanent magnet synchronous motor. Novel specific BCPWM-type sequences were introduced in [13] and [14], enabling the production of new hybrid PWM techniques. In other investigations [14] [11], the aforementioned sequences were used in hybrid PWM techniques so as to reduce the resultant current distortion. Such hybrid PWM techniques were also used to reduce both current distortion and switching losses in [15], to diminish the acoustic noise of an induction motor in [16] or to lower the torque ripple of an induction motor in [17][18]. Recently [19] [20], new sequences were drawn for three-level converters and novel hybrid PWM techniques were introduced.

Although the aforementioned Hybrid PWM techniques achieve an improvement in comparison with CSVPWM, they

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are all based on a sector partitioning to select the appropriate sequence and are therefore fixed designs. For this reason, the latter hybrid PWM techniques cannot be optimized for all the existing operating conditions. The contribution of this paper is to propose a Predictive Hybrid PWM (PH-PWM) technique for an AFE rectifier, that can be coupled to any kind of SVPWM controller. The originality is that the PWM sequences are selected on-line by a predictive algorithm. The choice of the PWM sequence is based on a user-defined trade-off between various criteria, such as the current distortion and the switching losses. The trade-off can be adjusted on-line, which offers more flexibility than the existing hybrid PWM techniques and enables a better fitting to the working point under consideration. Independent of the used SVPWM-based controller, the proposed PH-PWM technique achieves both a better current Total Harmonic Distortion (THD) and lower switching losses through modulation without change of the AFE converter. Here, a conventional VOC is used since it is more reputed and since the contribution of this paper focuses on the modulation level.

The rest of the paper is organized as follows. Section II describes the AFE rectifier and its control scheme to indicate where the proposed PH-PWM is located. Section III introduces the principle of the PH-PWM technique, including the specification of the considered PWM sequences, the current distortion and switching loss predictions mandatory for the cost function calculation, and the predictive algorithm. Section IV analyzes the simulation results and Section V presents the experimental results and shows the effectiveness of the proposed solution.

II. The AFE rectifier and its control scheme

The considered AFE rectifier is composed of a basic three-leg two-level converter, a set of three inductances on the AC side and a storage capacitor connected in parallel to the load on the DC side, as depicted in Fig. 1. In order to control this structure, one can use a VOC controller, which is a vector control based on a rotating dq reference frame with the d-axis aligned with the grid-voltage. In this frame, the current behavior is described by the following model:

$$\begin{aligned} V_d &= -R \cdot i_d - L \cdot \dot{i}_d + L \cdot \omega \cdot i_q + V_{gridd} \\ V_q &= -R \cdot i_q - L \cdot \dot{i}_q - L \cdot \omega \cdot i_d + V_{gridq} \end{aligned} \quad (1)$$

where V_d and V_q are the d- and q- axis voltages on the rectifier side, i_d and i_q are the d- and q-axis currents, L and R are

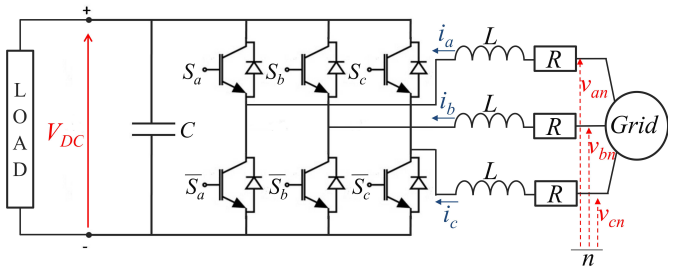

Fig. 1. Functional scheme of an AFE based on a three-leg two-level converter.

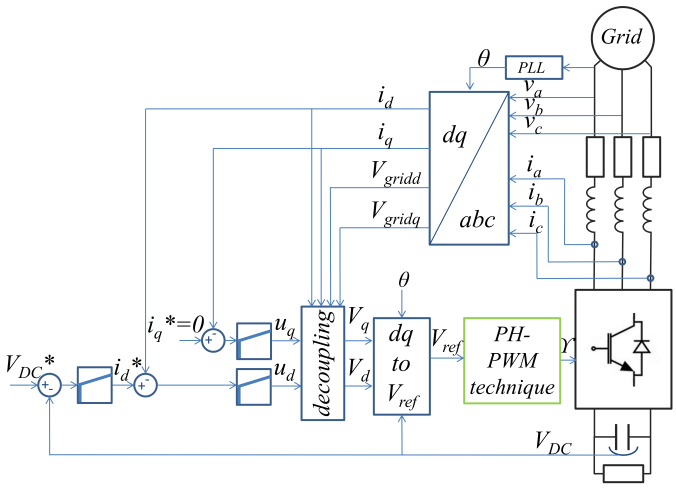

Fig. 2. Functional scheme of the complete VOC of the AFE rectifier with the proposed Predictive Hybrid PWM technique.

the line inductance and resistance, ω is the grid pulsation, and V_{gridd} and V_{gridq} are the projection of the grid voltage on the d- and q-axis, respectively. The functional scheme of the AFE controller is given in Fig. 2. To separately control the d- and q-axis currents, the decoupling terms $e_d = L\omega i_q + V_{gridd}$ and $e_q = -L\omega i_d + V_{gridq}$ are added to the outputs, u_d and u_q, of the current regulators, thus enabling the control of i_d and i_q by conventional proportional-integral (PI) controllers. To simultaneously achieve the control of the DC bus voltage and a unity power factor, a voltage PI controller delivers a current reference to the d-axis current controller. The q-axis current reference is set to 0. The resultant control voltages, V_d and V_q, are then translated into a voltage reference V_{ref} delivered to the proposed PH-PWM technique which is the focus of this paper and which is developed in the next section. The PH-PWM technique applies this voltage reference to the AC side of the converter taking into account its discrete characteristics. The resulting PWM sequence can be implemented with a dead-time compensation method as in [21].

III. The principle of the Predictive Hybrid PWM technique

The principle of the PH-PWM technique is drawn as a functional scheme in Fig.3. At each sample time $k.T_s$, where T_s is the sampling period of the VOC controller, it will select the appropriate PWM sequence, among a finite set Σ of N PWM sequences, and use it to apply $V_{ref}(k)$. This selection is based on a predictive algorithm, whose principle can be summarized in the following steps:

- At each sample time, k, the voltage reference, $V_{ref}(k)$, the three-phase currents, $i_{abc}(k)$, and the DC bus voltage, $V_{DC}(k)$, are acquired;
- For each considered PWM sequences, the prediction of the current distortion and the switching losses for the next sampling period, noted respectively $\Delta I^p_{SEQ}(k+1)$ and $P^p_{SEQ}(k+1)$, will be evaluated;

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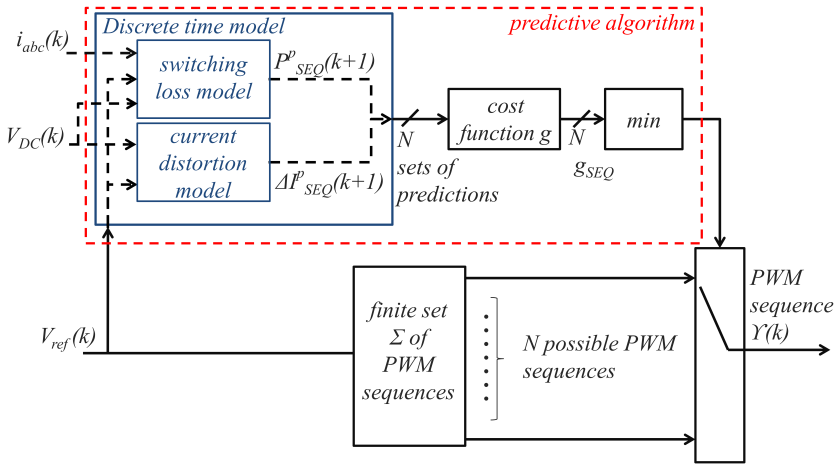

Fig. 3. Functional scheme of the proposed Predictive-PWM Technique.

- These predictions are integrated in a cost function, given in (2) , expressing the trade-off between the reduction of the current distortion and the lowering of the switching losses. In (2), β is a weighting factor enabling the user to adapt the cost function to its specifications;

$$g = \Delta I^p_{SEQ}(k+1) + \beta \cdot P^p_{SEQ}(k+1) \tag{2}$$

- The PWM sequence, $\Upsilon(k)$, whose predictions minimize the cost function, is selected, and applied to the drivers of the converter during the next sampling period.

As such, the predictive algorithm has some similarities to the FCS-MPC which has been extensively covered in the literature [22]. However, contrary to the FCS-MPC which acts on the current or power level, the predictive algorithm is used in a PWM generator. Thus, it has no impact on either the closed loop dynamic, or the system stability.

According to the aforementioned structure of the PH-PWM, we require definitions of the considered PWM sequences Σ and of the discrete-time model enabling the current distortion and the switching loss predictions. They will thus be the focus of the three following subsections.

A. The considered PWM sequences

As a conventional SVPWM generator, the PH-PWM tends, at each sample time, to apply the voltage reference delivered by the controller, $V_{ref}(k)$, in an average approach over a PWM period. It therefore considers this reference as a vector of a magnitude, $v_{ref}(k)$, and a phase lag, $\alpha(k)$, in the stationary reference frame (Fig. 4). It then applies the two nearest among the six existing active configurations for specific dwell times. The zero vector is set for the rest of the PWM period, T_{pwm}. The magnitude of vectors representing the active configurations in the stationary reference frame and $v_{ref}(k)$ are normalized with respect to $\frac{2}{3}$ of the measured $V_{DC}(k)$, and $v_{ref}(k)$ can then be defined as the modulation index. The sum of the resultant vectors equals $V_{ref}(k)$ in an average approach over the PWM period, as can be seen for sector I in Fig. 4. For this sector, between the active vectors 1 and 2, the dwell times $T_1(k)$ and $T_2(k)$ are calculated as in (3). The zero voltage vector will be applied during $T_z(k)$.

$$\begin{aligned} T_1(k) &= v_{ref}(k) \cdot \frac{sin\left(\frac{\pi}{3} - \alpha(k)\right)}{sin\left(\frac{\pi}{3}\right)} \cdot T_{pwm} \\ T_2(k) &= v_{ref}(k) \cdot \frac{sin\left(\alpha(k)\right)}{sin\left(\frac{\pi}{3}\right)} \cdot T_{pwm} \\ T_z(k) &= T_{pwm} - T_1(k) - T_2(k) \end{aligned} \tag{3}$$

The zero voltage vector can be applied by the two switching configurations 0 and 7, leading to the connection of the three phases of the load either on the negative or on the positive DC bus potential. Moreover, the active configurations can be

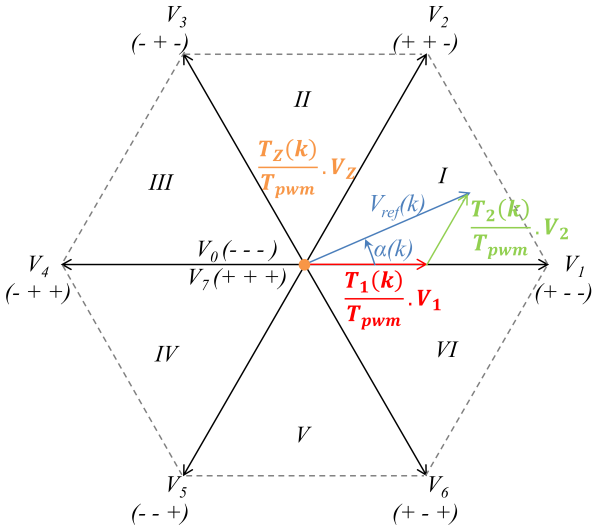

Fig. 4. Example of the application of a voltage reference on the load in the normalized stationary reference frame.

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applied more than once in the PWM period as long as the total application time equals the corresponding dwell time. A multiplicity of sequences leading to the application of the same value of $V_{ref}(k)$ arises from these facts. According to the criterium given in [14] and considering a maximum of three switchings per half PWM period, seven sequences emerge:

- the CSVPWM sequence (0127;7210), denoted 0127. In the example of Fig. 4, this corresponds to the application of vectors V_0, V_1,V_2,V_7 in the half PWM period. In the other half PWM period, a symmetrical sequence is applied as V_7, V_2,V_1,V_0. This leads to an equal partitioning of the zero vector between 0 and 7;
- the BCPWM sequences (012;210) and (721;127), denoted 012 and 721 respectively, that use either 0 or 7;
- the special BCPWM sequences (0121;1210), (1012;2101), (2721;1272) and (7212;2127), denoted respectively 0121, 1012, 2721 and 7212, which are derived from the BCPWM sequences by applying one of the active configurations twice.

In order to keep the switching frequency over the fundamental independent of the sequences, the PWM period of the BCPWM sequences is set to $\frac{2}{3}$ of the PWM period of the CSVPWM sequence [14]. The special BCPWM sequences possess the same PWM period as the CSVPWM sequence. These seven sequences form the finite set Σ of PWM sequences of the PH-PWM technique for the rest of the paper, even if more PWM sequences exist and improve other characteristics such as the common mode voltage. It has to be noted that the more PWM sequences that are included in Σ, the more the computational load increases. Therefore, in order to limit it, it is interesting to adapt the composition of Σ according to the user specifications.

Aside from the finite set of PWM sequences, the discrete-time model used in the predictive algorithm to predict the behavior of the converter and load association over the next sample time has to be developed.

B. The current distortion factor

The factor $\Delta I^p_{SEQ}(k+1)$, quantifying the current distortion over the next sample time for every PWM sequences, has to be defined.

Two approaches make it possible to define the current distortion due to the PWM sequences. This can be studied directly in the stationary reference frame and the phase currents kept as a three-phase system [23][24]. Another approach cancels the influence of the current fundamental on the current distortions [13][14][15][11][17]. It is based on a dq-frame that rotates synchronously with the voltage reference vector, V_{ref}, and whose q-axis is aligned with V_{ref}. As has been underlined earlier, the instantaneous three-phase voltages resulting from each PWM sequence achieve the value of $V_{ref}(k)$ in a average approach between the sample time k and the next sample time $k+1$. However each sequence leads to a specific instantaneous voltage error Δv over the PWM period, expressed in the dq-frame. The time integral of this voltage error is termed the stator flux ripple [15] and is denoted Ψ. When the phase-resistance of the load can be neglected, which is most often the case for the AFE rectifier, this stator flux ripple is directly proportional to the current ripple. Fig.5 gives as an example the evolution of Δv and Ψ in the dq-frame between the sample time k and the future sample time $k+1$ for a specific working point ($v_{ref}(k) = 0.75$ and $\alpha(k) = 20^o$) and for the sequence 0127, with two PWM periods per sampling cycle. The shapes of these curves depend on the actual working point, i.e., $v_{ref}(k)$ and $\alpha(k)$. As the PWM sequences differ in the succession of configurations they induce, the evolution of Δv over the PWM period, and thus of Ψ, is also specific to the used PWM sequence. In Fig.5, the use of a PWM sequence other than 0127 for this working point results in different values of Δv and Ψ. The RMS value of the current distortion over the PWM period between the sample time k and the next sample time $k+1$ enables a comparison of the current distortion induced by each PWM sequence, for the actual working point. It is derived from the RMS value of the stator flux ripple, developed for each sequence in [15], and leads to:

$$\begin{aligned}\Delta I^p_{SEQ}(k+1) &= \frac{V_{DC}(k)\cdot T_{pwm}}{3\cdot L}\cdot\big[C_{0(SEQ,\alpha(k))}\cdot v^2_{ref}(k)\\ &+ C_{1(SEQ,\alpha(k))}\cdot v^3_{ref}(k)\\ &+ C_{2(SEQ,\alpha(k))}\cdot v^4_{ref}(k)\big]^{1/2}\end{aligned} \quad (4)$$

Here, $v_{ref}(k)$ is the modulation index, $V_{DC}(k)$ the measured DC bus voltage, and the coefficients C_0, C_1 and C_2 depend on the chosen PWM sequence and on the phase lag $\alpha(k)$. They are taken from [15].

For the studied AFE rectifier with a phase inductance of 2.3mH and a DC bus voltage of 670V, Fig. 6 shows the evolution of the predicted value $\Delta I^p_{SEQ}(k+1)$ for an $\alpha(k)$ varying on the first sector for different PWM sequences with three different values of $v_{ref}(k)$. Due to the axis symmetry between the sectors, a study on the first sector is sufficient to determine the behavior over the entire stationary reference

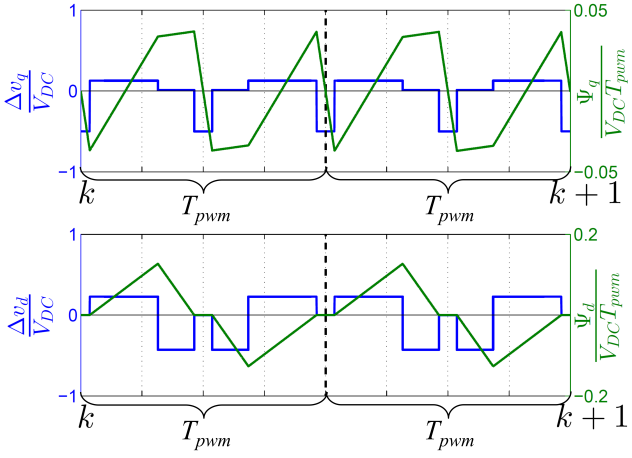

Fig. 5. Evolution of Δv and Ψ between k and $k+1$ for the PWM sequence 0127.

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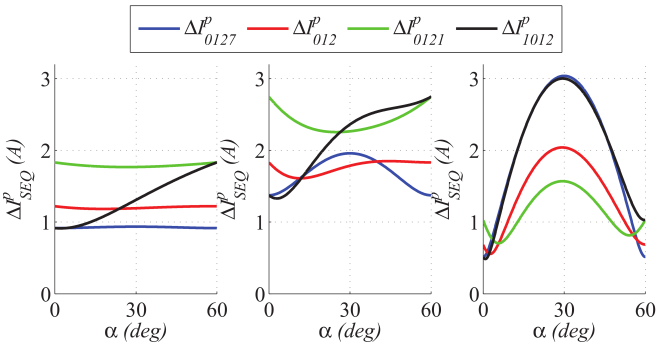

Fig. 6. RMS values of the current distortion for different PWM sequences with on the left side v_{ref}=0.2, on the middle v_{ref}=0.6 and on the right side v_{ref}=0.9.

frame. $\Delta I^p_{SEQ}(k+1)$ induced by the BCPWM sequences using the 0-configuration and the one using the 7-configuration are symmetric around the center of each sector [14]. Only the values of the sequences using the 0-configuration are shown in Fig. 6 for the BCPWM and special BCPWM sequences.

C. The switching loss factor

The second part of the discrete-time model included in the predictive algorithm of the PH-PWM is the factor $P^p_{SEQ}(k+1)$, which predicts the switching losses of the converter and load association between the sample time k and the following one, $k+1$, for each sequences.

If the PWM sequence implies a change of state in one inverter leg, then the energy lost in the switching process during the PWM period, T_{pwm}, is the sum of the turn-on and turn-off switching losses, E_{on} and E_{off}, of each IGBT and of the turn-off switching losses, E_{offD}, of each diode. These values are normally given in the datasheets of the IGBT/diode module for specific test conditions, V_{test} and I_{test}. By assuming that E_{on}, E_{off} and E_{offD} of one module are proportional to the DC bus voltage, V_{DC}, and to the phase current, i, their values are ruled by (5) [25].

$$\begin{aligned} E_{off} &= \frac{1}{2}\cdot\frac{2\cdot E_{off\ test}}{V_{test}\cdot I_{test}}\cdot i\cdot V_{DC} = \frac{t_{off}}{2}\cdot i\cdot V_{DC} \\ E_{on} &= \frac{1}{2}\cdot\frac{2\cdot E_{on\ test}}{V_{test}\cdot I_{test}}\cdot i\cdot V_{DC} = \frac{t_{on}}{2}\cdot i\cdot V_{DC} \\ E_{offD} &= \frac{1}{2}\cdot\frac{2\cdot E_{offD\ test}}{V_{test}\cdot I_{test}}\cdot i\cdot V_{DC} = \frac{t_{offD}}{2}\cdot i\cdot V_{DC} \end{aligned} \quad (5)$$

where t_{on}, t_{off} and t_{offD} are the resultant equivalent turn-on and turn-off times respectively, and $E_{on\ test}$, $E_{off\ test}$ and $E_{offD\ test}$ the energy losses in the test conditions.

A second-order behavioral model between the switching losses and the phase current is actually more accurate [25][26], but as $P^p_{SEQ}(k+1)$ has to be kept simple, the linear model is going to be considered. According to (5), this factor can be evaluated for the different PWM sequences as the sum of the energies lost in each leg in the switching process over a PWM period. It results in (6) for the sequence 0127:

$$\begin{aligned} P^p_{0127}(k+1) = &\frac{1}{T_{pwm}}\cdot V_{DC}(k)\cdot(t_{on}+t_{off}+t_{offD}) \\ &\cdot(|i_a(k)|+|i_b(k)|+|i_c(k)|) \end{aligned} \quad (6)$$

For the BCPWM sequences, it results in (7):

$$\begin{aligned} P^p_{SEQ}(k) = &\frac{3}{2T_{pwm}}\cdot V_{DC}(k)\cdot(t_{on}+t_{off}+t_{offD}) \\ &\cdot(|i_i(k)|+|i_j(k)|) \end{aligned} \quad (7)$$

where SEQ denotes 012 or 721, i and j denote the two non-clamped phases a, b, or c on the PWM period.

For the special BCPWM sequences, (8) is obtained:

$$\begin{aligned} P^p_{SEQ}(k) = &\frac{1}{T_{pwm}}\cdot V_{DC}(k)\cdot(t_{on}+t_{off}+t_{offD}) \\ &\cdot(2\cdot|i_i(k)|+|i_j(k)|) \end{aligned} \quad (8)$$

where SEQ denotes 0121, 7212, 1012 or 2721, i denotes the double-switching phase a, b, or c and j denotes the single-switching phase a, b, or c on the PWM period.

In short, with the acquired three-phase currents $i_{abc}(k)$, voltage reference $V_{ref}(k)$ and DC bus voltage $V_{DC}(k)$ at the current sample time, the predictions of the current distortion and the switching losses caused be each PWM sequence between k and $k+1$ will be quantified by using (4)-(8).

D. The predictive algorithm

According to the descriptions above, the predictive algorithm included in the proposed PH-PWM technique to select the appropriate PWM sequence can be formulated as an algorithm of Fig. 7.

According to the developed discrete time model, the results obtained with the PH-PWM technique are relatively independent of a variation of inductance of the input filter as long as this value is the same for the three lines. Indeed, since the current distortion model is based on the stator flux ripple for the different PWM sequences, the inductance value does not impact their order. The switching loss model will not depend on the input filter parameters. Thus the only effect of the variation of the inductance value is the same as a modification of the weighting factor β of (2), so it leads to a slightly different trade-off as opposed to the one that the user has defined.

IV. Simulation Results

In order to show the effectiveness of the proposed PH-PWM technique, the system which corresponds to the VOC controlled AFE-rectifier, presented in Fig. 2, will be simulated. The resulting electrical signals will be compared to the ones issued from the same VOC controlled AFE-rectifier using two other PWM techniques: the CSVPWM technique and the BCPWM technique. This simulation study will be performed for three different cases, corresponding to three user specifications. In the first considered specification, the user just wants to reduce

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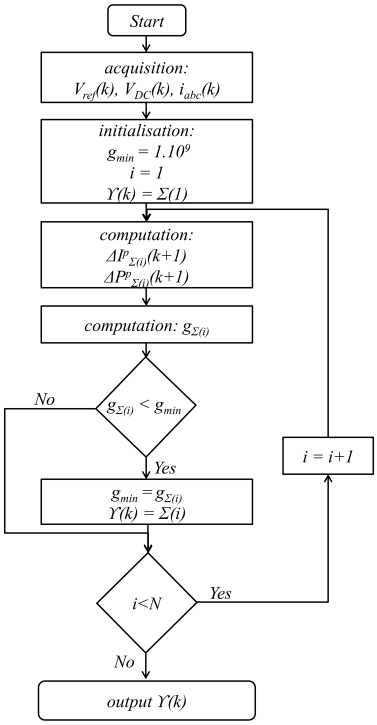

Fig. 7. Algorithm of the predictive algorithm that defines the PWM sequence to be used in the PH-PWM technique, with $\Sigma = \{0127, 012, 721, 0121, 7212, 1012, 2721\}$.

the current distortion. In the second specification, the user prioritizes the switching losses. In the last specification, the user wants to achieve a trade-off between the current distortion and the switching losses.

The complete system shown in Fig. 2 is modeled in Matlab/Simulink using the SimPowerSystem toolbox for the electrical elements. The grid is modeled as ideal three-phase voltages, whose values are set to represent the European grid. The line inductances are modeled with their parasitic resistances. The parameters are given in Table I. The resistive load is set to consume a nominal power of 4kW at a nominal DC bus voltage of 670V. All the physical parts are modeled with an ode23tb variable step-solver.

From a control point of view, the control loops of the VOC and the predictive algorithm of the PH-PWM technique are implemented with a sampling frequency, F_s, fixed at 3kHz. The PWM sequences are created with a frequency of 2.25MHz, offering a decimation of 250 points per PWM period for the BCPWM sequences.

TABLE I
PARAMETERS USED FOR THE SIMULATION

Grid frequency ω (Hz)	50	Grid peak voltage V_{peak} (V)	325,27
Line inductance L (mH)	2.3	Line parasitic resistor R (Ω)	0.6586
Storage Capacitor C (mF)	9.4	Sampling frequency F_s (kHz)	3
PWM frequency CSVPWM and special type BCPWM F_{pwm1} (kHz)	6	PWM frequency BCPWM F_{pwm2} (kHz)	9

A. Specification 1: reduction of the current distortion

In order to fulfill this specification, the cost function defined in (2) is modified as (9):

$$g = \Delta I^p_{SEQ}(k+1) \tag{9}$$

As the input voltage is set to the fixed grid voltage value given in Table I, the impact of the DC bus voltage level and the modulation indexes is analyzed. The reference of V_{DC} is set to different values from 600V to 1000V. In this case, the resistive load is adapted according to the operating conditions in order to consume the nominal power.

For each considered operating point, VOC is simulated using the PH-PWM technique, the CSVPWM technique and the 30^o clamp, which is the BCPWM technique offering the lowest current distortion. In this last technique, the change of zero configurations used is made at the middle of every sector, so that each phase is clamped in the middle 30^o duration in every quarter cycle of the fundamental [13]. To quantify the results, the RMS value of the current distortion over several periods of the fundamental is calculated according to (10):

$$\Delta I_{RMS} = \sqrt{\frac{1}{N_s}\sum_{i=1}^{N_s}(di_a)^2} \tag{10}$$

Here N_s is the number of samples (1.10^6 samples), di_a is the instantaneous current distortion of the first line current i_a, and is defined as the difference between the instantaneous current i_a and its fundamental.

The simulated results are given in Fig. 8 according to the voltage reference. For a low DC bus voltage, the modulation index is high, and the 30^o clamp therefore gives less current distortion. As the DC bus voltage increases, the modulation index drops, and the CSVPWM technique becomes more interesting with regard to the current distortion. For all the conditions, the PH-PWM technique demonstrates the lowest current distortion.

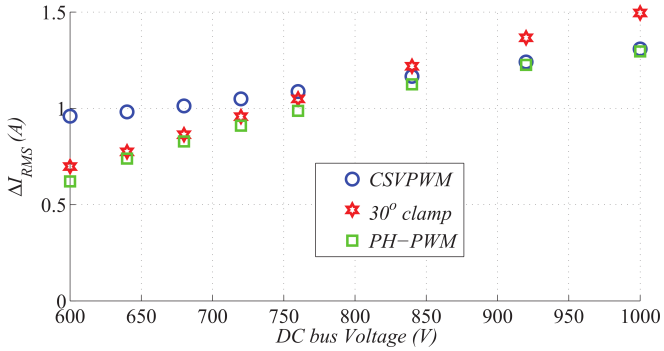

Fig. 8. Simulated RMS values of the current distortion for the three considered PWM techniques.

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B. Specification 2: the reduction of the switching losses

In this specification, the user focuses on the switching losses of the converter. This means that the cost function described in (2) becomes:

$$g = P^{p}_{SEQ}(k+1) \tag{11}$$

The performances of the hybrid PWM techniques developed in literature regarding the switching losses are highly dependent on the phase lag between the three-phase currents and the three-phase voltages. Therefore, in order to quantify the performances of the PH-PWM technique compared with the other PWM methods, the DC bus voltage is set to its nominal value 670V. The q-axis current reference, and thereby the reactive power, varies in order to change the phase lag between the three-phase voltages and the resultant three-phase currents.

The simulation results obtained with the PH-PWM technique are compared with respectively the ones with the CSVPWM technique and with those of the continual BCPWM techniques. The continual BCPWM techniques lead to the clamping of every phase continually for a 60^o duration in every half cycle of the fundamental. The angle at which the change between the two zero configurations is made in the sectors, noted γ, can vary from 0^o and 60^o, and it shifts the clamping duration on the half cycle of the fundamental, resulting in different continual BCPWM techniques. These achieve the lowest switching losses among the BCPWM techniques [13]. The common 60^o clamp, for example, has a γ of 30^o, leading to a clamping of each phase in the middle of every half cycle of the fundamental, and thus to the lowest switching losses at unity power factor. Fig. 9 presents the simulated switching losses normalized by the switching losses obtained with the CSVPWM technique. In this plot, the dotted lines represent the raw simulation data and the solid lines correspond to the resulting polynomial curve fitting. As can be seen, the switching losses with the continual BCPWM techniques have a local minimum at a phase lag of -30^o, 0^o or 30^o depending of the value of γ. The proposed PH-PWM technique demonstrates a better reduction of the switching losses independently of the phase lag. It leads to a constant reduction of the switching losses close to 23% in comparison to the CSVPWM technique, whereas the 60^o clamps only enable a reduction of at most 16% in comparison with the CSVPWM.

C. Specification 3: the trade-off between the current distortion and the switching losses

When the user wants to make a trade-off between the current distortion and the switching losses, (2) has to be implemented as the cost function, and the user has to choose the weighting factor β. To show the influence of β, the simulated normalized switching losses and the simulated normalized current distortion obtained with the PH-PWM technique on the nominal operating point are given in Fig. 10. Here, β is varied from 0 to 0.21, and the CSVPWM technique serves as a reference. As can be seen, an increase in β leads to a decrease of the switching losses and an increase of the current distortion. The resultant values of the switching losses and current distortion stabilize for higher values of β and converge in a slower manner to the values obtained for $\beta = \infty$. The distortions on the switching losses presented in Fig. 10 are due to the fact that the switching between two PWM sequences is not taken into account, leading to a difference between the estimated switching losses and their real counterparts.

According to the latter curves and for the nominal operating point, an appropriate trade-off can be obtained by fixing the weighting factor β to 0.039. This enables a 12.7% reduction of the switching losses, and still 10% less current distortion than the CSVPWM technique. Once the value of β is set, the AFE-rectifier controlled by VOC using the resulting PH-PWM technique is simulated for a change in the load from its nominal value to half of its nominal value. The simulated i_a, the simulated switching losses and the simulated V_{DC} are given in Fig. 11 and are compared to the ones obtained with the CSVPWM technique. As can be clearly seen in Fig. 11, the PH-PWM technique enables a reduction of both the current distortion and the switching losses in comparison with the CSVPWM technique without impacting the DC bus voltage. Both PWM techniques lead to the same DC bus voltage (Fig. 11).

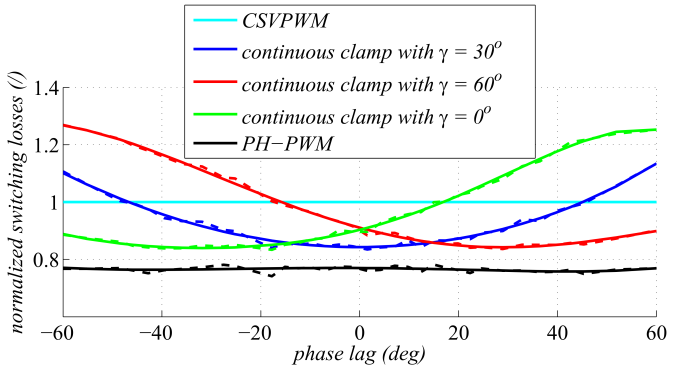

Fig. 9. Normalized switching losses obtained in simulation for the considered PWM techniques vs the phase lag between the current and the voltage systems.

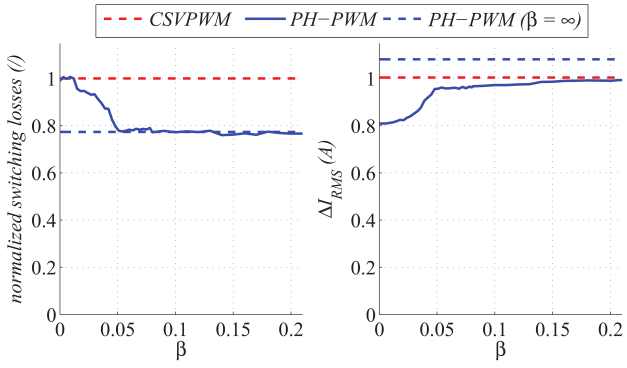

Fig. 10. Normalized switching losses and normalized current distortion for the PH-PWM technique for different values of β.

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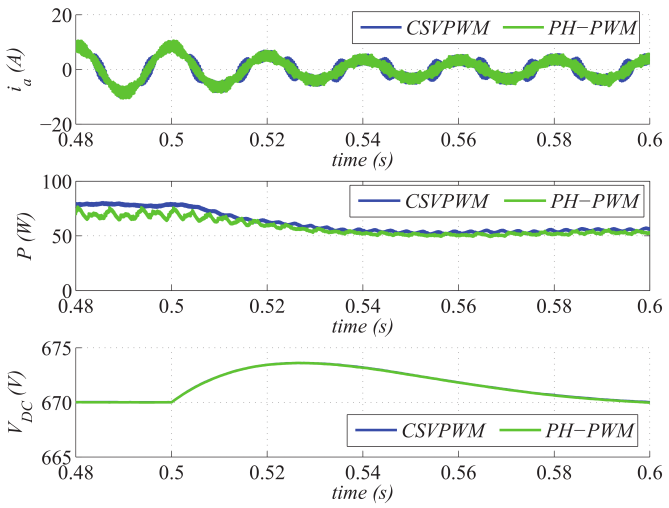

Fig. 11. Simulated waveforms of line current, i_a, switching losses, P, and DC bus voltage, V_{DC}, for a $\beta = 0.039$.

It has to be noted that the shape of the curves presented in Fig.10 depends slightly on the working point, leading to a variation of the gains obtained with PH-PWM. However, this effect can be countered by an on-line variation of the weighting factor β.

According to Figs. 8-11, the simulation results presented in this section make it clear that the use of the PH-PWM technique enables an increase in performances of the controlled AFE rectifier. It shows the ability of the proposed PH-PWM technique to reduce both the current distortion and the switching losses in this grid connected device. It also demonstrates the adaptability of the proposed design.

V. Experimental results

A set of experiments has been realized on a laboratory test bench. It is supplied by the grid through an autotransformer with a fixed reduction ratio of 1/4 for safety reasons. As both the current distortion and the switching losses are proportional to the DC bus voltage, it is assumed that if the experimental results validate the simulation results, an increase in the DC bus voltage can only benefit the proposed design. The output of the autotransformer is linked to a set of three inductances connected to the AC side of an Arcel 17kW three-phase two-levels converter. Its parameters are given in Table I.

From an implementation point of view, the VOC and the predictive algorithm of the PH-PWM technique are implemented on a dSPACE DS1006 with a sampling frequency F_s of 3kHz. The creation of the PWM sequence, the addition of the dead-time ($3\mu s$) and the PWM sequence selector are implemented on a dSPACE DS5203 FPGA board. The choice of the PWM sequence is communicated at each T_s at the same time as $V_{ref}(k)$ between the two boards. To ensure the acquisition of the many electrical signals at a proper time independently of the used PWM sequence, the PWM period, T_{pwm}, is set to $2.T_s$, leading to a PWM frequency of 6kHz for the CSVPWM sequence and for the special BCPWM sequences, and of 9kHz for the BCPWM sequences. The clock frequency of the FPGA is fixed on the DS5203 at 10MHz, enabling over a thousand points per PWM period and thus a high resolution.

The tests on a VOC-controlled AFE with the PH-PWM technique are performed for specification 1 and specification 3. The studied working points are adapted in order to keep the same modulation indexes as in the simulation section.

A. Specification 1: the reduction of the current distortion

Fig. 12 presents the experimental RMS values of the current distortion calculated with (10) when (9) is used as a cost function for the PH-PWM technique. The DC bus voltage is set between 150V to 250V, and the resistive load consumes 1kW. Due to the low DC-bus voltage values, the current distortions as well as the resulting gains obtained with the proposed PH-PWM technique in comparison to the two other PWM techniques presented in Fig. 12 are lower than the ones obtained in simulation. However, if the DC bus voltages are normalized with respectively 1000V for the simulation and 250V for the experimentation, the normalized ranges where the CSVPWM technique and the 30^o clamp demonstrate better results are mostly respected when compared with the simulation results. Furthermore, when the gains obtained with the proposed PH-PWM technique are expressed in percent of the RMS values of the current distortion of the other techniques, comparable values in simulation and in experimentation are achieved. Nevertheless, the obtained experimental results prove that the proposed PH-PWM technique is able to reduce the current distortion when (9) is used as the cost function.

The spectral decomposition of the current distortion obtained in experimentation for a DC bus voltage of 150V, 190V and 250V is given in Fig. 13. It can be seen that in the higher frequency range, the PH-PWM technique presents lower harmonic peaks than the two other techniques regardless of the studied operating point. These peaks are spread over the two PWM frequencies, F_{pwm1} and F_{pwm2}, defined in Table I, since all the possible PWM sequences are used. In the lower frequency range, the spectral decompositions of the line current present significant harmonic peaks for all the PWM

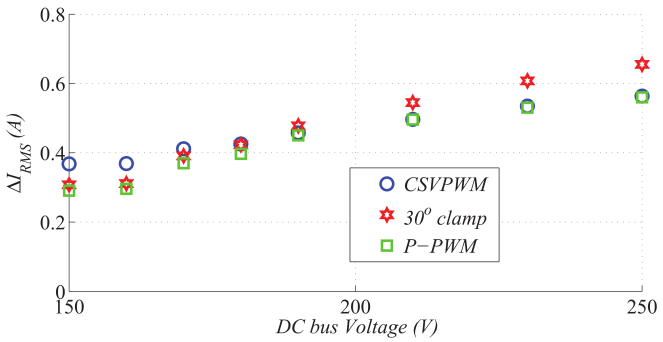

Fig. 12. Experimental RMS values of the current distortion for the three considered PWM techniques.

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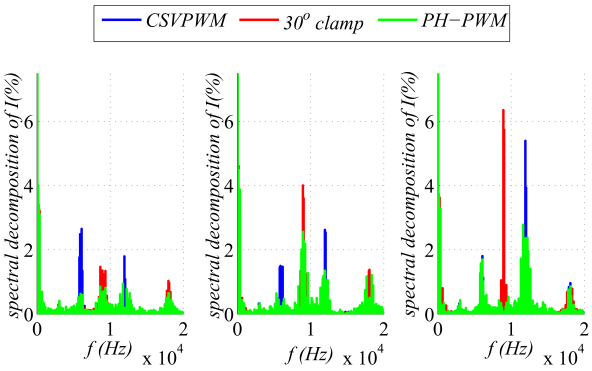

Fig. 13. Experimental spectral decomposition of the line current for the three PWM techniques for a DC bus voltage of 150V, 190V and 250V, respectively.

techniques and all the DC bus voltages. They are mostly due to the harmonic distortions of the voltage grid that are not completely canceled by the decoupling in VOC. These current harmonics result in a THD value calculated for the first 30 harmonics, varying between 4.7% and 6.7%. Throughout, there is no correlation between the use of a specific PWM technique and the minimization of the THD for the first 30 harmonics. Thus, the proposed PH-PWM technique enables a reduction of the current distortion in the higher frequency range without significantly impacting the lower frequency range.

B. Specification 3: the trade-off between the reduction of the current distortion and the switching losses

To validate the trade-off ability of the PH-PWM technique as well as its capacity to reduce the switching losses, the DC bus voltage is set to 160V and the resistive load is adapted in order to consume 1kW. Here, (2) is used as the cost function. To quantify the resulting reductions of switching losses, the temperature variation on the converter using the PH-PWM technique is measured with a FLUKE TI9 thermal camera and normalized with the one obtained with the CSVPWM. The use of a thermal camera makes it possible to avoid the installation of a temperature sensor directly on the converter used in the laboratory, and still offers the required precision. Furthermore, it delivers a global overview of the temperature of the converter. Fig. 14 presents the normalized temperature variation and the current distortion versus the weighting factor β. The results obtained with the CSVPWM technique are given as a reference. The figure proves the predicted behavior: an increase in β induces a decrease of the temperature variation for the converter and an increase of the current distortion. The maximal gain obtained with regard to the temperature variation is about 8.21% and involves both the conduction and the switching losses for the converter. Fig. 15 shows the temperature increase measured for a test of two hours for the PH-PWM technique when β is very large and for the CSVPWM technique. The figure displays a reduced overall temperature increase for the PH-PWM technique in comparison with its CSVPWM counterpart.

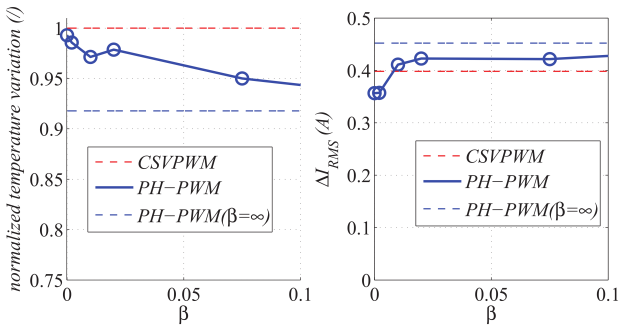

Fig. 14. Evolution of the temperature variation on the converter and of the current distortion vs β for the PH-PWM technique (experimental results).

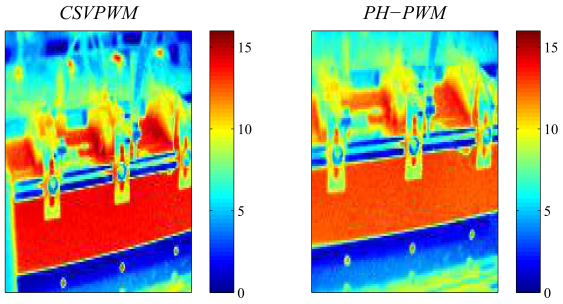

Fig. 15. Temperature increase in degrees Celsius measured for the converter for the CSVPWM technique and for the PH-PWM technique.

According to Fig. 14 and to the operating point, fixing β in the cost function (2) at 0.075 enables a reduction of 5% of the temperature variation for the converter for a small increase of the current distortion of 0.02A in comparison with CSVPWM. The measured i_a resulting from this operating point is given in Fig. 16 for a β of 0.075, and shows the closed-loop behavior of the complete VOC controlled AFE rectifier. One can also decide to keep the same current distortion as with the CSVPWM by setting β at 0.0083, leading to a temperature increase that is reduced by 2.55%.

Therefore, both the reductions with regard to the current distortion and the switching losses as well as the trade-off ability of the PH-PWM technique are validated by experimental results. Furthermore, in the proposed technique, the weighting factor β can be tuned on-line by a supervisor, in order to more accurately fit the working conditions.

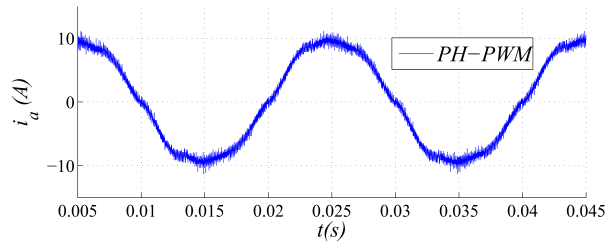

Fig. 16. Measured i_a for the considered working point and for the PH-PWM technique with $\beta = 0.075$.

VI. Conclusion

This paper describes the integration of a PH-PWM technique in a VOC to control an AFE-rectifier. The method selects the appropriate PWM sequence on-line according to the operating point with the help of a predictive algorithm applied at the level of PWM generation. The effectiveness of the proposed PH-PWM technique has been validated both in simulation and in experimentation, and was found to enable larger reductions of both the switching losses and the current distortions in comparison with the conventional PWM techniques. Furthermore, the trade-off between the current distortion and the switching losses can be adapted by fixing a weighting factor. This weighting factor can also be varied on-line, enabling us to increase the range of performance improvements that are attainable with the proposed PH-PWM. Consequently the resulting PH-PWM technique offers increased performances in comparison with existing PWM generators. The proposed PH-PWM technique can be associated with other PWM based controllers, such as a Predictive Direct Power Controller, to improve the performance of an AFE rectifier both with regard to power control and modulation. This association enables a fixed switching frequency as well as a lower computational load in comparison with the direct control methods. The PH-PWM technique can be extended to enable a reduction of other parasitic phenomena, such as the common-mode-voltage, by taking into account their models in the cost function.

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