High density SOT-MRAM memory array based on a single transistor

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***Abstract*—Spin Orbit Torque Magnetic RAM (SOT-MRAM) approach represents a new way to overcome over Spin Transfer Torque (STT) memory limitations by separating the reading and the writing paths. It is particularly interesting for high speed applications that do not require very high density because of two transistors per bit cell. This paper presents a high density SOT-MRAM memory array based on a single transistor and a unidirectional diode. There are three advantages of this approach. The number of transistors for 32kb memory array is decreased by factor of 45% which leads to an improved cell density by 20% compared to conventional SOT bit cell. Moreover, it requires less control to read operation and finally high endurance, high speed and high density can be achieved. The key challenge going will be to adjust between sense margin and read energy.**

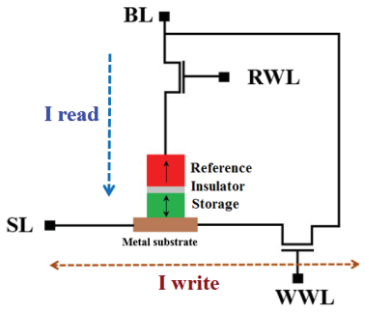
Keywords: SOT-MRAM, unidirectional diode, high density, high endurance

I. INTRODUCTION

Emerging technologies to replace DRAM and SRAM memories are crucial for microelectronics industry. The access time of these work memories is fast, but their capacity of storage is not large and they are volatile. Additionally, refresh energy of DRAM and leakage current of SRAM are big sources of power dissipation [1]. Magnetic Random Access Memory (MRAM) is one of the best candidates for the replacement of DRAM and SRAM. Although a significant attention is given to the Spin Transfer Torque (STT) as the potential candidate for future memories, it suffers from weaknesses:

- The high drive current needs a large access transistor leading to an increased area.
- The current conduction through the tunnel junction decreases reliability because of the high voltage.
- The achievement of a reliable reading without ever switching the cell remains a challenge (since writing and reading operations share the same path).

For these reasons, it is of great interest to pursue exploring technologies for MTJ based MRAMs which provides a better reliability. The recent discovery of Spin-Orbit Torque (SOT) is leading to a new technology called SOT-MRAM. This promising technology combines non-volatility, high speed, zero standby leakage, and good reliability. SOT allows switching the magnetization of storage layer by different possible mechanisms. These mechanisms issued from the spin orbit interaction are often named the Rashba effect originating from the interfaces between the different layer and the Spin Hall Effect for the contribution of the bulk of the materials [2, 3].



Operations	*Write '1'/'0'*	*Read*
WWL	V_{DD}	0
RWL	0	V_{DD}
BL	V_{Write} / 0	I_{sense}
SL	0 / V_{Write}	0

(a) (b)

Figure 1. (a) Schematic of the three-terminal SOT device and the the two independent paths (b) Signal control for memory operation.

A typical structure of SOT, as shown in figure 1, consists of a MTJ mounted on heavy metal substrate. The resistance of MTJ is high/ low when the magnetization of reference and storage layer is respectively antiparallel/ parallel due to the Tunnel Magneto Resistance (TMR) effect [4]. Two transistors per bit cell are required in order to properly control write and read operations. For memory write, write word line (WWL) is set to V_{DD} and the write access transistor is switched on. Then, positive write voltage on BL (or SL) is applied in order to write logic '1' (or '0'). For memory read, read word line (RWL) is set to V_{DD} and the read access transistor is switched on. A sensing current (I_{sense}) flowing through the junction generates a sensing voltage which can be detected by a sense amplifier.

Great benefits are obtained by separating the writing and reading paths: firstly, risks of accidental writing during reading are reduced. Secondly, high endurance is guaranteed (>5x1010) and the switching duration can be very fast (210 ps) experimentally demonstrated in [5].

The main limitation of this technology compared to STT is apparently the area density because of the additional terminal. Hence, in this paper, we study a new structure of SOT-MRAM design using one transistor and one diode per bit cell.

II. DIODE BITCELL STRUCTURE

The key idea to improve the area density of SOT-MRAM is to use one transistor per bit cell so that we can obtain a similar density as DRAM and STT-MRAM.

Figure 3 represents the architecture of 4x4 SOT-MRAM memory array based on a single transistor for writing and a unidirectional diode for reading. The diode passes unidirectional current through MTJ during reading operation only, so zero leakage current is passing during write mode. When a bit cell memory is selected in programming mode, all the transistors (t_i) of multiplexer are kept deactivated. WWL1, write (wr), and access column (ac1) transistors are set to V_{DD} to write the first cell. Positive write voltage on BL (or SL) is applied so that the current is flowing from BL to SL through the conductive layer to write '1' logic (or '0'). On the other hand, when a memory cell is selected in reading mode, wr transistor and WWL_i are kept low and the diode selector has to be polarized in forward mode to deliver the maximum current through the memory point. BL is decoded with two stage nMOS transistors t_i and ac_i and a diode. It generates a sensing current flowing through the junction which can be detected by sense amplifier. Since t_i and ac_i properly control the selected junction, zero current flows through unselected cells so the resulting leakage is negligible.

As shown in Figure 2, the diode is formed by the junction of two semiconductors doped with opposite sign, i.e. a p-n junction. Compared to conventional SOT-MRAM which is based on two transistors, the area density is approximately improved by 20%.

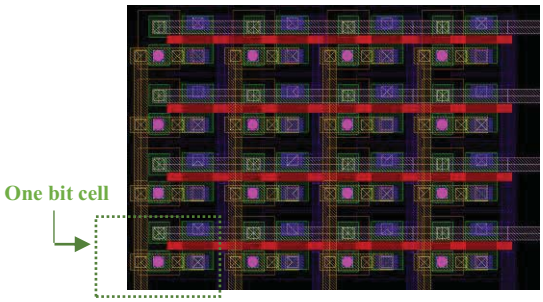


Figure 2. Layout of 4x4 memory array where the diode is forming by a simple PN junction.

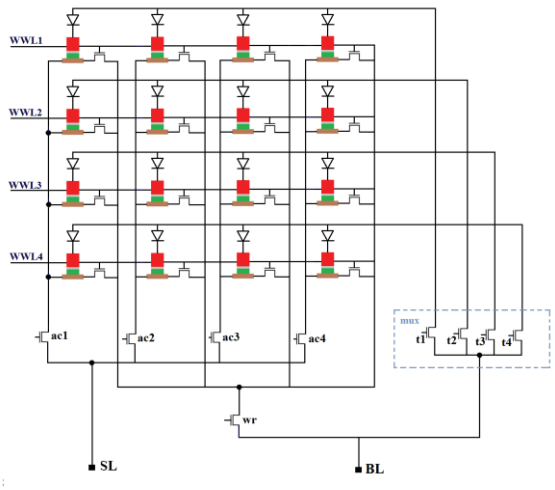


Figure 2. Equivalent schematic of 4x4 SOT-MRAM memory array based on a single transistor and one diode

III. ELECTRICAL CHARACTERISTICS

In terms of reading, correct functioning of the 1 diode-SOT-MRAM requires robust read. It requires a larger read voltage to overcome the diode's ON voltage and generate the required read current. The corresponding BL should be set to $V_{DD} - V_T$ where V_T is the threshold voltage of diode ~ 0.7V. A new bidirectional threshold switching selector with 0.3V threshold voltage is proposed in [6] and used for selector diode STT-MRAM crossbar arrays in [7].

Figure 4 shows the current substractor read circuit based on current mirror. In every read operation, Read signal (Re) is set to V_{DD}, t_i, and ac_i are selected to discharge BL. The read cell currents flow from BL to the accessed MTJ, then the current difference caused by the resistance of MTJ is converted into a difference of voltage. This difference is detected by using sense amplifier to output read data, out. The penalty of using this scheme is that the size of driving nMOS should be increased a little. The diode then requires applying a relatively higher Vread due to the drop of voltage across it in order to supply the required Isense. The characteristic curve of read mode to enable good read current is represented in figure 5.

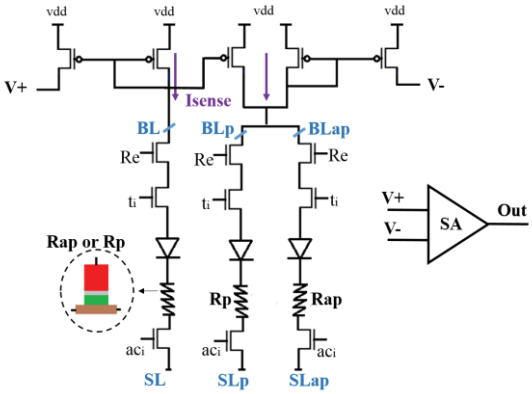


Figure 3. Circuit state in array read mode

It shows that the turn ON diode is > 11μA when the forward bias on BL reaches 800mV. In order to generate the maximum current flowing through the MTJ, read path should be in the relatively lower resistance.

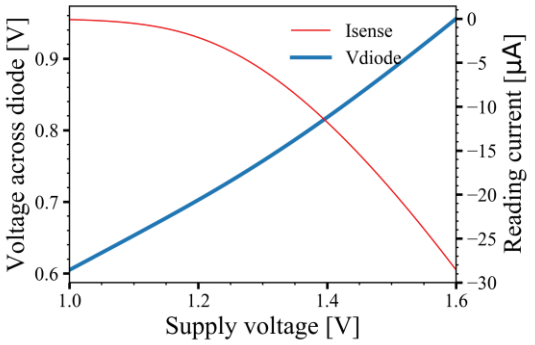


Figure 4: Dependence of voltage supply on reading current

By simulating a read operation including different value of parallel resistance junction value (R_p) with different TMR, we can see in Figure 5 that the higher Rp can improve the sense margin. To maximize the sense margin, it is important to select the ideal value of R_p with higher TMR respecting the required read current. On the contrary, high resistance of the MTJ can not only greatly improve the sense margin but also increase the read energy. Thus, there is a tradeoff between sense margin and read energy.

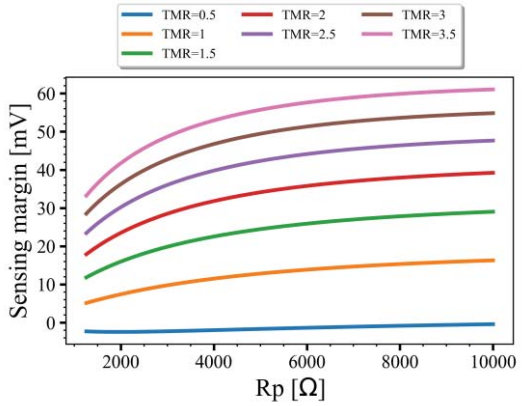


Figure 5: Dependence of parallel resistance junction on reading current for different TMR value

We compared the conventional SOT-MRAM structure (as shown in figure 1(a)) to the proposed cell based on one transistor and one diode (see Table I). The conventional SOT-MRAM has larger area than that of the proposed due to the need of a second transistor during read operation. The replacement of this transistor by a diode leads to reducing the number of transistors by 45% and less control for these transistors in the logic part.

Since read and write operations are completely separated, no current passes through diode during writing so we can obtain the same write power in these two structures. However, the read power seems to be larger than that of the conventional structure because the read voltage had to be increased to overcome the diode forward mode.

TABLE I. RESULTS COMPARISON BETWEEN 2T/1MTJ AND 1T/1DIODE/1MTJ OF SOT-MRAM CELL

	2T/1MTJ SOT-MRAM	*1T/1diode SOT-MRAM*
Technology	28 nm	28 nm
Cell size	118 F^2	95 F^2
Write power	99 μW	99 μW
Read power	7 μW	18 μW
N for 32kb memory array	73728	40960

N: number of transistor

I. CONCLUSION

We studied a high density SOT-MRAM memory cell based on a single transistor and one diode per bit cell where zero leakage power is achieved thanks to a separated write/ read paths. The diode is introduced during read operation instead of a transistor to reduce the area density and the logic control part. In addition the number of transistors is reduced by 45% for 32kb memory array and the area density is improved by 20%. For further density improvement, this diode can be developed by materials elements since minimizing the bit cell area is limited by the design rules. Moreover, unidirectional metal-insulator-metal diode can be integrated in series with the MTJ to achieve a higher memory density.

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