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Impact of Different Transistor Arrangements on Gate Variability

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Abstract

This paper evaluates a set of complex cells with different transistor arrangements that implement the same logic function. These cells were evaluated under nominal conditions and with gate variability at layout level. The purpose is to verify what topology is more appropriate to increase the robustness of cells regarding the process variability issues. Results emphasize the importance of investigating the effects caused by process variability in FinFET technologies, as the electrical characteristics of circuits suffer significant changes. In general, the best choice is to use the network that the transistor in series is as far as possible to the output node. However, a trade-off needs to be done due to performance and power consumption penalties.

1. Process Variability on Nanotechnologies

For continuing with the technology scaling on sub-22nm, novel materials and new devices architectures had to be adopted in integrated circuit designs [1]. Multigate devices were introduced with the objective of overcome obstacles encountered in standard Complementary Metal Oxide Semiconductor (CMOS) technologies and keep scaling [2]. FinFETs gained prominence for presenting an excellent short-channel effects (SCE) control, reduced leakage currents, high driving capability, better yield, and the fabrication process compatible to the conventional CMOS [3].

The emerged technologies raised relevant topics related to reliability and robustness that to need to be investigated. The process variability still as one of the most significant challenges in nanometer regime becomes even more meaningful in designs based on FinFET technology. The sub-wavelength lithography introduced difficulties in transferring the small geometric patterns required by the layout of nanometer technologies to the substrate surface [4]. The side effect is that this manufacturing step impacts directly on the transistor threshold voltage (V_{TH}).

FinFET technologies use high-k/metal gate stack to improve the gate control on the channel region [5]. Thereby, the Metal Gate Granularity (MGG) has been identified as a source of statistical variability. The orientation of the grains used in the gate is not considered ideal as a unique metal uniformly aligned. The metal gate having different work-functions (ϕm) randomly aligned that implies in higher work-functions fluctuations (WFF) [4,6]. Moreover, the imperfections caused by process variations can influence the fin height, fin width, fin-to-fin similarity, and the resistance MOL (Middle of Line).

All these factors can compromise entire blocks of cells because they modify the transistor structure. Therefore, the electrical properties of the circuits also suffer deviations [7]. The impact on performance and power metrics can accelerate the circuit degradation besides introducing errors in the circuit functionality. The consequence is the parameter yield loss leading to a higher cost of fabrication. This emphasizes the importance of creating new design guidelines able to deal with the challenges imposed by the process variability in nanometer technologies.

Many related works studied the challenges and the impact of variability in the circuits and devices at nanometer technologies [6-11]. The influence of the variation of the main geometric parameters on the currents I_{ON} and I_{OFF} of FinFET transistors considering a set of predictive FinFET technologies sub-22nm was analyzed in [12]. In [13], the impact of Process, Voltage and Temperature (PVT) variations in timing and power on a subset of circuits using a commercial standard cell was studied. Different transistor sizing techniques were applied in FinFET circuits with PVT variations in [14]. However, there are only few approaches in the literature to mitigate the variability effects. The replacement of traditional inverters by Schmitt Triggers (ST) into near-threshold full-adder architecture was proposed by [15] as a process variability mitigation technique. Their results showed a significant reduction in timing and power deviation at 16-nm bulk CMOS technology. The similar analysis was done in [16].

Transistor arrangement optimization is a technique used to design faster circuits [17], but also to deal with Bias Temperature Instability (BTI) effects [18] or to improve design robustness against permanent and transient faults. The adoption of complex gates reduces the transistor number that is correlated to the area and also, reduces the delay and power consumption. Some logic cells can be designed using different kinds of transistor networks [19]. It is well known that different transistor combinations, that implement the same logic function, present different electrical and physical characteristics as well as distinct behavior under process variations [18].

In this context, this work evaluates the electrical characteristics of a set of complex gates with different transistor arrangements considering the ideal behavior and a realistic behavior, i.e., with WFF variations. The more suitable topology to process variability mitigation is analyzed. Moreover, gains and penalties regarding performance and power consumption were investigated alongside variability robustness. The set of information provided here helps the designers to choose the most appropriate physical layout depending on the target application.

Section II shows the methodology adopted in this work. A review about the 7nm FinFET technology from ASAP and the layout techniques are presented in Section III. Section IV and V propose a description of simulation and a discussion of the results.

2. Methodology

This work evaluates the impact of process variability on different transistor arrangements. Fig. 1 shows the design flow adopted in this research. First, a set of six complex gates of 3 to 5-inputs was chosen to perform this analysis. This choice was made due to the cells present serial transistors allowing more than one topology type. All complex cells are designed with symmetric sizing such that NFET and PFET transistors have the number of fins equal to three.

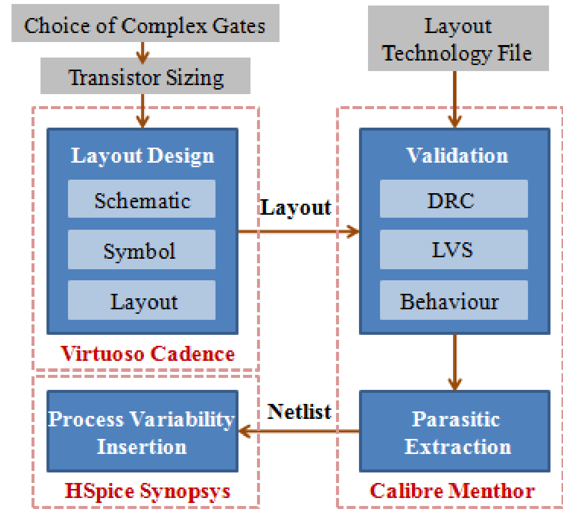

Fig. 1 Design flow of the experiments

Fig. 2 presents different transistor arrangements for a set of four complex gates. For the gate AO21, in the pull-up network, the serial transistor with the signal *a* on the input can be connected close or far related to the cell output terminal. In other gates, when possible, this work also explores an intermediate place in the middle of the cell, as illustrated on AOI211 and AOI221. As a general rule, AOI gates have the alternative transistor arrangements explored in the pull-up network. On the other hand, the OAI gates explored different pull-down network options, as Fig. 2 demonstrates for the OAI21 function. The complementary networks do not need to be rearranged because the transistors are associated in parallel.

The purpose of the next stage was dedicated to the development of the schematic and the physical layout for all investigated complex gates. The layouts were submitted to the physical verification flow composed by DRC (Design Rule Check) and LVS (Layout Versus Schematic) steps. Both steps are based on the

technology rules of the 7-nm FinFET Predictive Process Design Kit (ASAP7) developed at Arizona State University in partnership with ARM Ltd [20]. The main parameters of this technology are summarized in the Table I. The behavior of each complex gate is verified to certificate that it implements your function correctly. Nominal conditions were used as a reference to the variability evaluation.

Table I – 7nm FinFET device parameters [20]

Parameter		7nm
Nominal Supply Voltage		0.7 V
Gate Length (L_G)		21nm
Fin Width (W_{FIN})		6.5nm
Fin Height (H_{FIN})		32nm
Oxide Thickness (Tox)		2.1nm
Channel Doping		$1x10^{22}$ m^{-3}
Source/Drain Doping		$2x10^{26}$ m^{-3}
Work Function	NFET	4.3720
	PFET	4.8108

After setting the parasitic extraction configurations with the options desired, the parasitic wire capacitances and resistances from the layout were extracted. A new netlist was generated where each net contains one subckt with the RC tree structure modeling the net and the connections between the parasitic networks.

Process variability was taken through two thousand Monte Carlo simulations carried out in HSPICE with the WFF parameter modelled as a Gaussian function with a 3σ deviation of 5% from nominal values [12][21]. The mean (μ), the standard deviation (σ) and the normalized standard deviation (σ/μ) were analyzed for all complex gates.

The choice of the transistor topology with less impact of variability effects is given observing the deviation, i.e., the σ/μ relation. An arrangement is pointed as the best choice to mitigate the variability impact if it has the lowest value for the σ/μ relation. All complex gates drive a FO4 inverter and this has two inverters used as the load connected to each input.

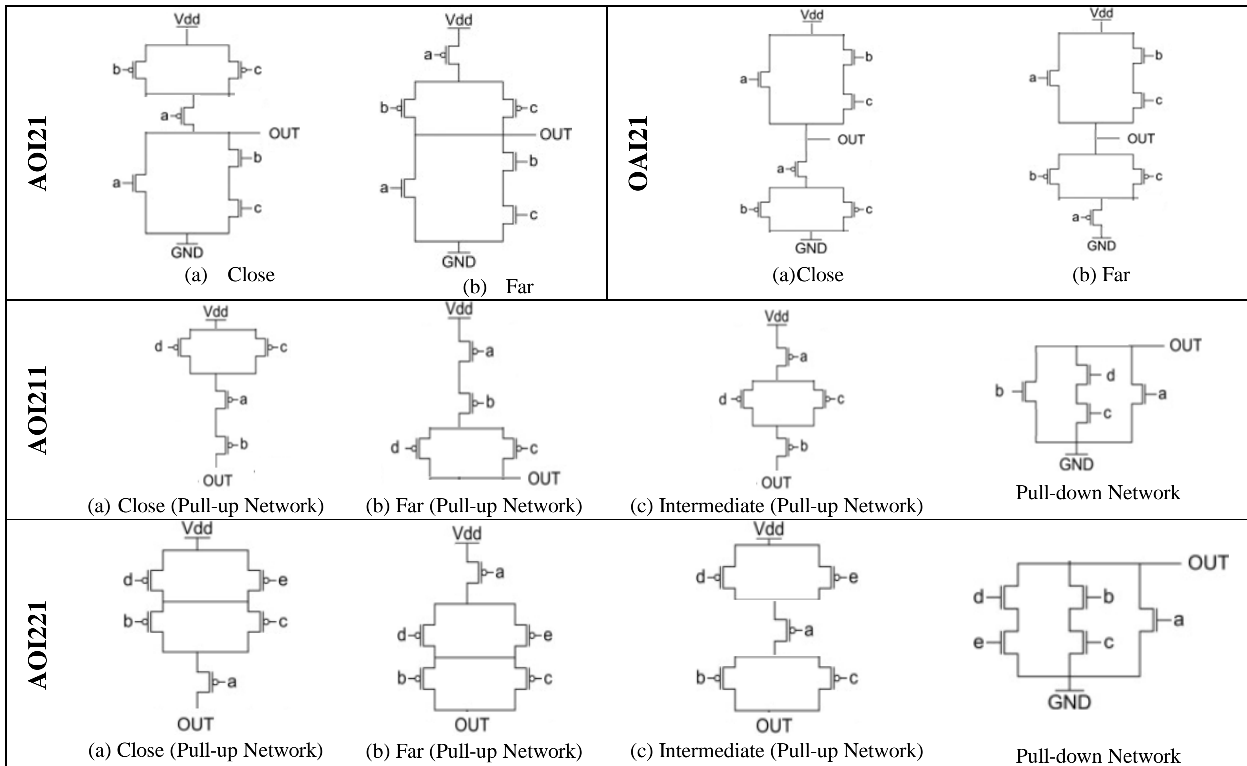

Fig. 2 Complex gates logically equivalent with series transistor (a) close, (b) far and an (c) intermediate place to the output node

3. Layout Description based on ASAP7

All the complex gates were designed using the ASAP7 Process Design Kit (PDK) that considers a not yet available technology node for academic use. This PDK was chosen because admits realistic design conjectures regarding the lithography step and the current technology competencies [20]. Table II shows some essential layers and the design rules considered in this PDK.

Table II – Some key layers, widths and pitches [20]

Layer	Lithography	Width/ drawn (nm)	Pitch (nm)
Fin	SAQP	6.5/7	27
Active	EUV	54/16	108
Gate	SADP	21/20	54
SDT/LISD	EUV	25/24	54
LIG	EUV	16/16	54
VIA0-VIA3	EUV	18/18	25
M1-M3	EUV	18/18	36
VIA4-VIA5	LELE	24/24	34
M4-M5	SADP	24/24	48

FinFET technologies have a width quantization characteristic [21]. With a 27 nm fin pitch, high-density layout design is achieved with three fins for each PFET and NFET devices [22]. Fig. 3 shows the layout view of the AOI21 complex gate with the serial transistor close to the output. The difference of the far topology is the serial transistor connected to supply voltage. The cell height is set to 7.5 tracks of metal 2 (M2) that correspond to 0.27 µm. The supply/ground rails have a tall approximately equal to 1.22 tracks of M2. The total area of complex cells with three, four and five inputs is 84.78 nm^2, 101.74 nm^2 and 118.67 nm^2, respectively.

This PDK has the manufacturing process composed by front end of line (FEOL), middle of line (MOL) and back end of line (BEOL) as shown the Fig. 3. The layouts were developed with a continuous diffusion layer and every gate must have at least one other gate surrounding the horizontal axis. The fin layer polygons should have an equal length along the X-axis. The Source-Drain Trench (SDT) connects the active area to the LISD layer. The Local-Interconnect Gate (LIG) is used to connect the gate terminal and the Local-Interconnect Source-Drain (LISD) connects the source and drain of the transistors. The function of V0 is to join the LIG and LISD to the BEOL layers. The metal 1 (M1) is used for intra-cell routing and short connections. The power rails are made using M1 and LIG that are connecting at V0 in regular intervals. For obtain success in the LVS verification step is necessary to add a TAP cell in the design of each cell.

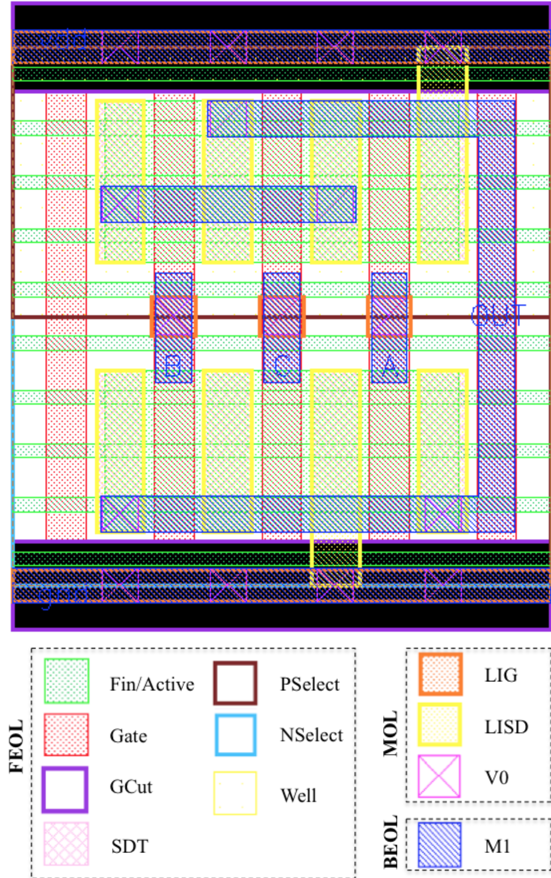

Fig. 3 Layout of AOI21 Complex Gate in 7nm FinFET Technology (ASAP7) with serial transistor close to the output

4. Investigation of Arrangement Effects

In this work, the analysis is divided into three main parts. First, a comparison of electrical characteristics of each complex gate with different networks considering the typical behavior and under WFF variations is made. The second part verifies the more suitable topology to gate variability mitigation as well as the improvements and penalties on delays and power consumption.

Fig. 4 and Fig. 5 show the difference between nominal values and the mean of the results obtained by Monte Carlo simulations for power consumption and considering the worst-case of the propagation delay, respectively. The worst-case delay is the higher propagation time from all timing arches of each function. The red bars indicate the increase caused in the electrical characteristics due to process variability. The power consumption suffers around 4-5.5% of deviation while the effects on the worst case of the propagation delay were of up to 7.5% from the nominal values. The arrangements with transistors in

series far to the output node result in more power consumption and longer delays in the majority of cases. This outcome is very similar to what happens in the analysis of timing and aging as related in the literature [18].

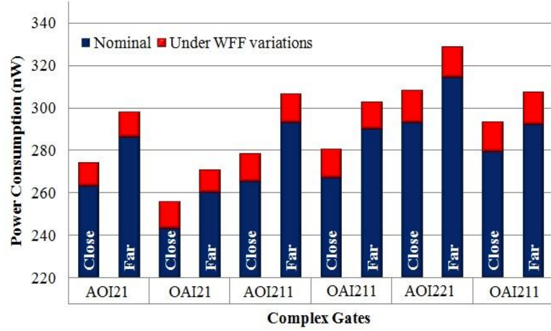

Fig. 4 Difference between power consumption nominal values and under WFF variations

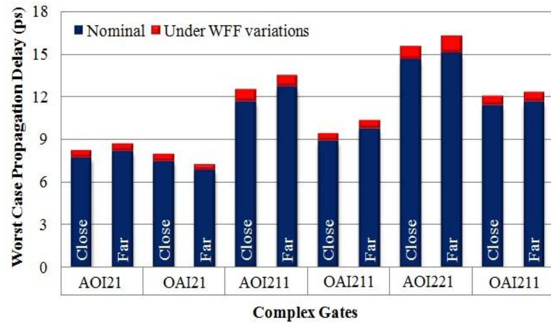

Fig. 5 Difference between the worst-case delay considering nominal values and under WFF variations

Table III summarizes the mean (μ) and the normalized standard deviation (σ/μ) of the worst-case delay and the power consumption for all complex gates analyzed. Also, to show the process variability impact dimension on energy and the energy consumed per switching event, results are evaluated considering the Power-Delay-Product (PDP), where the PDP is calculated for each Monte Carlo simulation. The metrics of intermediate topology are between the close and far values, and then, they were omitted.

All results in Table III enforce the high sensibility to process variability of these cells on 7-nm technology, inserting wide deviations on power and delay, and consequently on PDP. When the power deviation is analysed, all complex gates found as the best cases the options where transistors in series are placed as far as possible from the output node ((b) alternatives presented in Fig. 1). Moreover, the OAIs complex gates are around 7-9.5% more sensible to WFF variations than the AOIs. On the other hand, the propagation time is most impacted by more than 30% of deviation independently of the function or transistor topology. The OAI21, AOI211 and AOI221 gates have attenuation in the effects of variability when the transistors in series are closer to the output node.

If considering the only the degradation on delay, the choice of the far topology is disadvantageous for the OAI21, AOI211 and AOI221. This choice increases in the delay mean value of about 53.2% compared to the expected nominal behavior. In this casethe far topology brings few advantages with a better trade-off. Adopting the close topology in these cells, it is possible to attenuate the effects of process variability until 2.3% besides improving the performance of OAI21 in 14.5%.

Otherwise, for the OAI211 cell, the far topology is promising, presenting a variability robustness gain of 4.9% on average delay compared to close topology with a decrease of 14.7% in delay mean value with this topology. The far topology also becomes the OAI221 6.2% more robust to variability effects. However, in comparison to close topology, this cell presents an increase of 8.7% in the delay mean values. Although with some penalties, the far topology is a good choice to improve the variability tolerance of this cell.

However, the adoption of the far topology increases in the power robustness variability for all complex gates and this effect is reflected on the PDP, as shown Fig. 6. For the majority of investigated complex gates, the far topology remains the best choice.

Table III - Mean and standard deviation of the worst-case delay, power consumption and PDP

Metrics		AOI21		OAI21		AOI211		OAI211		AOI221		OAI221	
		Close	Far	Close	Far	Close	Far	Close	Far	Close	Far	Close	Far
Delay	μ (ps)	4.2	6.4	4.4	6.4	9.3	10.0	9.4	8.0	11.6	12.0	9.9	10.7
	σ/μ (%)	34.3	33.8	32.7	33.4	33.6	34.3	31.6	35.0	35.0	35.6	34.4	32.2
Power	μ (nW)	274.2	297.8	255.6	270.8	278.5	306.4	302.8	308.0	308.0	328.5	393.4	307.5
	σ/μ (%)	24.0	22.1	26.0	24.2	27.8	25.4	29.7	27.3	28.9	27.3	31.2	29.8
PDP	μ (aJ)	2.3	2.6	2.1	2.2	3.4	4.0	3.0	3.2	4.7	5.2	3.9	4.1
	σ/μ (%)	27.0	26.0	26.7	27.8	29.7	28.1	30.5	31.4	30.3	28.2	31.8	31.4

All the AOI complex gates achieve a decrease in the process variability effects using the far topology. For the AOI221, the improvement in relation to the close topology reaches to 6.9%.

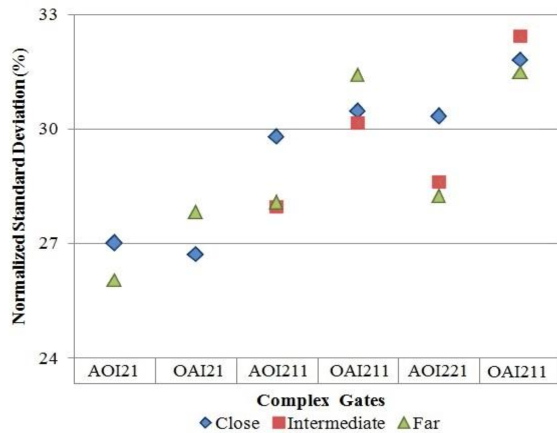

Fig. 6 PDP Normalized Standard Deviation considering WFF variations

This benefit of far topology is due to the high improvement on power robustness compared to the close topology. Fig. 7 illustrates the power evaluation and highlights the main benefits and penalties in term of power of using the far topology instead of the close topologye. The complex gates with three and four inputs present improvements that can reach until 7.6% and 8.6%, respectively. However, a penalty in the power consumption mean value is observed. The AOI211 and the OAI211 gates consume around 10% and 8% more power compared to nominal values, respectively. In general, the AOIs present a little more gain in power robustness variability, but they have a higher increase in the power consumption compared to the OAIs complex gates.

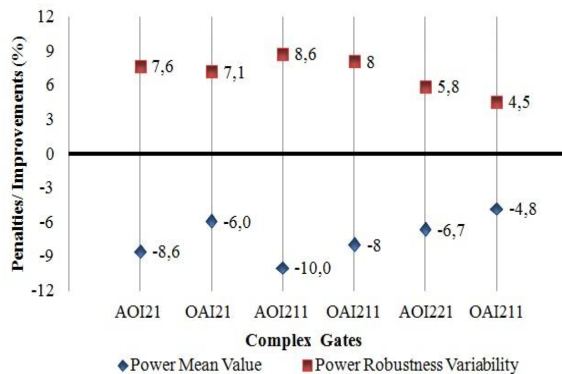

Fig. 7 Gains and penalties related to power in adopting the far topology

6. Conclusions

This work presented an evaluation of the influence of process variability on a set of complex cells designed in 7nm FinFET ASAP technology. The objective was verified what is the best arrangement to mitigate the effects of process variability. The improvements and penalties also are analysed. For ensure the improvement in the power robustness variability, the best alternative is adopted the far topology in the designs. On the other hand, the choice of the far topology to increase the delay robustness variability is only advantageous for the OAI211 and OAI221 complex gates. For the others complex cells analysed, the close arrangement is the better alternative to mitigate the process variability. The improvements in variability caused by the power are reflected on the PDP. Then, far topology seems to be the best choice to mitigate the process variability effects.

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