Towards high density STT-MRAM at sub-20nm nodes

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STT-MRAM are attracting an increasing interest from microelectronics industry. They are about to enter in volume production with the first goal of replacing embedded Flash memory. To go towards high density STT-MRAM at sub-20nm nodes, two major issues have to be solved. One is the nanopatterning of the magnetic tunnel junctions at 1x feature size (F) and narrow pitch (pitch<2F). The other is to increase the thermal stability of the storage magnetization at sub-20nm nodes. Here are proposed innovative approaches to solve these two difficulties.

I. NOVEL APPROACH FOR THE NANOPATTERNING OF MAGNETIC TUNNEL JUNCTIONS AT NARROW PITCH

Spin-Transfer-Torque Magnetic Random Access Memory (STT-MRAM) based on out-of-plane magnetized MTJ (pMTJ) is one of the most promising emerging non-volatile memory technologies. Indeed, it combines a unique set of assets: quasi infinite write endurance, high speed, low power consumption and scalability. Embedded STT-MRAM are about to replace e-FLASH memory. For this type of applications not requiring very high memory density, the preferred etching technique is still ion beam etching (IBE). However this technique is not appropriate for high density memory due to shadowing effects. This effect worsens as the memory pitch shrinks below typically 5F resulting in a poor control of the critical dimension at very dense pitch [1]. Reactive ion etching (RIE) was also tried for MTJs patterning with various gas but was found to be very complex due to the heterogeneous nature of the MTJ stacks and to cause corrosion and delamination of the magnetic materials [2]. Therefore, to be able to use STT-MRAM as a dense working memory, a new method for nanopatterning MTJ elements at small feature size (F<20nm) and narrow pitch (pitch~2F) is still required. In our novel approach, the MTJ stack is directly deposited on pre-patterned conducting pillars consisting of a non-magnetic material for which the patterning process is already well mastered (e.g Ta pillars prepared by RIE or Cu or W vias prepared by damascene process). Thus, the MTJ stack is naturally patterned while being deposited, not requiring any post-deposition etching. Some magnetic material is also deposited in the spaces between pillars. It can be left there without causing any problem. Fig. 1(a) illustrates the principle of this nanopatterning process. The prepatterned non-magnetic metallic pillars are etched with undercut by a combination of anisotropic and isotropic RIE. The undercuts prevent shortcuts between the MTJ material deposited in the trenches and the feet of the pillars.

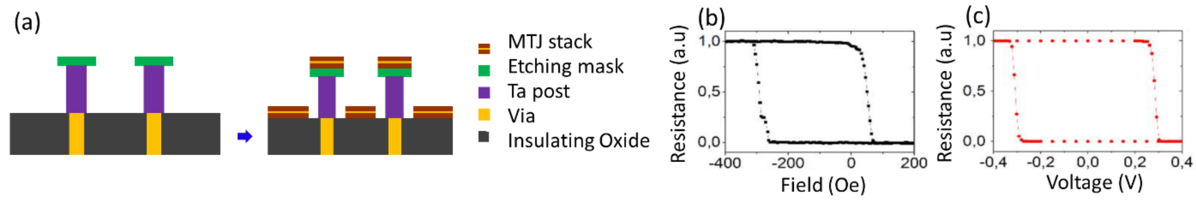

Fig. 1 (a) Illustration of the principle of the nanopatterning of magnetic tunnel junctions at sub-20nm feature size (F) and narrow pitch by depositing the MTJ stack on prepatterned pillars. (b), (c) Room temperature magnetoresistance loop of perpendicular MTJ stack deposited on pre-patterned Ta/Pt pillars versus perpendicular magnetic field (b) and voltage (c).

In this study, the prepatterned pillars consisted of Ta posts capped with a Pt etching mask. Conventional out-of-plane magnetized magnetic tunnel junction stacks were then deposited on these prepatterned arrays of pillars. Subsequently, top contacts were made on top of these junctions to measure their magnetoresistance properties and STT-switching characteristics. Fig.1 (b) and (c) illustrate typical R(H) loops and STT-switching experiments performed on such nanopatterned MTJs [3]. STT switching is observed at write voltage of the order of 0.3V for 100ns write pulse which is comparable to typical values observed in MTJs patterned by RIE.

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II. PERPENDICULAR SHAPE ANISOTROPY STT-MRAM (PSA-STT-MRAM)

In STT-MRAM, a key parameter is the thermal stability factor Δ_T which determines the bit error rate in standby (i.e. the memory retention) and during read. In macrospin approximation, Δ_T is given by:

$$\Delta_T = \frac{E_B}{k_B\,T} = \frac{A}{k_B\,T}\left[\frac{1}{2}\mu_0 M_S^2 t\,(N_{xx} - N_{zz}) + K_S\right] \quad (1)$$

where E_B is the energy required to switch the memory between its two stable states at temperature T, k_B and μ_0 are respectively the Boltzmann constant and the vacuum magnetic permeability. M_S is the saturation magnetization, N_{xx} and N_{zz} are respectively the in-plane and out-of plane demagnetizing factors where z refers to the out-of-plane direction, $A=\pi(D/2)^2$ is the storage layer area with D its diameter, t its thickness, K_S is the interfacial anisotropy at the MgO/FeCoB interface. For standard FeCoB/MgO/FeCoB p-MTJs, $N_{xx} - N_{zz} = -1$ as the thickness (1.4 nm) is much lower than the diameter (> 20 nm) leading to a negative (i.e. in-plane) demagnetizing anisotropy. On the contrary, the strong positive interfacial anisotropy (K_S^{FeCoB}~1.4 mJ/m2 for Fe rich alloys) pulls the magnetization out-of-plane. To fulfill industrial needs, Δ_T should be typically in the range 60 to 100 at 300K [4] depending on the memory capacity and allowed bit error rate. Because Δ_T scales quadratically with D for sub-20nm diameter (macrospin model)[5], Δ_{300} inevitably drops below 60, thus limiting the downsize scalability of p-STT-MRAM. To increase Δ_T at sub-20nm feature size, it is proposed to dramatically increase the thickness of the storage layer to values comparable to its diameter so that its shape anisotropy becomes positive (i.e. out-of plane) as the interfacial anisotropy. Fig.2 (a) shows the evolution of Δ_T (color scale) versus storage layer diameter and thickness. This diagram shows that Δ_T above 60 can be maintained for MTJs down to 4nm diameter provided their storage layer thickness is increased up to ~30nm.

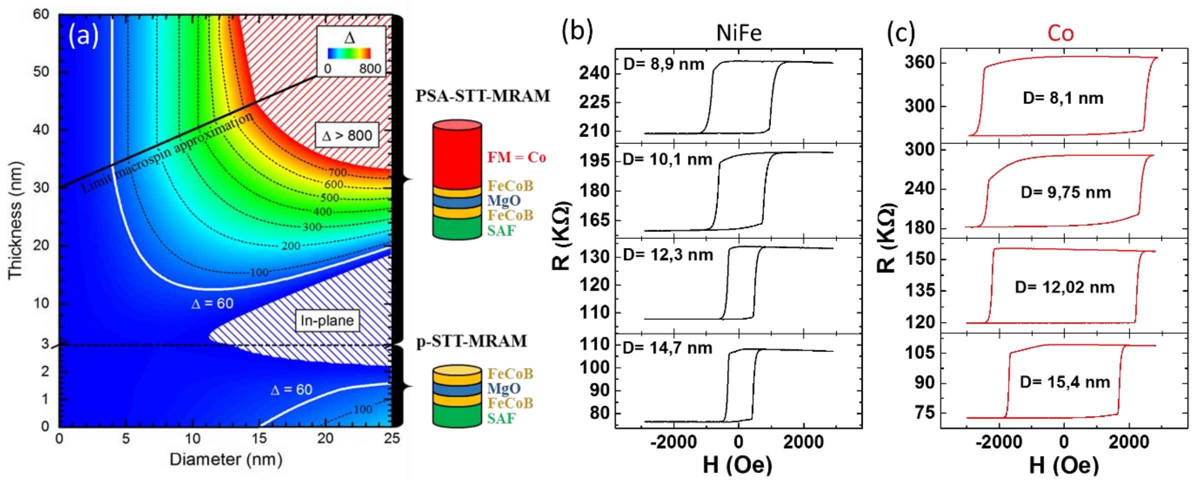

Fig. 2 (a) Stability diagram of a cylindrical storage layer made of FeCoB(1.4 nm)/Co(t-1.4 nm) versus its total thickness (t) and diameter (D), at room temperature (300 K). $M_S^{FeCoB} = 1.0\ 10^6$ A/m and $K_S^{FeCoB} = 1.4$ mJ/m^2, $M_S^{Co} = 1.446\ 10^6$ A/m and $K_u^{Co} = 0$ J/m^3. The iso-Δ line, $\Delta_{300} = 60$, is highlighted in bold white, other iso-Δ lines are shown in dashed black lines. (b), (c) Evolution of the resistance R as a function of a perpendicular field for MTJ of various diameters D in the cases of a 60 nm thick storage layer of NiFe (b) and Co (c).

This concept of Perpendicular Shape Anisotropy STT-MRAM (PSA-STT-MRAM) was demonstrated by patterning narrow MTJ pillars with thick storage layer. NiFe and Co-based storage layers were investigated. The magnetic and transport properties of these MTJs were measured electrically as illustrated in Fig.2 (b) and (c) with field applied out-of-plane. Clearly, strong perpendicular magnetic anisotropy was observed at diameter down to 8nm. Δ_T could be as high as 200 in some of these 8nm diameter junctions demonstrating that very high thermal stability can be achieved in these PSA-STT-MRAM. Of course, the cell aspect ratio (t/D) must be adjusted to keep Δ_T in the range 60-100 allowing to get switching by STT.

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