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Abstract

Synchronous switching circuit is viewed as an effective solution of enhancing the generator's performance and providing better adaptability for load variations. A critical issue for these synchronous switching circuits is the self-powered realization. In contrast with other methods, the electronic breaker possesses the advantage of simplicity and reliability. However, beside the energy consumption of the electronic breakers, the parasitic capacitance decreases the available piezoelectric voltage. In this technical note, a new compact design of the self-powered switching circuit using electronic breaker is proposed. The envelope diodes are excluded and only a single envelope capacitor is used. The parasitic capacitance is reduced to half with boosted performance while the components are reduced with cost saved.

Keywords: Energy harvesting Piezoelectric generator Synchronous switching circuit Electronic breaker

1- Introduction

With the growth of electronic portable devices, autonomous energy systems and autonomous network systems, devices which can generate electrical power by exploiting ambient vibration energy have been developed in recent years. In addition to the improvement of the power density [1] or the bandwidth [2-5] of the generator through the mechanical structure, the interface circuit plays a critical role in the harvester's performance, especially for the piezoelectric generator with high output impedance. Dedicated circuit design is required to extract more power from the generator and improve the impedance match. In comparison with the usual standard circuit of a rectifier and a filter capacitor [6], the synchronous switching circuit is viewed as an effective solution of enhancing the generator's performance and providing better adaptability for load variations. The SSHI (Synchronous Switching Harvesting on Inductor) [7] is firstly introduced to utilize the voltage inversion process to avoid the energy return

phenomena in the standard circuit. A diversity of improved circuits based on SSHI are then proposed, such as SSHI-MR [8], DSSH [9], ESSH [10] and so on. In addition, the SECE (Synchronous Electric Charge Extraction) [11] is raised to solve the impedance matching problem. Furthermore, the OSECE (Optimized SECE) is promoted to improve the performance of SECE while keeping low load dependence [12] while the tuneable SECE is developed to extend the bandwidth of generator from the circuit part [13]. However, a critical issue for these synchronous switching circuits is the self-powered realization.

Various methods including mechanical switches [14-17], velocity control [18], integrated control circuits [19-20], electronic breakers [21-25] etc. have been developed. Among them, the mechanical switches approach has the fewest electronic components with the contacting electrodes [14-16] or the reed switch [17] instead of the electronic switches. However, it is not so adaptive to the displacement variations in many cases. The velocity control utilizes an additional sensing unit to detect the displacement extreme and control the switches precisely with analogue comparators [18]. Additional fabrication requirements are usually required for the piezoelectric generator. The integrated control circuits [19-20] have the strongest function but also the most components and the most complicated design. In contrast, the electronic breaker possesses the advantage of simplicity and reliability. Generally, a part of the extracted energy from the generator is consumed by the electronic breaker and the switching phase lag is introduced by the envelope detector [21-23] and the charging of the switches [25]. Moreover, the parasitic capacitance in the electronic breaker, mainly referred to the envelope detector capacitance, imposes an equivalent effect of connecting a parallel capacitor of the total parasitic capacitance to the generator and induces the charge neutralization after the voltage inversion, thus decreasing the available piezoelectric voltage, especially for the generators with small intrinsic capacitance. Consequently, the generator's performance degenerates obviously compared with the ideal case.

Reducing the components of the self-powered circuit components while keeping the function could save the energy consumption and would be helpful for saving the costs. Recently, an alternative SSHI self-powered design using electronic breakers has been proposed with fewer diodes used and better performance [26]. However, two capacitors are still used in the circuit for peak detectors. In comparison with the diodes, the capacitance plays a more critical role in the performance by introducing the switching phase lag and decreasing the piezoelectric voltage. In this technical note, a CSPOSECE (Compact Self-Powered OSECE) design is propose by multiplexing the comparator instead of the diode in the regular SP-OSECE circuit [23]. More important, only a single capacitor is used for both positive and negative peak detection. The parasitic capacitance of the electronic breaker is thus reduced to half so that the performance is improved.

2- Proposed CSP-OSECE circuit

2.1- Circuit principle

Fig. 1 (a) shows the SP-OSECE circuit with both NPN and PNP power transistors as the switches, which are different from previous works with both NMOS switches [23]. The circuit mainly consists of two electronic breakers, two transistor switches, a three-winding fly-back transformer (turn ratio L_1:L_2:L_3 = 1:1:m) and the load unit. The positive and negative breakers are connected to the two windings of the transformer's primary side respectively while the secondary side is connected to the load unit. Each electronic breaker is composed of an envelope detector and a comparator. In the circuit, the piezo element is represented by an equivalent current source i_{eq} and an intrinsic capacitance C_0. When the piezoelectric element is subjected to a sinusoidal excitation with the displacement u=$u_M sin\omega t$, we have

$$i_{eq} = \alpha \dot{u} = \alpha \omega u_M \cos \omega t \tag{1}$$

in which α is the piezoelectric force factor, ω is the excitation frequency and u_M is the displacement amplitude.

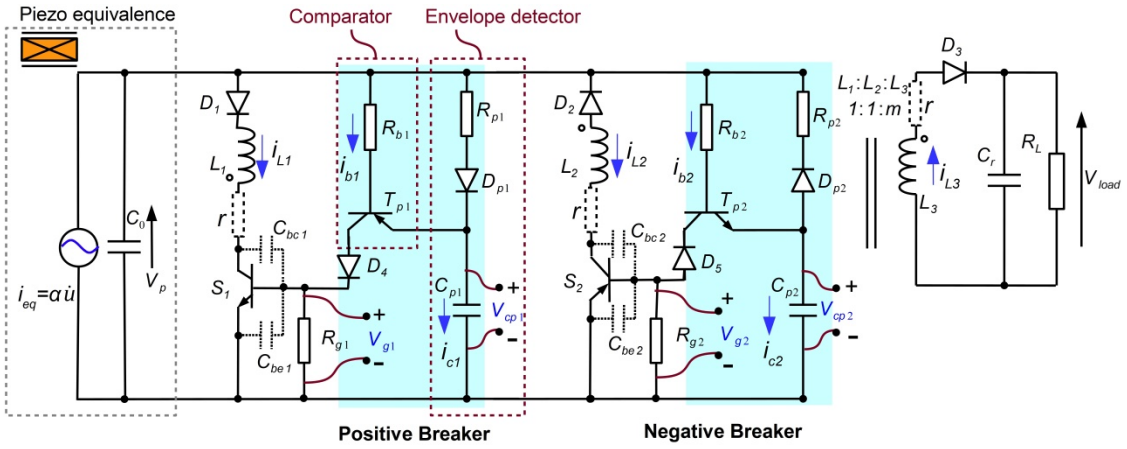

Fig. 1. Self-powered realizations of the OSECE circuit: (a) SP-OSECE; (b) CSP-OSECE.

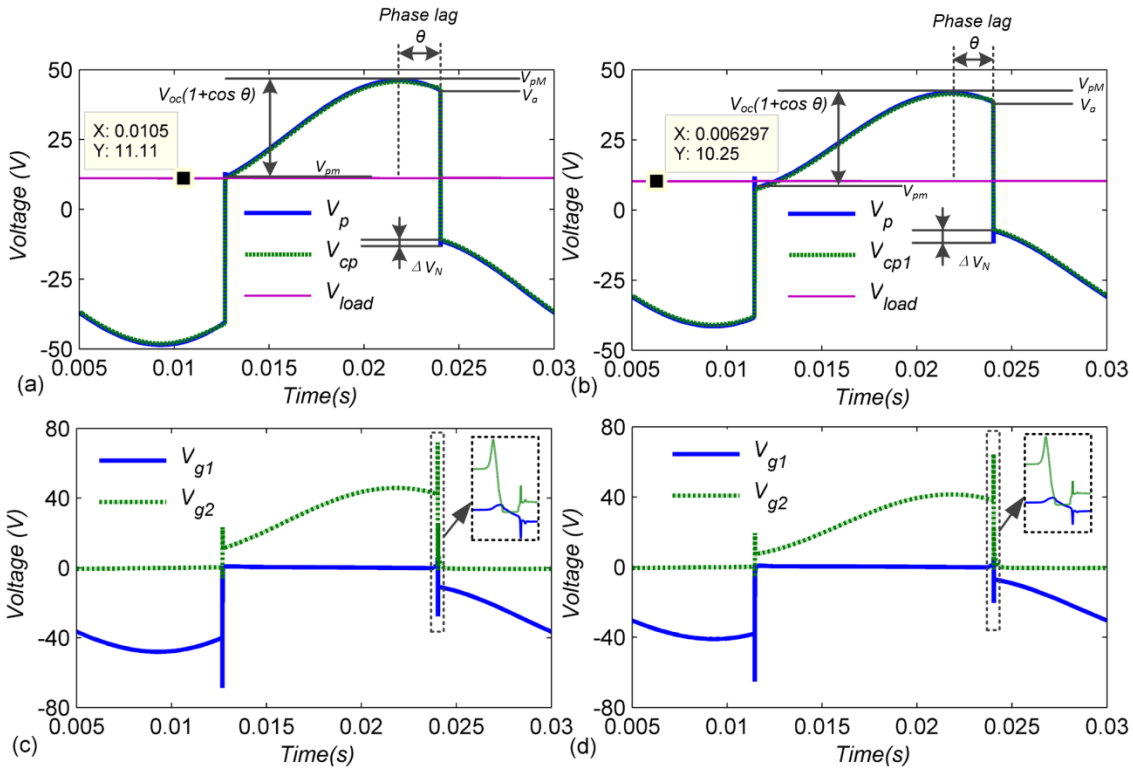

Fig. 2. Simulated Waveforms of the CSP-OSECE and SP-OSECE circuits: (a) and (c) for CSP-OSECE, (b) and (d) for SP-OSCE.

The operation principle is simply introduced here for easy readability and more details can be found in [23, 25]. In the positive half-period, C_0 is charged by the current source i_{eq} and the piezoelectric voltage V_p increases until the peak V_{pM}. With this peak value reserved on the envelope capacitance C_{p1} in the form of V_{cp1}, V_p begins to decrease due to the reverse charging by i_{eq}. As V_p is lower than V_{cp1} with the difference of V_{be}, leading to the conduction of the comparator T_{p1}, the current from C_{p1} starts to charge the base-emitter parasitic capacitance C_{be1} to turn on the switch S_1. Afterwards, a LC oscillation (L_1 and C_0) begins and the piezoelectric voltage is inverted. As soon as V_p reaches $-V_{load}/m$, the remained energy in the transformer is transferred to the load due to the special mechanism of the fly-back transformer. Subsequently, the negative half-period starts with similar operations. In this regular SP-OSECE circuit of Fig. 1 (a), the positive breaker and the negative breaker are independent to each other with similar yet complementary configurations. Two separate sets of envelope detectors are used, including the diodes (D_{p1} and D_{p2}), the resistors (R_{p1} and R_{p2}) and the capacitors (C_{p1} and C_{p2}).

Fig. 1 (b) presents the proposed CSP-OSECE (Compact SP-OSECE) design. The improvements in comparison with the regular SP-OSECE circuit arise from two aspects: (1) the comparators T_{pi} are multiplexed as the envelope diodes which are indicated by the dashed symbols in Fig. 1 (b); (2) a single envelope capacitor is shared by both positive and negative breakers. In the positive half-period, R_{b2}, the base-emitter PN junction of T_{P2} and C_p work as the positive envelope detector; in the negative half-period,

R_{b1}, the base-emitter PN junction of T_{p1} and C_p work as the negative envelope detector. The circuit operations are similar to the regular SP-OSECE circuit and the simulated voltage waveforms for both circuits are plotted in Fig. 2 with C_p=1.75nF and R_{load}=470kΩ while other components and parameters are listed in Table 1. Notably, the variables are denoted in Fig. 1. Easy to find, the produced switching control signals V_{g1} and V_{g2} are almost the same while the piezoelectric voltage (V_p) waveforms are similar as well.

Replacing the rectifying diode with the PN junction inside the bipolar transistor comparator might require special attention to the interchangeability. By observing the circuit in Fig. 1 and the waveforms in Fig.2, it can be found that the voltage on the envelope capacitor V_{cp} always follows the piezoelectric voltage with a voltage difference of +/-V_D (V_{BE}). It means that the voltage stress on the PN junction is small. Therefore, the only issue is the current rating of the PN junction. Considering that the current from the piezoelectric element to the envelope capacitor is usually small in micro-power energy harvesting cases, few efforts are added when selecting the components for the comparator function. However, it should be noticed that the voltage drop on the PN junction might be higher than the rectifier diode. Normally, the voltage difference is small and negligible but it might bring some performance degeneration by introducing additional phase lag, especially for the low piezoelectric voltage case. Therefore, it is recommended to select the bipolar transistor with small V_{BE} value.

Clearly, the required components in CSP-OSECE circuit are less than the SP-OSECE circuit with the same function. The needs for specific envelope resistors and diodes are excluded. More important, the parasitic capacitance in the circuit is reduced to a single capacitor. It brings additional performance enhancement which will be detailed in next section.

However, it has to be pointed out that the proposed CSP-OSECE circuit is only applicable to the case of complementary branches with N type switch for positive breaker and P type switch for negative breaker. In addition, the bipolar transistors have to be used as the comparators due to the multipurpose use. When the MOSFET transistor or the nano-power integrated comparator such as LT1540 is used [27], the idea of multipurpose use in CSP-OSECE circuit is not suitable.

2.2- Performance analysis

For the OSECE approach, the harvested power after stabilization can be expressed as

$$P = \frac{V_{load}^2}{R_L} = 2f \times \Delta E \approx 2f \times \frac{1}{2}\eta C_0 (V_a^{\,2} - \frac{V_{load}^2}{m^2}) \tag{2}$$

in which f=ω/(2π) is the excitation frequency, ΔE is the transferred energy during each switching operation, η is the energy transfer efficiency related to the circuit quality factor and V_a is the piezoelectric voltage at the instant right before the switching operation. And we have

$$V_a \approx V_{pm} + 2V_{oc}\cos\theta \approx \frac{V_{load}}{m} - \Delta V_N + 2V_{oc}\cos\theta \tag{3}$$

Here, V_{pm} is the local minimum of V_p after the voltage inversion, V_{oc} is the open-circuit voltage magnitude of the piezo element when connecting to the extraction circuit with the switches turn-off and θ is the switching phase lag related to piezoelectric maximum V_{pM}. It is noted that V_{pm} is smaller than V_{load}/m with a difference of about ΔV_N which refers to the voltage retreatment towards zero after the voltage inversion as seen in Fig. 2. This voltage retreat phenomena is due to the charge neutralization of the parasitic capacitance in the circuit, mainly relates to the envelope detector capacitor C_{pi}, as pointed out in [22, 25].

Using eq. (2) and eq. (3), the power can be written in the other form as

$$P = \frac{V_{load}^{\ 2}}{R_L} \approx \frac{m^2\eta f C_0(-\Delta V_N + 2V_{\ oc}\cos\theta)^2}{(\sqrt{m^2 + \eta f C_0 R_L} - \sqrt{\eta f C_0 R_L})^2} \tag{4}$$

With the same switches, load resistor and transformer used for the regular SP-OSECE and the CSP-OSECE, the values of C_0, R_L and m are identical for both circuits. Moreover, when the envelope resistor R_{pi} has the same value of R_{bi} and the voltage drop on the diode D_{pi} in SP-OSECE are close to the drop on T_{pi} in CSP-OSECE, the phase lag θ is inclined to have approximate values as well in both cases since the factors inducing the phase lag are almost the same. It is partly verified by the waveforms in Fig. 2 (a) and (b) that the approximate phase lag values are obtained for both cases. Furthermore, it can be inferred that the values of the efficiency η are expected to be similar with the above conditions since the three circuit branches ((1) L_1, S_1, D_1; (2) L_2, S_2, D_2 and (3) L_3, D_3) related to the voltage inversion process are the same in both circuits. Consequently, the power difference between the regular SP-OSECE and the CSP-OSECE are mainly related to the open-circuit voltage magnitude V_{oc} and the voltage retreatment ΔV_N due to the charge neutralization. Therefore, comparative investigations are further performed on these two factors.

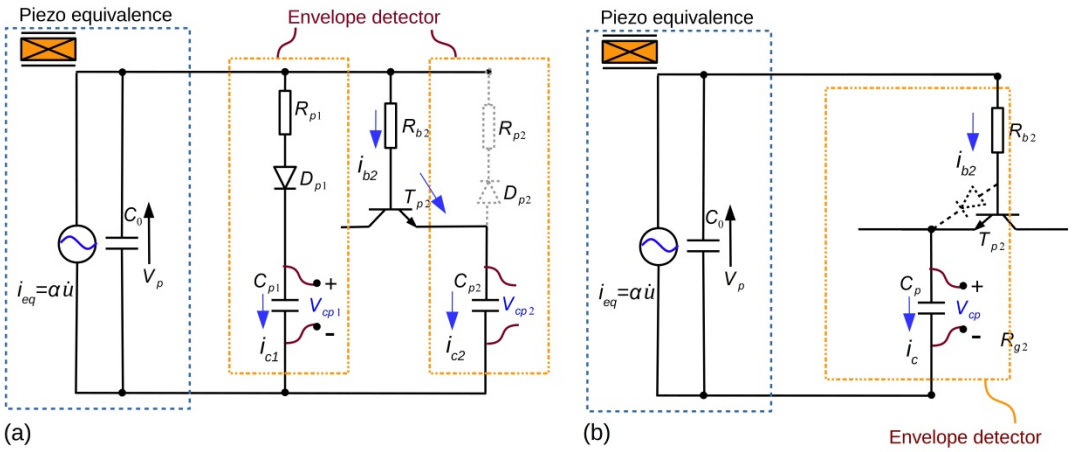

Fig. 3 Equivalent circuit of the two circuits in the charging phase: (a) CSP-OSECE; (b) SP-OSECE.

According to the definition, the open-circuit voltage magnitude V_{oc} can be obtained with the assumption that the switches S_1 and S_2 are turned off. It is similar to the charging phase between two switching operations. By carefully observing the regular SP-OSECE circuit in Fig. 1 (a) and the CSP-OSECE circuit in Fig. 1 (b) in this case, they can be simplified to the reduced circuits in Fig. 3 (a) and (b) respectively. Here, only the positive half-period is considered while the negative half-period can be obtained in the same way. Clearly, beside C_0, the equivalent current source i_{eq} is required to charge C_{p1} through R_{p1}, D_{p1} and C_{p2} through R_{p2}, T_{p2} simultaneously. When $\omega R_{pi}C_{pi}<<1$ and $\omega R_{bi}C_{pi}<<1$ are satisfied for the usual case, the open-circuit voltage magnitude V_{oc} can be written as

$$V_{oc@SP\_OSECE} \approx \frac{\alpha u_M}{C_0 + 2C_p} = \frac{C_0 V_{oc,org}}{C_0 + 2C_p} \tag{5}$$

for the regular SP-OSECE circuit. Here, $C_{p1}=C_{p2}=C_p$ and $V_{oc,org}=\alpha u_M/C_0$ is the original open-circuit voltage of the piezoelectric generator without any circuits. In contrast, i_{eq} only needs to charge a single capacitor C_p beside C_0 in the CSP-OSECE circuit and we have:

$$V_{oc@CSP\_OSECE} \approx \frac{\alpha u_M}{C_0 + C_p} = \frac{C_0 V_{oc,org}}{C_0 + C_p} \tag{6}$$

Easy to find, a higher open-circuit voltage magnitude is obtained for CSP-OSECE in comparison with the regular SP-OSECE and the difference increases with C_p.

The charge neutralization refers to the short phase after the voltage inversion during which the charge on C_0 is redistributed on C_0, C_{p1} and C_{p2} for SP-OSECE or C_0 and C_p for CSP-OSECE until new voltage equilibrium between them. It induces the voltage retreatment towards zero and we have

$$\Delta V_{N@SP-OSECE} \approx \frac{V_{load}}{m} - \frac{C_0 V_{load}/m - q_{r1} - q_{r2}}{C_0 + 2C_p} \tag{7}$$

for SP-OSECE and

$$\Delta V_{N@CSP-OSECE} \approx \frac{V_{load}}{m} - \frac{C_0 V_{load}/m - q_{r0}}{C_0 + C_p} \tag{8}$$

for CSP-OSECE. Here, $q_{r1}\approx C_p V_a \approx C_p(V_{load}/m+2V_{oc}\cos\theta)$ and $q_{r2}\approx C_p(V_{be}+V_D+V_{ce})$ are the remained charge on C_{p1} and C_{p2} to be neutralized respectively in the SP-OSECE circuit in Fig. 1 (a) and $q_{r0}\approx C_p(V_{be}+V_D+V_{ce})$ is the remained charge on C_p to be neutralized in the CSP-OSECE circuit. V_{be}, V_D and V_{ce} represent the base-emitter voltage drop of the switches S_i, the voltage drop on the diodes D_i and the voltage collector-

emitter voltage drop of the comparators T_{pi} respectively. Considering $q_{r2}<<q_{r1}$ and $q_{r0}<<C_0V_{load}/m$, eq. (7) and eq. (8) can be further simplified as:

$$\Delta V_{N@SP-OSECE} \approx \frac{3C_pV_{load}/m + 2C_pV_{oc}\cos\theta}{C_0 + 2C_p} \tag{9}$$

$$\Delta V_{N@CSP-OSECE} \approx \frac{C_pV_{load}/m}{C_0 + C_p} \tag{10}$$

Clearly, the CSP-OSECE has smaller ΔV_N values than the SP-OSECE circuit does and the difference increases with C_p as well.

Combining eq. (5), eq. (6), eq. (9), eq. (10) and using eq. (4), we have the following equation

$$\frac{P_{SP-OSECE}}{P_{CSP-OSECE}} = \frac{(2V_{oc@SP-OSECE}\cos\theta - \Delta V_{N@SP-OSECE})^2}{(2V_{oc@CSP-OSECE}\cos\theta - \Delta V_{N@CSP-OSECE})} \tag{11}$$

in which $P_{SP\text{-}OSECE}$ is the power of the SP-OSECE circuit and $P_{CSP\text{-}OSECE}$ is the power of the CSP-OSECE circuit. Since $V_{oc@SP\text{-}OSECE}<V_{oc@CSP\text{-}OSECE}$ and $\Delta V_{N@SP\text{-}OSECE}>\Delta V_{N@CSP\text{-}OSECE}$ are satisfied, the power performance of CSP-OSECE is always superior to the one of SP-OSECE. Moreover, it can be inferred that the advantages of the CSP-OSECE is especially obvious for large C_p values.

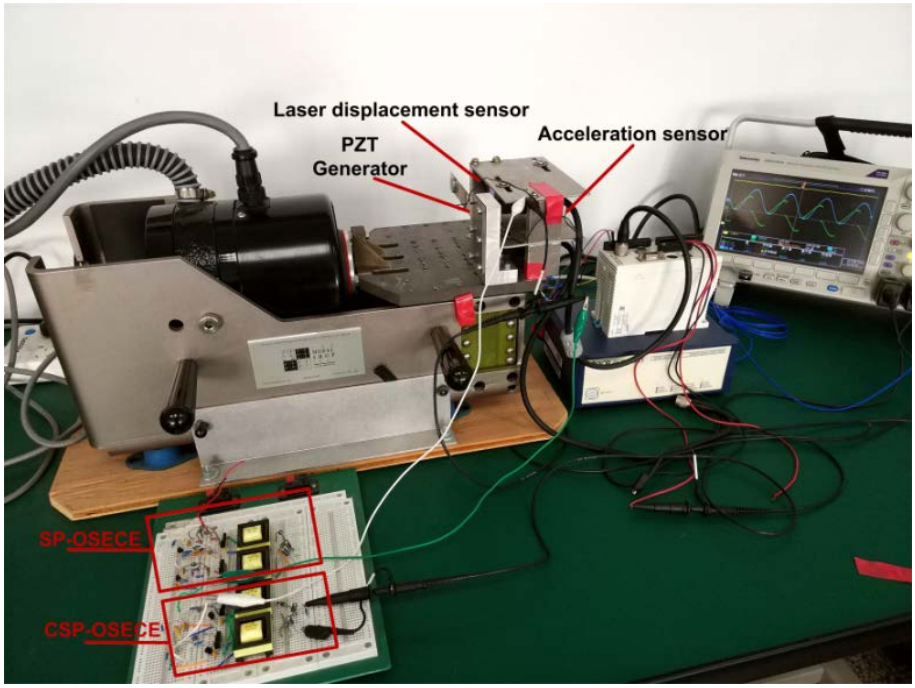

Fig. 4. Experimental platform.

3- Experimental platform

Fig. 4 presents the experimental set-up for the validation of the CSP-OSECE circuit's performance. A piezoelectric cantilever generator is horizontally placed on the shaker (2075E-HT, The Modal Shop©) with a fixture. Two piezoelectric patches (20mm×10mm×0.4mm) are attached to the top and bottom of the steel cantilever (20mm×10mm×0.6mm) respectively. A small mass of 5.7 gram is fixed on the beam tip to pick up the excitation. When the shaker is driven by a signal source (DG1032, Rigol©), an acceleration sensor (M352C68, PCB©) is used to measure the excitation magnitude and a laser displacement sensor (HL-C203BE, SUNX©) is adopted to acquire the vibration responses of the generator. Both CSP-OSECE and SP-OSECE appoaches are elaborated with the same compents listed in table 1 except the different ciruit configurations. The piezoelectric generator is connected to these two circuit alternatively under the same conditions for fair comparison. The load voltage is then sampled by an oscilloscope together with the acceleration and the displacment signals. Parameters identification is firstly performed to the generator with the values given in table 1. For each piezoelectric patch, α and C_0 are estimated to $0.0003 NV^{-1}$ and 14nF respectively. Meanwhile, the open-circuit resonant frequency is found to be around 41Hz. Since the energy transfer efficiency η is related to the circuit working condition and the load voltage [24], it fluctuates in a certain range from around 40%. For simplification, a constant efficiency is assumed for theoretical modeling with this value.

Table 1. Components and Parameters

Definition	Value	Definition	Value
Switches (S_i)	TIP31C	Transistor (T_{pi})	2N5401
Transformer T_1	WE750811290 (m=1)	C_0 (single piezo)	14nF
Diodes(D_i, D_{pi})	BYV28-100	C_0 (two piezo)	28nF
f	41 Hz	R_{bi}	3.3 kΩ
R_{gi}	1 MΩ	R_{pi}	3.3 kΩ
u_M	1.25mm	α (single piezo)	0.0003 N/V

4- Results

In order to focus on the circuit performance, the constant displacement case is firstly studied here as the main part. In this case, the displacement of the beam is controlled to be constant with u_M=1.25mm and the piezoelectric generator is considered as an equivalent current source i_{eq}. As analyzed before, the circuit performance is closely related to the envelope capacitance C_p. Therefore, tests are repeated for both

circuits with C_p varying from 0.5nF to 8.2nF and the load resistor is fixed to 470kΩ. The results are presented in Fig. 5 for two situations of a single piezoelectric patch or two patches.

In both situations, the harvested power firstly increases and then decreases for two circuits. The reason has been explained in [25] that, small C_p values are not able to make the switch in the optimal working condition due the large phase lag and conduction loss while large C_p values decrease the available piezoelectric voltage. Therefore, an optimal C_p exists for the self-powered switching control circuits with electronic breakers as seen in Fig. 5. It is worthy of note that the CSP-OSECE circuit is superior to the SP-OSECE one with better power results in both C_0 cases. When a single piezoelectric patch (C_0=14nF) is used, a maximum power of 0.281mW is obtained for the CSP-OSECE in comparison with the value of 0.204mW for the regular SP-OSECE at the optimal C_p values which are around 1.75nF. A boost of 37.8% is found. For the case of two piezoelectric patches, the maximum power of the CSP-OSECE circuit is 0.697mW which is about 40.8% higher than the SP-OSECE's value of 0.495mW and the optimal C_p values are around 3nF. Due to the CSP-OSECE's improvement of less parasitic capacitance with a single envelope capacitor used, the circuit performance is obviously enhanced. Moreover, it is found that the power enhancement is more obvious as C_p increases. It is in accordance with the analysis in section 2. The theoretical results are also plotted in Fig. 5. Good agreements between experimental and theoretical results are found.

The performance comparison for different load resistance is also performed for both circuits with the estimated optimal C_p used (C_p=1.75nF for C_0=14nF; C_p=3nF for C_0=28nF). Cleary, the CSP-OSECE circuit outperforms the regular SP-OSECE circuit for the whole load range in both C_0 cases. For the case of C_0=14nF, the maximum power of the CSP-OSECE circuit is 0.301mW with R_{load}=670kΩ where the maximum power of the regular SP-OSECE is 0.23mW. For the case of C_0=28nF, the maximum power values of 0.697mW and 0.495mW are obtained with R_{load}=470kΩ. Good agreements are still found between theory and experiment except the discrepancy for large load resistance. It is because the efficiency decreases in these cases due to longer switching duration and larger consumption on switches.

Clearly, better performance is always seen by the CSP-OSECE circuit due to the less parasitic capacitance and charge neutralization for the constant displacement case. It means that more damping effect on the generator will be exerted by the CSP-OSECE circuit as well. However, for the constant force case, the optimal power performance is obtained when the damping effect induced by the harvesting process matches the mechanical damping [12]. When the damping effect induced by the harvesting process is higher than the mechanical damping, the performance decreases. The CSP-OSECE with higher damping effect would be not as good as the SP-OSECE. Generally, the relationship between the damping induced by the harvesting process and the mechanical damping can be roughly indicated by a specific

value of k^2Q_m for different extraction circuits. Here, k^2 means the electromechanical coupling level while Q_m refers to the mechanical quality factor. For the ideal OSECE approach, this value of k^2Q_m is around $\pi/4$ corresponding to the case where the damping induced by the harvesting process is optimal. Since the self-powered OSECE approaches are affected by many parasitic effects, such as the phase lag of the switching, it is difficult to obtain a determined value. However, studies show that higher values are expected in comparison with the ideal one [23]. Therefore, it can be inferred that for the generators with $k^2Q_m<\pi/4$, the CSP-OSECE circuit would achieve better performance than the SP-OSECE one. As a complement, comparative experimental investigations about these two circuits are also performed for the constant acceleration case with a single piezoelectric patch used. With k^2Q_m=0.145, it hints that either CSP-OSECE or SP-OSECE imposes less damping effect than the mechanical damping for the studied cases. Fig. 7 presents the obtained power results of these two circuits. Obvious power improvement is still observed for the CSP-OSECE circuit as expected by the analysis. A power boost of 38% is found around the resonant frequency.

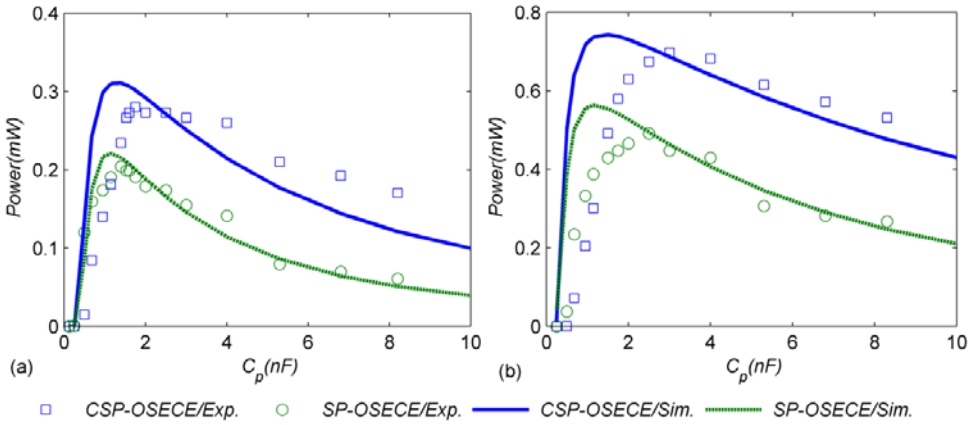

Fig. 5. Power results of both circuits with various C_p and constant R_{load}: (a) a single piezoelectric patch (C_0=14nF); (b) two piezoelectric patches (C_0=28nF).

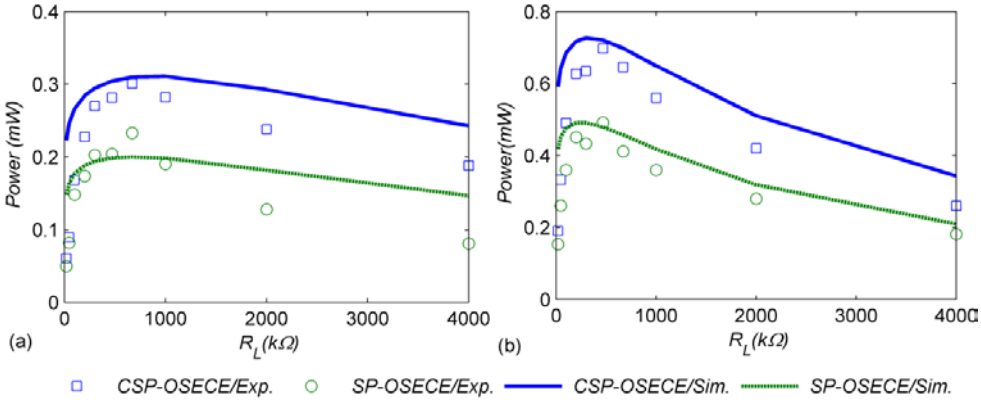

Fig. 6. Power results of both circuits with various R_{load} and constant C_p: (a) a single piezoelectric patch (C_0=14nF); (b) two piezoelectric patches (C_0=28nF).

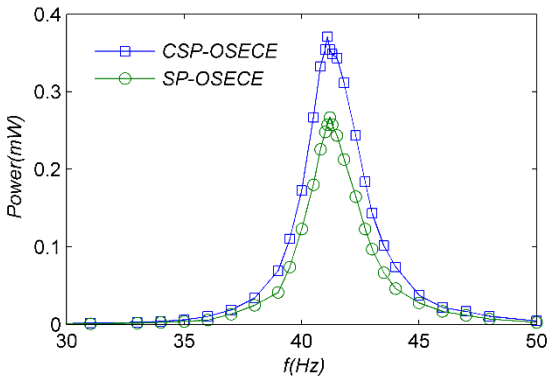

Fig. 7. Experimental power results comparison between CSP-OSECE and SP-OSECE for the constant acceleration of 5m s^{-2} with a single piezoelectric patch used (R_{load}=470kΩ and C_p=1.75nF).

5- Theoretical discussion

In order to obtain a more complete performance comparison between the two circuits, further theoretical investigations are conducted on the two circuits. Two relevant factors are considered: the original open-circuit voltage magnitude $V_{oc,org}$ and the intrinsic capacitance C_0. For simplicity, the load is assumed to be a constant value of 100kΩ in both cases while other parameters are adopted from Table 1.

The generators with C_0 values from 10nF to 50nF are firstly investigated with $V_{oc,org}$=25V. Fig. 8 (a) presents the power results of the CSP-OSECE and the SP-OSECE approaches for different C_0 and C_p while Fig. 8(b) shows the performance improvement of the CSP-OSECE in comparison with the regular SP-OSECE. Clearly, the performance improvement is most obvious for small C_0 and large C_p cases in which C_p has more influence on V_{oc} and ΔV_N, and it is not so significant for large C_0 and small C_p cases in which C_p has weaker influence. Considering that the max power at the optimal C_p value for each C_0 case is more relevant, the enhancement in these points is also plotted in Fig. 9. It is found that the max power enhancement decreases as C_0 increases. The reason is that the ratio C_p/C_0 gets smaller due the slow increase of the optimal C_p as seen in Fig. 8 (a). Consequently, the effects of C_p on the harvested power become less important so that the performance improvement by CSP-OSECE is less significant as well. However, for the case of C_0=50nF, the power boost still reaches 19.4%.

The influence of the original open-circuit voltage magnitude $V_{oc,org}$ is also studied for the generator with C_0=14nF. Considering that the optimal C_p corresponding to a fixed C_0 does not vary much when $V_{oc,org}$ changes, C_p is fixed to 1.75nF in this case. Fig. 10 presents the power increase with $V_{oc,org}$ changing from 15V to 45V. The power improvement slightly decrease to an almost stable value as $V_{oc,org}$ increases. The possible reason is that the parasitic capacitance plays a more critical role in the case of low open-circuit voltage magnitude close to the circuit's start voltage.

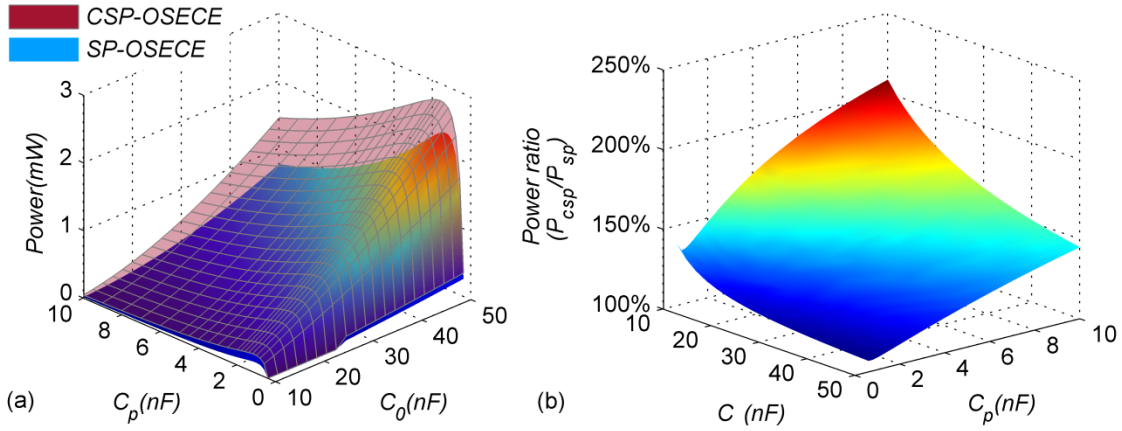

Fig. 8. (a) Power comparison of both circuits for different C_0 and C_p; (b) Power improvement of CSP-OSECE with SP-OSECE as the reference.

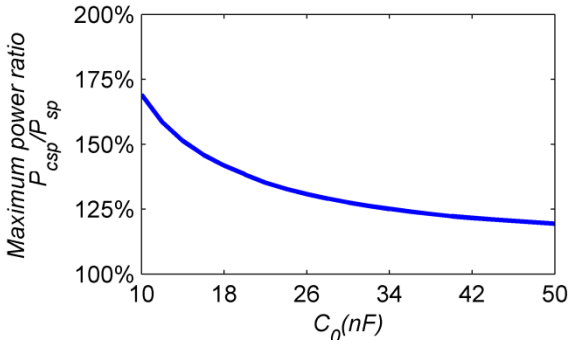

Fig. 9. Max power enhancement of CSP-OSECE versus C_0 at the optimal C_p points with SP-OSECE as reference.

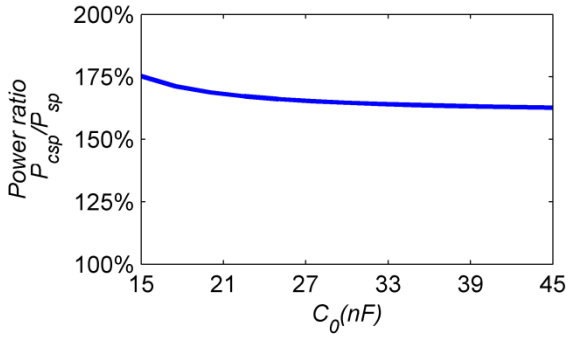

Fig. 10. Power improvement of CSP-OSECE versus $V_{oc,org}$ in comparison with SP-OSECE.

6- Conclusion

In this technical note, the CSP-OSECE circuit is newly proposed. By the multi-purpose use of the comparators, the specific envelope diodes can be saved. More important, a single envelope capacitor is multiplexed for both positive and negative electronic breakers instead of the two envelope capacitors in

the regular SP-OSECE circuit. Therefore, the parasitic capacitance in the self-powered circuit is reduced to half for CSP-OSECE. It brings two benefits: (1) the available open-circuit voltage magnitude is enhanced; (2) the neutralization charge after inversion is reduced. Experimental and theoretical investigations validates that the CSP-OSECE design brings much better performance than the regular SP-OSECE circuit. The advantages are especially obvious for small C_0 or large C_p cases. It can be then concluded that the CSP-OSECE circuit is a better choice with enhanced performance and saved costs. Moreover, the compact design here can be extended to other self-powered circuits with electronic breakers. However, it is reminded that the results are only obtained for the self-powered circuit with complementary branches. In comparison with the self-powered circuit with two identical branches, the CSP-OSECE circuit shows the same advantage of less parasitic capacitance. When the switch influence is assumed the same in both configurations, it can be inferred that better power performance is still expected for CSP-OSECE. As for other self-powered architectures, such as the nano-power comparator LTC1540, the performance comparison result is hard to reach directly and specific investigations are required.

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