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Capacitive Adiabatic Logic based on gap-closing MEMS devices

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***Abstract*—This paper presents the energy analysis of capacitive adiabatic logic (CAL) based on gap-closing MEMS devices. CAL uses variable capacitance components instead of transistor elements to have a new balance between on- and off-state losses. Ultra-low power consumption in CAL requires an energy efficient way for charging and discharging of the variable capacitance. First, we investigate "pure" electrical model of the two-terminal variable-gap capacitor and demonstrate that any hysteresis in CV-characteristic leads to losses of the stored energy. Next, we propose the design of a four-terminal gap-closing MEMS capacitive element to implement variable capacitance element for CAL and build its Verilog-A compact model. Further, we analyze the energy transfer and losses within this device during adiabatic charging and discharging. The received results demonstrate that the variable gap devices with hysteresis have a non-adiabatic losses during operation with four-phase power clock. Finally, the cascadability of the signal throw buffer chain is presented.**

I. Introduction

Despite the nanoscale transistor size, the lowest dissipation per operation is nowadays a few decades higher than the theoretical limit introduced by Landauer (3 zJ at 300 K) [1]. Even though Landauer's theory is still being discussed [2], it is possible to decrease the energy required to implement the logical operation at the hardware level. Adiabatic logic based on FET transistors has been introduced to alleviate this inherent trade-off and reduce the conduction loss [3], [4]. By smoothing transitions between logic states, the charge and discharge of the FET gate capacitance C through the FET channel resistance R of the previous stage is lowered by a factor of $\frac{2RC}{T}$, where T is the ramp duration. The adiabatic part of loss is defined as a part of losses inversely proportional to the ramping time. Decreasing operating frequency, this type of losses can be suppressed up to a Landauer limit for irreversible gate [1].

But there is still a reduction limit factor due to the FET threshold voltage V_{TH}. The non-adiabatic part of the conduction limit remains equal to $\frac{CV_{TH}^2}{2}$. This part of the losses is independent of the ramp duration T and operating frequency. Moreover, adiabatic operation reduces the operation frequency and magnifies the contribution of the FET leakage loss. Even if the energy per operation is slightly reduced, by only a factor of ten, there is still a trade-off between the non-adiabatic conduction and leakage loss. This therefore limits the interest of FET-based adiabatic logic.

To suppress the leakage, electromechanical relays have been used in the literature [5]. As they are based on metal-metal contact instead of a semiconductor junction, the leakage becomes almost negligible [6]. The Shockley law, which basically links the on-state resistance and leakage in the off-region in a semiconductor devices, is not valid in relay devices as it is based on electrical contact between two plates separated by air gap [7]. Moreover, the main bottleneck of the relay-based adiabatic logic is the mechanical reliability of devices [8], [9]. The contactless logic gates, based on NEMS resonators proposed in [10], but this solution has a problem with cascadability [11]. As shown in Fig. 1a, to overcome these limitations, we propose a new logic family called Capacitive-based Adiabatic Logic (CAL) [12]. By substituting relays with variable capacitors, this approach avoids electrical contact. Mechanical contact between the electrodes is then no longer required. For this reason, CAL could be more reliable compared to electromechanical relays. Moreover, the possibility of cascadability is also numerically demonstrated in [12], [13].

The first section of this paper presents a CAL principles. Next, we investigate two-terminal variable capacitor model with arbitrarily chosen smooth CV-characteristic and demonstrate that any hysteresis leads to non-adiabatic energy loss. Further, the design of a four-terminal MEMS capacitive element is proposed and its compact Verilog-A model is built. The energy transfer and losses are analyzed in this particular implementation. Finally, the cascadability for buffer chain based on gap-closing MEMS devices is presented.

II. CAL principles

CMOS-based adiabatic logic circuits basically operate with two types of architecture: Bennett clocking and the quasi-adiabatic pipeline [14]. Power supplies called power clocks (PC's) are quite different for these two architectures. In Bennett clocking PC, the power supply voltage of the current gate increases and decreases only when the inputs are stable.

In a pipeline architecture, a four-phase power supply is used as presented in Fig. 1b. The logical operations are separated in time and performed one after the other. In order to guarantee it, a 90° phase shift between subsequent PC's is added.

In this work, we use the four-phase PC, because Bennett clocking type of architecture is limited for a long logic chain

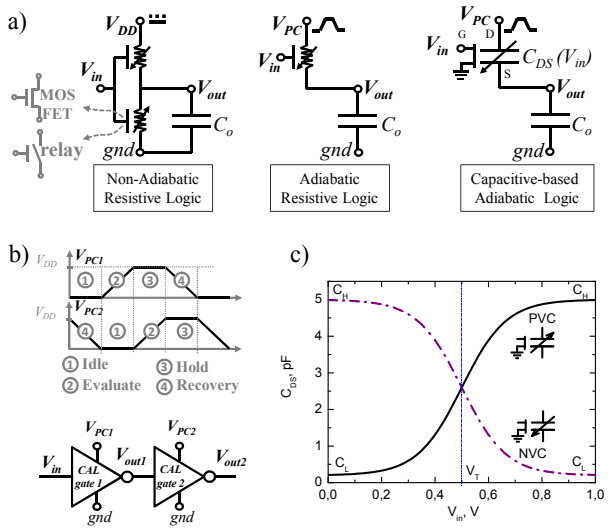

Fig. 1. (a) Schematics depicting conventional resistive logic (left), adiabatic resistive logic (center), and capacitive-based adiabatic logic (right). (b) The four-phase clocking principle. (c) CV-characteristics and symbols for PVC (solid line) and NVC (dash-dot line) capacitors.

and requires N different PC's for N-deep logic chain. The CAL can also be operated in Bennett clocking PC, but it is out the scope of this paper and discussed in [13].

As the PC provides a trapezoidal signal, the resistive elements (transistors) in a voltage divider circuit can be replaced by capacitive ones. In this paper, we keep the FET transistor notations, i.e. the input voltage is applied between the gate (G) and the ground. These two terminals are isolated from the drain (D) and source (S) terminals, which form output with a capacitance C_{DS}. Let us consider the capacitive divider circuit, presented in the left part of the Fig. 1a. In the first assumption, $C_{DS}(V_{in})$ is a variable capacitor which depends only on the input voltage V_{in}. The fixed capacitor C_0 is the equivalent load of the next gate(s) and the interconnections. The output voltage is defined by the capacitance ratio and the PC voltage $V_{PC}(t)$ such that:

$$V_{out}(t) = \frac{C_{DS}(V_{in})}{C_0 + C_{DS}(V_{in})} V_{PC}(t). \quad (1)$$

In this section, the voltages are normalized to the maximum voltage reached by the PC, V_{PCmax}, i.e. voltages range from 0 to 1. Two limiting cases emerge which are:

- when $C_{DS} \gg C_0$, the output voltage value is close to one;
- when $C_{DS} \ll C_0$, the output voltage value is close to zero.

Thus, with an appropriate $C_{DS}(V_{in})$ characteristic, the output voltage can be triggered by V_{in}. A particular electromechanical implementation of this variable capacitor will be discussed later.

There are two possible behaviors of capacitance as a function of the input voltage. The curve $C_{DS}(V_{in})$ can have a positive or negative slope, as presented in Fig. 1c. The former case is called positive variable capacitance (PVC) and the latter, negative variable capacitance (NVC). The low and high-capacitance values are denoted C_L and C_H, respectively. PVC and NVC voltage-controlled capacitors could play the same role in CAL as NMOS and PMOS in FET-based logic, respectively. According to (1), the load capacitance C_0 is a critical parameter in the design of cascadable gates. In order to maximize the difference between logical high and logical low levels, the load capacitance must satisfy the following condition:

$$C_0 = \sqrt{C_L C_H}. \quad (2)$$

III. Two-terminal parallel plate transducer

The key challenge of CAL development is being able to define the scalable hardware necessary to implement the elementary 4-terminal PVC and NVC devices. The capacitor value can be modulated by the variation of relative permittivity, plate surface and gap thickness. In principle, there are a wide range of available actuators to realize this modulation: magnetic, piezoelectric, electrostatic, etc. We selected gap-closing electromechanical actuators because it is proven that the electrostatic MEMS relays can be integrated to VLSI circuits [5] and scaled in sub-1-volt operation region [7]. For further analysis, the analytical model of variable capacitive element is required.

Let us firstly consider a 1D parallel-plate transducer model of a gap-variable capacitor with an initial air-filled gap g_0, equivalent mass m and equivalent spring constant k. The electromechanical transducer model in up-state position is shown in the upper part of Fig. 2a. The up-state capacitance equals:

$$C_{G\_U} = \frac{\epsilon_0 A_G}{g_{eff}}, \quad (3)$$

where ϵ_0 is the permittivity constant of a vacuum, $g_{eff} = g_0 + t_d/\epsilon_d$ is the effective electrostatic gap, A_G is the electrode area of the gate capacitance, and t_d, ϵ_d are the thickness and relative permittivity of the dielectric layer, respectively.

When V_G is applied to the electrodes, the electrostatic attractive force acting on the piston causes its static displacement z. There is a critical displacement equal to one third of the effective gap from which the electrostatic force is no longer balanced by the restoring force and the piston falls down to the bottom electrode as presented in the bottom part of Fig. 2a. The pull-in voltage is given by:

$$V_{PI} = \sqrt{\frac{8}{27} \frac{k g_{eff}^3}{\epsilon_0 A_G}}. \quad (4)$$

The down-state capacitance is defined by the dielectric layer thickness and equals:

$$C_{G\_D} = \frac{\epsilon_0 \epsilon_d A_G}{t_d}. \quad (5)$$

In a down-state position, electrostatic force dominates and the control voltage V_G decreasing below V_{PI} does not lead to the release of the device. It causes hysteresis behavior of the

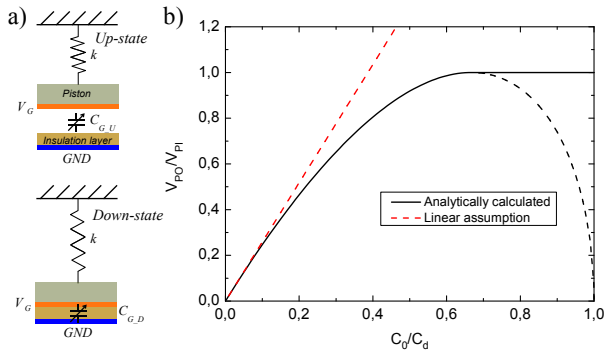

Fig. 2. (a) Electromechanical capacitance in up (top) and down (bottom) states. (b) Normalized pull-out bias voltage according to the capacitance ratio.

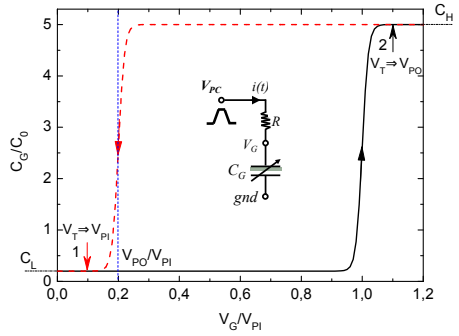

Fig. 3. The hysteresis curve model and test circuit. We used the following parameters: $V_{PCmax} = 1.2V_{PI}$, $a = 50$ V^{-1}, $C_L = 0.2$ pF, $C_H = 5$ pF, $R = 1$ kΩ, $T = 100$ ns.

electromechanical capacitive element. The piston release from the bottom electrode when V_G equals the pull-out voltage, V_{PO} (6) [15]. Adhesion force and an effect on charge injection into the dielectric are neglected here. Both of these effects increase hysteresis.

$$V_{PO} = \sqrt{\frac{2kg_0(t_d/\epsilon_d)^2}{\epsilon_0 A_G}} \tag{6}$$

In this configuration, the low up-state to down-state capacitance ratio $\frac{C_{G\_U}}{C_{G\_D}}$ is achievable. In addition, the pull-out to pull-in voltages ratio can be expressed through the capacitances ratio (7). The results of calculation are shown in Fig. 2b. In small capacitances ratio region voltages ratio is linearly proportional to capacitances ratio. The voltages ratio reaches 1, when capacitances ratio equals to 0.67. This point correspond to the pull-in instability point. For capacitances ratio higher than 0.67, there is no instability point and the voltages ratio stays equal to one, i.e. the device demonstrates a behavior without hysteresis.

$$\frac{V_{PO}}{V_{PI}} = \sqrt{\frac{27}{4}\left(\frac{C_{G\_U}}{C_{G\_D}}\right)^2\left(1-\frac{C_{G\_U}}{C_{G\_D}}\right)} \tag{7}$$

In small capacitances ratio region, there are two loss mechanisms induced by a non-adiabatic motion. According to [15], the impact kinetic energy loss is one of the dominant loss mechanisms in a MEMS relay. This type of loss cannot be suppressed by the increasing ramping time due to the pull-in instability.

The second loss mechanism appears in release point and caused by electromechanical hysteresis. To describe this problem we use arbitrarily chosen smooth CV-characteristic, described by (8) with added hysteresis as shown in Fig. 3.

$$C_{DS}(V_G) = \frac{C_H + C_L}{2} + \frac{C_H - C_L}{2}\tanh\left(a(V_G - V_T)\right) \tag{8}$$

where V_T is the threshold voltage and a is a positive parameter that defines the slope of the $C_{DS}(V_{in})$ curve.

The parameters of the model are presented in Fig. 3. In order to avoid discontinuous in CV-characteristic, the value of V_T is changed by conditional statement in two points. V_T is changed from V_{PI} to V_{PO} in point 2, higher than pull-in voltage, and from V_{PO} to V_{PI} in point 1, lower than pull-out voltage. The value of V_{PO} is varied as independent variable. The test schematic is presented on the inset in Fig. 3.

The energy consumed in the system can be calculated as the difference between energy provided and recovered by the voltage source V_{PC} during one cycle of charging and discharging. The resistive loss is negligible here as $T >> RC_H$ =5 ns. The amount of electrical energy converted to mechanical form caused by capacitance variation can be defined from (9).

$$E_{CONV} = \frac{1}{2}\int_0^{t_0} V_G(t)^2 \frac{dC_G(t)}{dt}dt \tag{9}$$

The same equation (9) can be used to define the amount of energy recovered from mechanical to electrical form. The direction of energy conversion is determined by the time derivative of the capacitance C_G. For developed model the ratio of recovered E_{REC} to converted E_{CONV} energy is equal to (10). The converted and recovered energies are equal only if the system has no hysteresis. Otherwise, the amount of recovered energy is less than amount of converted energy. Therefore, as lower pull-out to pull-in voltage ratio, as lower amount of recovered mechanical energy. The electromechanical hysteresis leads to unavoidable non-adiabatic losses.

$$\frac{E_{REC}}{E_{CONV}} = \left(\frac{V_{PO}}{V_{PI}}\right)^2 \tag{10}$$

In order to distinguish logic states in CAL, the capacitances ratio $\frac{C_{G\_U}}{C_{G\_D}}$ should be small. For this condition the voltages ratio $\frac{V_{PO}}{V_{PI}}$ is linearly proportional to capacitances ratio (7) and also small. Therefore, the total loss equals to almost all stored mechanical energy. This type of energy loss does not depend on ramping time T, and, consequently, non-adiabatic. In the next section we will extend the energy analysis from two-terminal to four-terminal devices which are used in CAL.

IV. Electromechanical Model of a Four-Terminal Variable Capacitor Element

The basic electromechanical device of CAL consists of the two electrically-isolated and mechanically-coupled capacitors.

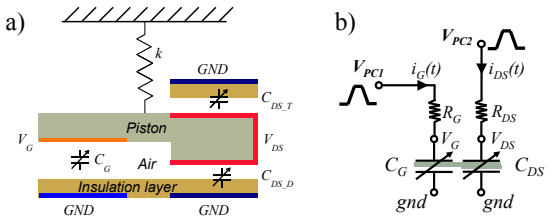

Fig. 4. (a) Four-terminal variable capacitor. (b) Test circuit.

The assumption that C_{DS} depends only on the input voltage is non-accurate, and a bias voltage V_{DC} across the output capacitance also can be used for actuation.

A. Four-terminal parallel plate transducer with stopper

The static pull-in point displacement equals one third of the effective gap. Thus, the uncontrolled collapse can be avoided if we add a stopper with a thickness greater than $2g_{eff}/3$ of the input electrode to stop the mechanical motion before the pull-in. This solution allows us to reduce the impact kinetic energy loss and eliminates the uncontrolled dynamic caused by the voltage V_G. Fig. 4a shows a viable candidate for PVC implementation, where the gap between the electrodes can be modulated by the electrostatic force caused by the gate voltage, V_G, and the drain-source voltage, V_{DS}. The right part (input) is electrically isolated from the left which has the drain and source terminals (output). To avoid output self-actuation, the moving mass displacement z should be insensitive to V_{DS} when V_G = 0 V. In order to guarantee this, we add two couples of symmetrical electrodes, which form two capacitors C_{DS_T} and C_{DS_D}. The C_{DS} capacitance is the sum of the latter:

$$C_{DS}(z) = \frac{\epsilon_0 A_{DS}}{g_0/3 + t_d/\epsilon_d + z} + \frac{\epsilon_0 A_{DS}}{g_0/3 + t_d/\epsilon_d - z}, \quad (11)$$

where A_{DS} is the symmetrical output electrode area of the C_{DS} capacitance and $g_0/3$ is the initial output gap thickness. When the input voltage V_G and, consequently, the displacement z are small, the electrostatic attractive force $F_{elDS}(z)$ in the output is almost balanced:

$$F_{elDS}(z) = 2\epsilon_0 A_{DS} V_{DS}^2 \frac{(g_0/3 + t_d/\epsilon_d)z}{[(g_0/3 + t_d/\epsilon_d)^2 - z^2]^2}. \quad (12)$$

The dynamic behavior of the parallel plate transducer with an air-filled cavity is described by the following differential equation of motion:

$$m\ddot{z} = F_{elG}(z) + F_{elDS}(z) + F_{con}(z) - b\dot{z} - kz, \quad (13)$$

where we assume that the viscous damping coefficient b does not depend on the piston displacement. The limit of piston displacement due to the stopper is modeled by injecting an additional restoring force F_{con}, as in work [16]. The adhesive forces are neglected.

B. Energy conversion and losses

In order to study the dynamic behavior of the 4-terminal electromechanical element, we perform transient simulation of the circuit depicted in Fig. 4b, which mimic an elementary PVC actuated by two four-phase PC's. Only the case of maximal displacement and large capacitance variation is discussed. The equivalent parameters of the model are extracted from a fixed-fixed gold plate: length 103 μm, width 30 μm and thickness 0.5 μm, according to [17]. The residual stresses in the plate equal zero and only the linear component of stiffness is used in the model. The energy components in this system are:

- energy delivered by the first voltage source $E_{S1} = \int_0^{t_0} V_{PC1}(t) i_G(t) dt$;
- energy delivered by the second voltage source $E_{S2} = \int_0^{t_0} V_{PC2}(t) i_{DS}(t) dt$;
- electrical energy stored in C_G: $E_{C_G} = \frac{1}{2} C_G V_G^2$;
- electrical energy stored in C_{DS}: $E_{C_{DS}} = \frac{1}{2} C_{DS} V_{DS}^2$;
- energy dissipated in the resistor R_G $E_{R_G} = R_G \int_0^{t_0} i_G(t)^2 dt$;
- energy dissipated in the resistor R_{DS} $E_{R_{DS}} = R_{DS} \int_0^{t_0} i_{DS}(t)^2 dt$;
- mechanical spring energy $E_M = \frac{1}{2} k z^2$;
- kinetic energy $E_{KIN} = \frac{1}{2} m v^2$;
- energy loss in damping $E_D = b \int_0^{t_0} v(t)^2 dt$;

where V_{PC1}, V_{PC2} are the output voltages of the two PC's, i_G and i_{DS} are the currents through the resistors R_G and R_{DS}, respectively, v is the piston velocity.

For the first simulation and model verification, we selected a four-phase PC's with $T = 5/f = 50$ μs and $V_{PC1max} = V_{PC2max} = 15$ V. The mechanical relaxation time constants of the model equals $Q/(\pi f)$=31.8 μs, so that electrical constant $R_{DS}C_{DSmax} = 32.5$ ps. As the mechanical time constant is significantly greater than the electrical one, the resistive loss is 5 orders of magnitude lower than the mechanical one loss does not presented in Fig. 5. The current peaks in the second graph of Fig. 5 are caused by the movement of the piston. During the charging process of C_G, part of the electrical energy is converted into mechanical energy. It can be observed as difference between energy provided by the first voltage source E_{S1} and energy stored in capacitor E_{C_G}. Most part of this energy stored in mechanical spring energy E_M. Small part of the converted energy, i.e. the kinetic energy E_{IMP} is lost during the impact. The energy saving law is satisfied here, the ΔE graph presents difference between provided energy and the sum of stored energy with work of the damping force. The step in the ΔE graph is caused by the work of the contact force F_{con} which limits the piston motion.

Charging of C_{DS} capacitor does not lead to energy conversion as the capacitance remains constant. When discharging C_G, the piston does not move and the first voltage source recovers only electrical part of energy stored in C_G. Even if V_G = 0 V, the moving mass stays in down-state position. The capacitances C_G and C_{DS} as a function of time are presented in fourth graph of Fig. 5. For selected parameters values, given

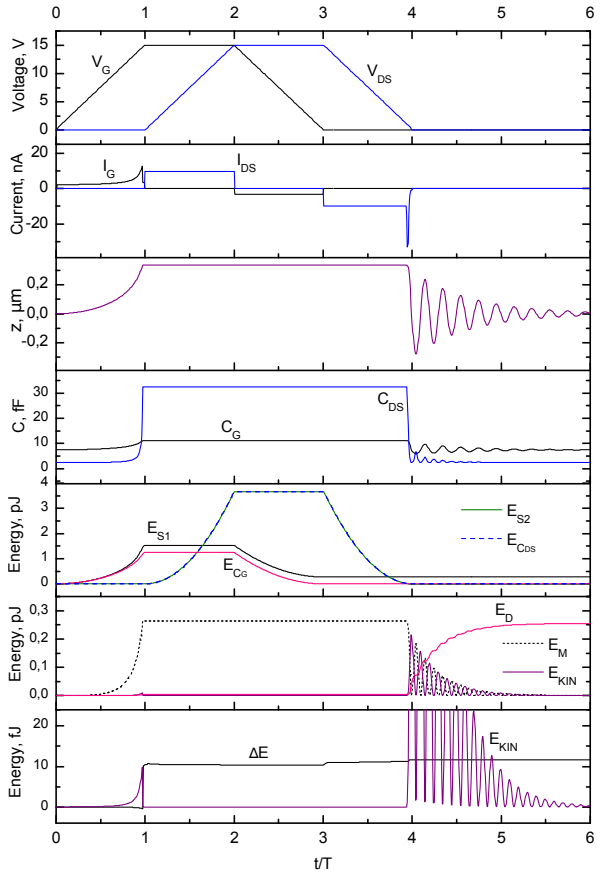

Fig. 5. Evolution of voltages applied to the 4-terminal transducer model (first graph), currents (second graph), equivalent mass displacement (third graph), capacitances (fourth graph), energy components of electrical part (fifth graph), mechanical spring energy, kinetic energy and damping loss (sixth graph), kinetic energy and energy balance (seventh graph) over time. We used the following parameters: $g_0 = 1$ μm, $t_d = 0.1$ μm, $\epsilon_d = 7.6$, $m = 1.19{\cdot}10^{-11}$ kg, k = 4.72 N/m, $b = 7.48 \cdot 10^{-7}$ Ns/m ($Q = 10$), $A_G = 8.53 \cdot 10^{-10}$ m^2, $A_{DS} = 0.47 \cdot 10^{-10}$ m^2, $f = 100$ kHz, $R_G = R_{DS} = 1$ $k\Omega$.

in the caption to Fig. 5, the ratio $\frac{C_H}{C_L}$ for C_{DS} is about 13.5, whereas the variation of C_G capacitance is not as high and does not exceed 50 %. According to (7) the output capacitance C_{DS} has a hysteresis here. For this reason, when discharging C_{DS}, only small part of the mechanical spring energy stored in the system is recovered in the second voltage source V_{PC2}. As discussed in previous section, the hysteresis in output actuator leads to unavoidable energy loss even in four-terminal device where hysteresis effect prevents to energy transfer between input and output sides.

The energy difference between stored mechanical energy and the energy recovered by the second voltage source is dissipated by damping loss after t/T = 4. The impact energy loss is only 4 % of the damping loss for this particular case, as the input has no hysteresis due to added stopper. The total dissipated energy (difference between provided and recovered energy by the two voltage sources) during one cycle is 267 fJ. The ratio of the recovered energy to the maximal energy delivered by two voltage sources is 94.8 %. Consequently, most of the energy provided is recovered. The

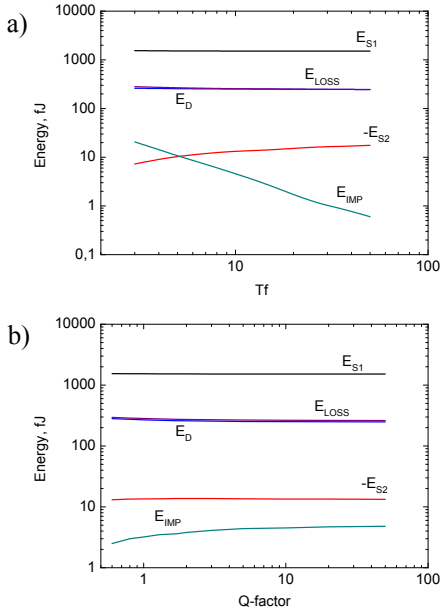

Fig. 6. Simulated energy components: (a) according to ramping time (Q = 10); (b) according to Q–factor (Tf = 10).

energy dissipated during one cycle is far from the energy dissipated by a nano-scale FET transistor which is in the order a fraction of fF. However, scalability is possible for the proposed electromechanical devices, and lower non-adiabatic part could be achieved with μ-side MEMS die. This simulation therefore allows us to verify that the proposed model is energy consistent, mostly adiabatic and can be used for further variable capacitance development.

In order to demonstrate the non-adiabatic origin of the loss, in Fig. 6a we present the effect of ramping time T on the energy components during one cycle. All other parameters are the same as in the previous calculation. The resistive loss is very small and is thus not given in Fig. 6. Increasing the ramping time decreases the impact kinetic energy loss E_{IMP}, but damping loss caused by the output hysteresis E_D stays constant and limits the total loss level E_{LOSS}. The energy recovered by the second voltage source $-E_{S2}$ slightly increases with the ramping time from 7.3 fJ for $T = 3/f$ to 17.5 fJ for $T = 50/f$. The results of simulation demonstrate presence of non-adiabatic losses for the proposed design operating with four-phase power clock.

The results for the energy components during one cycle in relation to Q–factor are shown in Fig. 6b. The ramping time is fixed and equals 100 μs ($10/f$). The increase in Q–factor practically does not affect to the total loss, which is defined by loss of stored mechanical spring energy. The maximal value of the Q–factor is limited by the idle phase between the ramping-down and ramping-up stages. This time should be sufficient to decay the vibration after output voltage decrease.

C. Cascadability

Even if gap-closing MEMS devices is not the best candidate for fully adiabatic CAL, the cascadability of the proposed

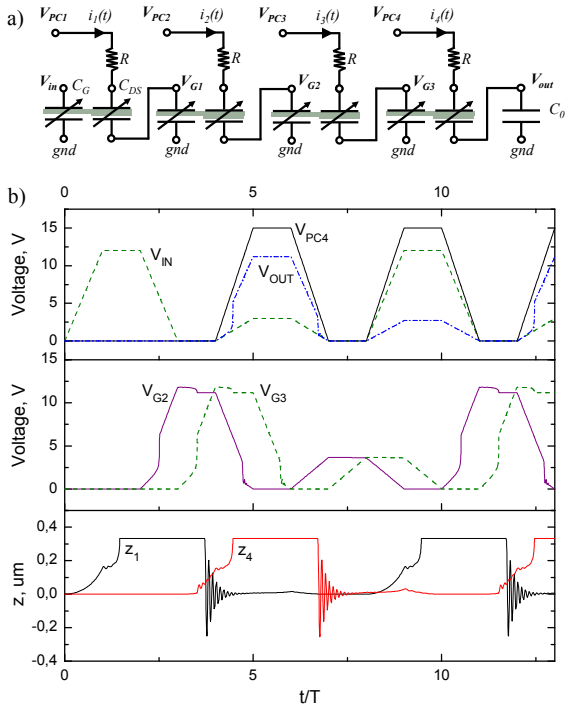

Fig. 7. a) The cascade of 4 buffers b) Spice-simulated: input voltage V_{IN}, V_{PC4}, output of the fourth buffer V_{OUT} (first graph), output of the second and third buffers (second graph), displacement of the first and the fourth moving mass (third graph) over time. $T = 100\mu$s, $C_0 = 11$ fF, the other model parameters are the same as in Fig. 5.

design is demonstrated for array of the 4 buffer elements. The test circuit is presented in Fig. 7a. The logic state is coded by the displacement, induced by input voltage. If the displacement is small, output capacitance C_{DS} is not affected by voltage V_{DS}, due to output symmetry. On the contrary, if the input and, consequently, the displacement is high, the output voltage increasing causes the moving mass displacement and collapse to the bottom electrode. The effect is shown in third graph of the Fig. 7b. The input voltage amplitude is 3 V and 12 V for "low" and "high" input level, respectively. The binary input logic word "1010" is transferred through 4 buffers as demonstrated in Fig. 7b. Energy recycling ratio equals 76 % for selected voltage levels. The system demonstrates cascadability for V_{PCmax} amplitude range from 12 to 16 V inclusive.

The developed electromechanical model of the variable MEMS capacitance has been successfully verified. In addition, the cascadability and the presence of non-adiabatic loss demonstrated for gap-closing MEMS device with four-phase PC actuation. In order to avoid this issue, a solution with a controlled dynamic should be proposed.

V. Conclusion

The present paper is focused on the loss analysis in CAL gates realized on gap-closing MEMS elements. First, we investigated two-terminal variable capacitor model and observed the well-known hysteresis problem in the context of variable capacitance with low up-state to down-state capacitance ratio. The charging of the variable capacitance with hysteresis leads to the impact kinetic energy loss during pull-in, and the discharging leads to loss of stored mechanical energy during pull-out. The latter effect is demonstrated for "pure" electrical model with hysteresis in CV-characteristics independently of the mechanical side.

To avoid the losses listed above, the design of the gap-closing variable capacitance with stopper has been proposed and discussed. In order to analyze all loss mechanisms, an analytical compact model of the variable capacitor element has been developed. With four-phase PC this design demonstrated the cascadability and presence of non-adiabatic loss, caused by the hysteresis in the output actuator. In order to avoid these issues, a solution without hysteresis and mechanical contact should be used for both electrical ports of elementary CAL device. Mechanical contact can be avoided in MEMS variable capacitance design, for example, by using comb-drive actuators.

The developed electromechanical model of the variable MEMS capacitive element will be used for further design of physically reversible CAL gates.

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