Silicon Carbide Technology of MESFET-Based Power Integrated Circuits

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Jean-François Mogniotte[1)], Dominique Tournier[2)], Christophe Raynaud[2)], Mihai Lazar[2)] Dominique Planson[2)] and Bruno Allard[2)]

1) ESTA School of Business and Technology, Université de Lyon, INSA-Lyon, CNRS, AMPERE, UMR 5005, F-69621 Villeurbanne, France,

   assistant professor, 21 avenue Jean Capelle, +33472438238, +33478433717, jean-francois.mogniotte@insa-lyon.fr

2) Université de Lyon, INSA-Lyon, CNRS, AMPERE, UMR 5005, F-69621 Villeurbanne, France

This paper has not been submitted anywhere before and has not been presented at a conference.

Abstract

This paper presents the start development of a design-kit for an innovative technology based on the same lateral topology and the same substrate, which is a dual-gate SiC MESFET. From the electrical characteristic of an initial dual-gate MESFETs, a SPICE model of this device has been established. This model allows developing by simulations a design-kit of three devices, which are respectively a signal MESFET, a buffer MESFET and a power MESFET. The signal MESFETs are dedicated to the signal command shaping. The buffer MESFETs would be used as current buffer in the driver circuit for supplying the gate electrode of the power switches. The power MESFETs would be used as power switches. The electrical measurements validate the feasibility of this technology. The characterizations have shown that the technology is operational and the three devices present the considered electrical behavior. The contact resistance technology must be improved for optimizing the electrical performances. The devices will be used for the design of electronic functions (e.g.: ring oscillator, totem-pole...) in the purpose to consider a full integrated driver in SiC, which could operate in harsh environments.

1) Introduction

The emergence of SiC power devices (BJT, JFET, Thyristor) allows to consider the design of high power converters able to operate in harsh environment especially at very high voltages (>10kV) and high temperatures (>300°C). The main applications concern embedded power systems dedicated to the harsh environments. One of the major topics is the control circuits (gate drive, protection and sensing) of the power switches. The driving circuitry converters does not exist in this temperature range. The development of basic electronic functions in SiC (comparator, oscillator...) is a preliminary step to design a fully driver demonstrator. Several laboratories have developed elementary functions as basic logical gates (NOR, NAND, circuit D flip flop), oscillator, Phase Frequency Detector … based on either JFET, BJT or MOSFET devices. High temperature operations have been reported (up to 800°C during hundreds hours) [1], [2], [3]. However, these developments have mostly been focused on the design of "logic functions" and not on laterally integrated power circuits. Ampere laboratory have designed an elementary dual-gate SiC MESFET to develop a SiC integrated circuit technology for power integrated circuits. It is an innovative technology for the harsh environments, based on the same lateral topology MESFET in the purpose to develop a system-on-chip dedicated to power applications. The MESFET technology was preferred to the MOSFET technology mainly due to the poor quality of the SiC/SiO_2 interface compared to the Si/SiO_2 one. Moreover, researches have shown that the MESFET topology

presents a good behavior for the working at high temperature (500 °C during 558h) [4]. The integration of the command stage and power stage on the same substrate presents many assets. The number of components, the volume, the weight and the economic cost of the system will be reduced. The reliability, the performances and the Electromagnetic Compatibility (EMC) will be improved. This paper presents the development of this integrated circuit technology based on a MESFET planar topology, whose the gate width could be scaling for designing a range of transistors with different drain-source current ranges. The research work focuses on the design of three types of the MESFETs (signal, buffer and power), that could be later introduced in the design of electronic functions as amplifier, comparator, oscillator. It is the starting point toward a design-kit.

2) Experimental details

The devices have been manufactured by the Institute of Microelectronics of Barcelona (IMB) and are based on the same technology used by M. Alexandru [2]. The MESFET technology has been successfully tested up to 300 °C as detailed in [2]. The inductors, the capacitors, and the resistors will be off-chip discrete components in the primary demonstrators.

The electrical characteristics of dual-gate MESFETs and SiC diodes have been measured with a semi-automatic probe station using a Keysight B1505 analyser. Additional measurements have been done in order to analyse the fabrication process uniformity across a 3" wafer. The capacitances have been measured using the impedance meter HP4194A from 20 kHz to 1 MHz with the standard harmonic measurement procedure modified for normally-on device. The statistical data provides from these electrical measurements.

The well-known JFET SPICE model have been used for the simulation of static and dynamic characteristics of the MESFETs.

In this model, the drain to source current I_{DS} is given vs. the drain-to-source voltage V_{DS} and the gate bias V_{GS} by

$$I_{DS}=k.\beta.(1+\lambda.V_{DS}).V_{DS}(2(V_{GS}-V_{TH})-V_{DS}) \quad \text{(Eq. 1)}$$

in the linear mode, and by

$$I_{DS}=k.\beta.(1+\lambda.V_{DS}).(V_{GS}-V_{TH})^2 \quad \text{(Eq. 2)}$$

in the saturation mode. V_{TH} is the threshold voltage, k is a coefficient for the geometrical area, β is the transconductance parameter and λ is the channel-length modulation

The classical SPICE model of the diode has been used for the simulation of the MESFET in switching on a RL load [5].

3) Topology of lateral double-gate MESFET

Lateral SiC-MESFETs with a dual gate have been manufactured on semi-insulating-SiC wafers [6]. Figure 1 presents the topology of the MESFET. The dual gate is constituted by a common Schottky contact G_1 and a bipolar contact G_2, which allows to consider new ways of controlling power switches. The layer N has a doping level $N_D \sim 10^{17}$ cm^{-3} and the layer P has a doping level $N_A \sim 10^{15}$ cm^{-3}. The electrode G_2 is not in the same planar level than the other electrodes in reason of the insulation technology, which is an insulation by etch for this device. The electrical measurements have validated the working of the MESFET devices and the features have been extracted to establish a SPICE model of the MESFET. These elements will be presented in the following part of the paper. This first topology is not the more appropriated for a technology of integrated circuit in particular concerning the insulation by etch and the geometrical shape of the MESFET. A second topology based on a planar insulation by P+ well implantation has been designed (Figure 2). This second topology is a planar MESFET, where the electrode G_2 is at the same level than the other electrodes. The differences between the two ways of insulation has been presented in a paper by M. Alexandru et al. [7]. Table 1, Figure 3 and Figure 4 indicate the sizing features of the both topologies.

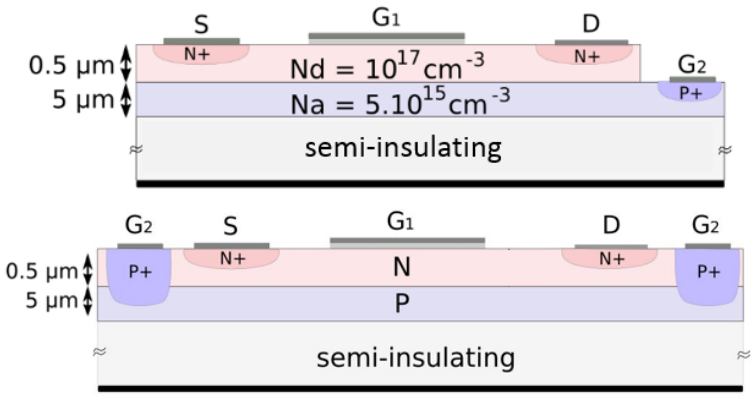


Figure 2: Cross section of the elementary MESFET with the topology 2.

Devices	Z	d	L_a	L_b	E
MESFET (1st topology)	440 µm	8 µm	640 µm	305 µm	0.5 µm
MESFET (2nd topology)	56 µm	8 µm	83 µm	38 µm	0.5 µm

Table1: Synthesis of features for the first and the second topology of the MESFET. Z and d are respectively the width and the length of the gate G1. L_a and L_b are respectively the width and the length of the elementary cell MESFET (Figure 3 and Figure 4). E is the n-type epilayer thickness.

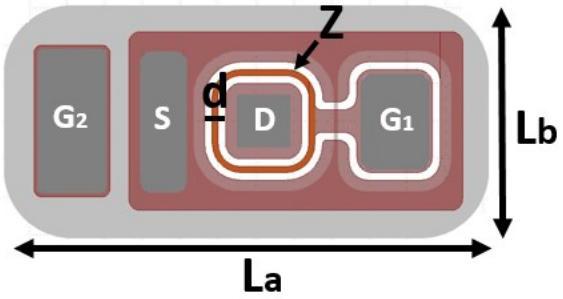


Figure 3: Top view of the mask for the MESFET based on the topology 1. The parameters are indicated in Table 1.

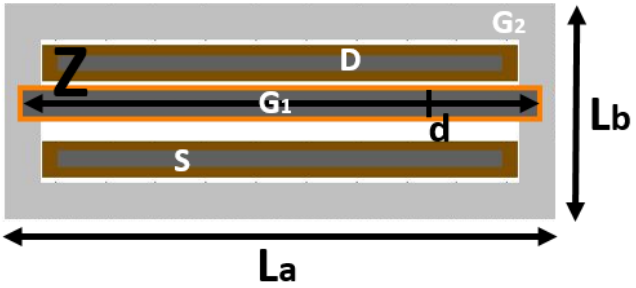


Figure 4: View of the mask top for the MESFET based on the topology 2. The parameters are indicated in Table 1.

4) Establishing a SPICE model from electrical characteristics of the dual-gate SiC MESFET

As indicated in the previous part, the topology 1 has been characterized in static conditions at room temperatures. Figure 5 shows the drain current (by unit of width Z) as a function of V_{DS} and V_{GS}. From these measurements, specific parameters have been extracted to establish an empiric model based on the

JFET SPICE model. The extraction of these parameters is based on the methodology proposed by P. Antognetti and G. Massabrio [5]. The parameters used for the SPICE model are presented in Table 2.

β (A/V)	λ (1/V)	V_{TH} (V)
$4{,}41.10^{-4}$	$5{,}16.10^{-3}$	-9.02

Table 2: Extracted parameters from the electrical characteristics of the topology 1. V_{TH} is the threshold voltage, β is the transconductance and λ is the channel-length modulation.

The experimental data are compared with theoretical curves calculated using a SPICE model and presented at CIPS in 2012 [8]. A good agreement is observed for the static characteristics in simulation excepted for $V_{G1S} = 0$ V (Figure 5). It could be explained by the fact that the SPICE model of the JFET does not take into account the self-heating effect, which is generated by the drain-to-source current. The heating involves the decrease of the charge carrier mobility that induces a decrease of the I_{DS} current in the experimental measurements. It is also probable that the gate oxide interface is not perfect. Hence, the effective channel width is smaller than designed and the minimum resistivity is higher. Moreover, this classical SPICE model is a model of a single gate device. So it does not take into account the influence of the bipolar junction linked to the gate G_2. Despite these limits, the established model is suitable to predict the static behavior of the dual-gate MESFET.

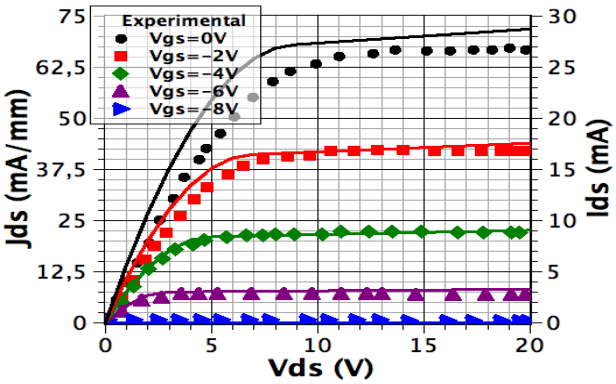


Figure 5: Comparison between simulated (lines) and experimental (symbols) static characteristics of a MESFET with the gate G_2 floating.

The capacitance C_{GD} and the capacitance C_{GS} of the device have been measured from 20 kHz to 1 MHz. These capacitances have been added to the static model to extend it to a dynamic one, which is required to simulate switching on a RL load. The JFET model allows only including the value of C_{G1D} and C_{G1S}. The capacitances of the SPICE model have been respectively set at 2 pF for C_{GD} and 5 pF for C_{GS}. Although the capacitance in the SPICE model does not match exactly with the specific structure of the dual gate MESFET (Figure 6), it is not a blocking point because the purpose is to determine a trend of the dynamic behavior. The dynamic model will allow to evaluate the capacitances for the MESFETs necessary of the future design-kit, but also the behavior of the devices in the considered demonstrator (e.g. to estimate the switching losses in a power converter, to design the gate driver).

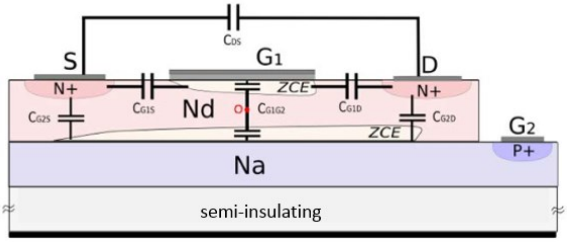
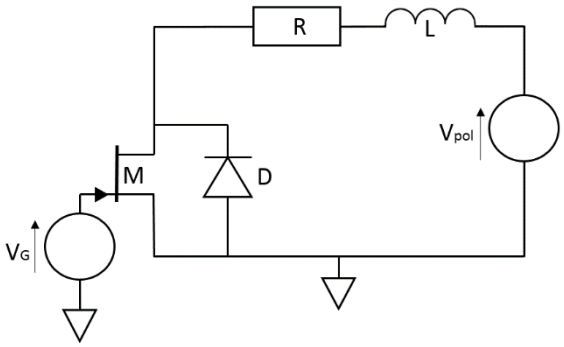


Figure 6: Cross section of the elementary MESFET with the topology 1, where the interelectrodes capacitances are represented.

Figure 7 presents the circuit used for the evaluation of the device. A diode is used to conduct the current in the circuit, when the MESFET is blocked. This diode is a SiC Schottky lateral diode in the purpose to demonstrate a fully SiC power converter. The diode has been manufactured on the same wafer as the MESFETs. It has a junction width of 10 µm and a junction length of 3.3mm. Figure 8 and Figure 9 present respectively the cross-view and the top view of the one device. It has been characterized with the Agilent B1505 and its corresponding SPICE model have the following parameters: the saturation current $I_S = 3.5\times10^{-11}$ A, the serie resistance $R_S = 57\ \Omega$, the junction potential V_J=0.79 V, the emission coefficient N=1.4, the junction capacitance C_{JO}=2.75 nF.

Figure 7: Schematic of the R-L circuit used for the switching of the SiC MESFET with R=1.1 kΩ and L=620 µF. The voltage V_{pol} is at 20 V and the gate G_2 is floating.



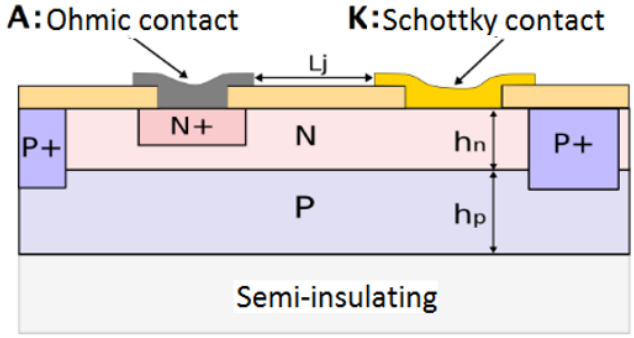


Figure 8: Cross view of the Schottky diode rectifier. A and K represented the anode and the cathode. h_n and h_p are respectively the thickness of the layer N (0.5 µm) and the layer P (5 µm). L_j is the width junction.

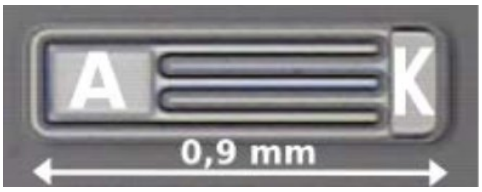


Figure 9: Photography of the top view for a Schottky diode rectifier. The length of the junction is 3.3 mm and the width junction L_j is 10 µm.

Figure 10 presents the comparison between theoretical and experimental V_{DS} as a function of time during a switching on a RL load. Both curves are in good agreement. An overvoltage of 29 V appears, when the state of the MESFET became off. This peak of overvoltage is related to the di/dt ramp of the inductor L. The MESFET presents a constant value of V_{DS} at 4 V for the state ON and the I_{DS} ~ 16 mA. The load resistor R of the circuit fixes this current.

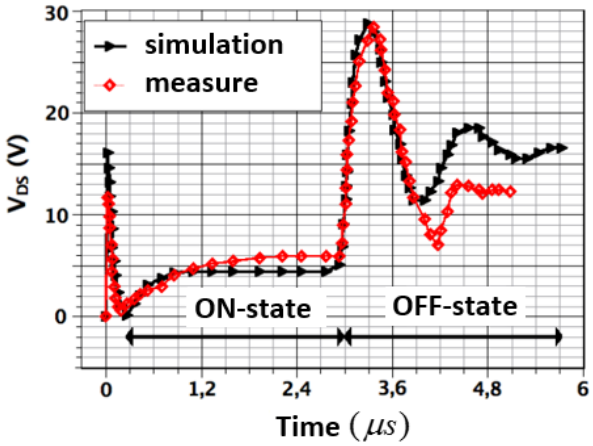


Figure 10: Comparison between simulated and measured characteristics for a switching on an RL load.

In conclusion, the SPICE model presents a good agreement with the experimental static and dynamic characterizations. The model allows predicting the behavior of the MESFET in circuits. It will be the reference model for the design-kit dedicated to the technology of integrated circuits in SiC.

5) Design for the range of MESFETs in SiC

From the SPICE model of the MESFET, the idea was to put the basis for a design-kit in the long term. Several MESFETs based on the same technology would be available as a design library with different current ratings. These devices allow to design elementary electronic functions (logical gates, comparator, oscillators…), but also buffer current circuits (amplifier, totem-pole…) and power lateral switches. For these working researches, three types of MESFET are designed from the SPICE model. The scaling of the devices has worked out as a part of a power converter, which could deliver a power density ~8 $W.cm^{-2}$. Table 3 indicates the features of the SPICE model for each components. The capacitances for the buffer MESFET and the power MESFET have been estimated from the signal MESFET assuming a constant capacitance by unit area.

Component	β (A/V)	Z (mm)	d (µm)	S (mm^2)	C_{GD} (pF)	C_{GS} (pF)
"Signal" MESFET	0.00044	0.440	8	0.03	2	5
"Buffer" MESFET	0.005	6.144	8	0.22	34	57
"Power" MESFET	0.1	99.880	8	4.08 mm^2	454	1135

Table 3: Synthesis of the main sizes from the designed MESFET for the design-kit. β is the transconductance. Z is the width of the gate G_1, d its length and S is the total area of the device.

a) Description of the geometry for the signal MESFET

The signal MESFET is designed to supply a current I_{DS}= 28 mA for V_{G1S}= 0 V and V_{DS} = 12 V with the floating buried gate G_2. To achieve this value, our SPICE model gives a value Z=440 µm. It is 8 times higher than the gate of the elementary cell (Z= 56 µm). The component is made of 8 elementary

MESFET cells connected in parallel with a multi-finger layout approach (Figure 11). This topology allows to optimize the structure of the transistor and to divide the R_{ON} by 8 in regards of an elementary MESFET with a channel width of 56 µm.

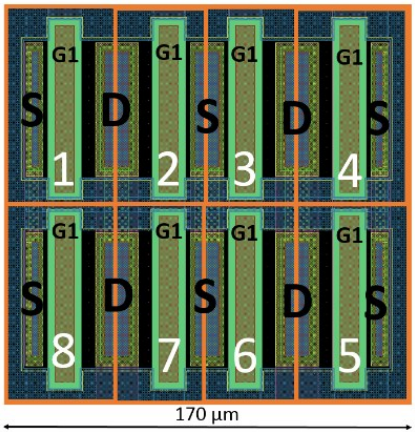


Figure 11: View of the mask for the signal MESFET, the device is made of 8 elementary MESFET cells with a gate G_1 of 56 µm, which are designed in parallel.

b) Description of the geometry for the buffer MESFET and the power MESFET

As the signal MESFET, the design of both MESFETs is based on multi-finger approach and a geometrical scalability of the elementary cell. The buffer MESFET is an intermediate device for the design-kit, which is designed for a current I_{DS} = 400 mA. It will be used for the driver circuits as buffer current. To optimize space on the wafer, the buffer MESFETs have been manufactured in a totem-pole circuit (Figure 12 and Figure 13). The PMA pad connects the source of M1A and the drain of M2A, which allows characterizing separately the devices.

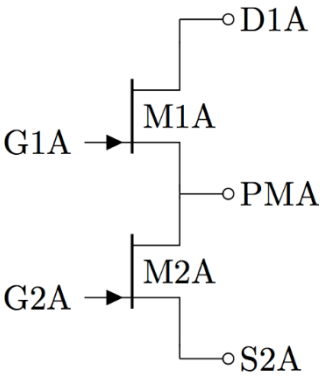


Figure 12: Schematic circuit of the totem pole.

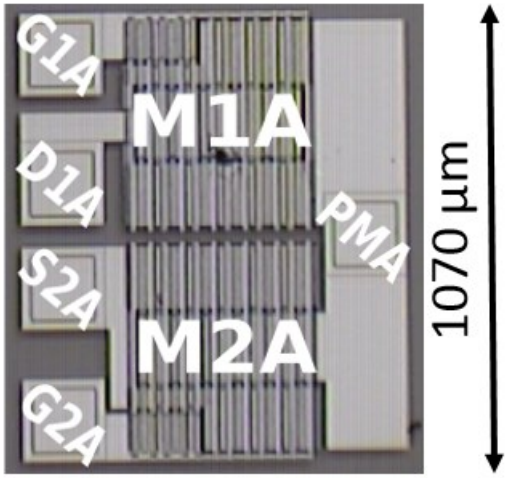


Figure 13: Photography of the top view for two buffer MESFETs (MIA1 and MIA2) connected in totem-pole topology.

The power MESFET is an association of 8 cells (Figure 14). It will be typically used as a power switch. The device is designed for a current I_{DS} = 8.5 A. The widths of the gates G_1 have been calculated, with the same assumption as for the signal MESFTET for the buffer and respectively the power MESFET.

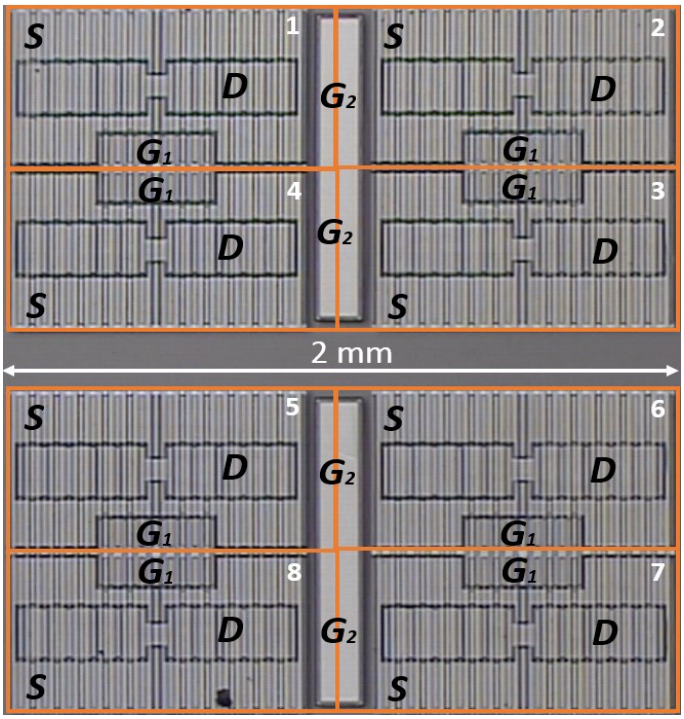


Figure 14: Top view of the mask for the power MESFET. A cell correspond to 1/8th of the whole area, whose the experimental measurements are presented in Figure 18.

6) Electrical characterizations of the SiC MESFETs

a) The signal MESFET

Figure 15 presents a typical static characteristic I_{DS}vs.V_{DS} of a signal MESFET. The electrical characteristic corresponds to the expected behaviour for a normally on transistor. The current I_{DS} is modulated by the voltage V_{GS}. The component is blocked when a negative potential is applied between the gate G_1 and the source. More the difference is important; more the MESFET reduces the passage of the current I_{DS} in the channel. The average features have been extracted from the measurements of 40 components. These values are summarised in Table 4. σ is the standard deviation. σ_high ==Average + σ and σ_low = Average - σ.

Feature	Average	σ	σ_high	σ_low
V_{TH} (V)	-15	1.3	-13.7	-16,3
R_{ON} (kΩ/mm)	1.05	0.33	1.38	0.72
$J_{DS\text{-}max}$ (mA/mm)	44.24	6.02	50.26	38.22
$J_{DS\text{-}leak}$ (µA/mm)	568	108	676	460
$J_{G1S\text{-}max}$ (µA/mm)	1.62	0.23	1.85	1.39

Table 4: Synthesis of the features extracted from the measurements of 40 signal MESFETs (R_{ON} @ V_{DS}= 0.12 V and V_{G1S}= 0 V, $J_{DS\text{-}max}$ @ V_{DS}= 12 V and V_{G1S}= 0 V, $J_{DS\text{-}leak}$ @ V_{DS}= 10 V and V_{G1S}= -20 V, $J_{G1S\text{-}max}$ @ V_{DS} = 10 V and V_{G1S} = -20 V).

In Figure 15, it must be noted that the measured current I_{DS} (e.g. at V_{G1S} = 0 V and V_{DS} = 12 V) has not the same value (17 mA) than the calculated one (28 mA) although they are in the same range. This difference can be explained by an underestimation of the drain and source contact resistances. Adding 500 Ω for each contact resistances of the SPICE model (R_D and R_S) gives a good agreement between experimental and theoretical results (Figure 16). This simulation seems to confirm the hypothesis of the high value of the resistance contact.

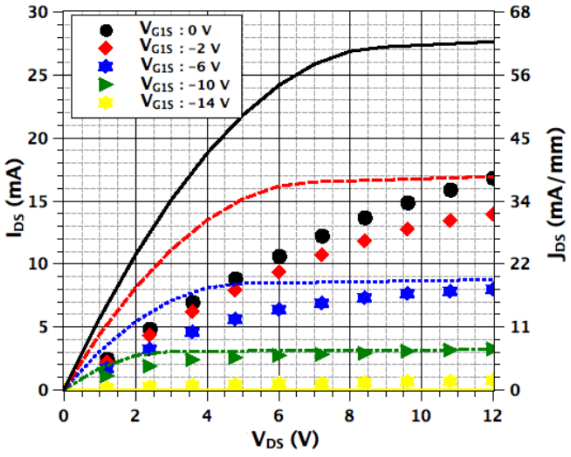


Figure 15: Comparison between the SPICE simulation of the signal MESFET and the experimental measurements of the characteristic statics $I_{DS\text{-}VS}.V_{DS}$. *Lines are for the simulation and dots for the experimental measurements.*

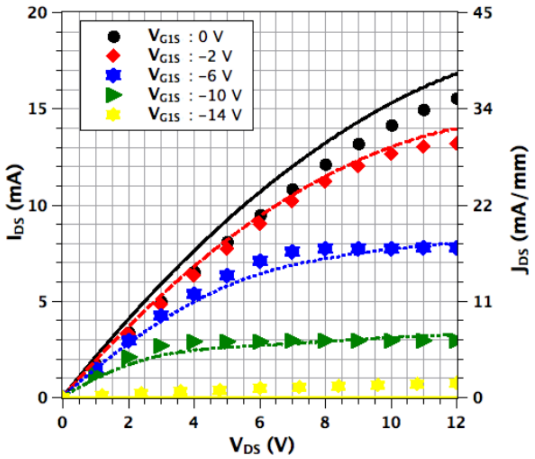


Figure 16: Comparison between the SPICE simulation by adding a contact resistance (R_D*=500 Ω and* R_S*=500 Ω) and the experimental static characteristic* $I_{DS\text{-}VS}.V_{DS}$. *Lines are for the simulation and dots for the experimental measurements.*

Furthermore, the Transmission Line Measurements (TLMs) included on the wafer give a contact resistance of 73 Ω. The SiC-IC technology is based on three levels of metallization. The elementary cells of each MESFET are connected between them by these levels of metallization to form the full device. It is possible that the high value of the contact resistance derive from defaults in these metallization layers. Unfortunately, it is not possible to check this hypothesis; it will be necessary to add test structures for each level of metallization in the future batches to deduce probably some conclusions for drawing conclusions

b) The buffer MESFET

The same characterization methodology as the signal MESFET is used for the device. Figure 17 presents $I_{DS\text{-}VS}.V_{DS}$ characteristics of a typical buffer MESFET. The buffer MESFET shows the expected behaviour. I_{DS} current can achieve 300 mA and the threshold voltage V_{TH} ~ -15 V. As for the signal MESFET, the real I_{DS} current is lower than the simulated one (300 mA against the 400 mA at V_{GS} = 0 and V_{DS} = 2 V). The explanation is the same as in the case of the signal MESFET: the difference can be explained by the value of the contact resistance (order of magnitude: kΩ). Results show that only 37% of the buffer MESFETs are functional, i.e. 51 devices on a total of 140 on the whole wafer. The average features have been extracted on these 51devices. The features of these functional devices are reported in Table 5.

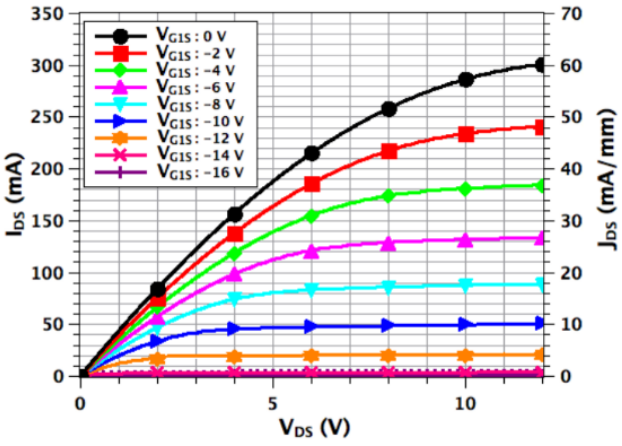


Figure 17: Characteristics statics of experimental measurements for a buffer MESFET with a G_1 *width gate of 6144 µm for different values of* V_{G1S}.

Feature	Average	σ	σ_high	σ_low
V_{TH} (V)	-14.24	0.81	-13.43	-15.05
R_{ON} (kΩ/mm)	5.01	0.59	5.60	4.42
$J_{DS\text{-}max}$ (mA/mm)	56.23	2.90	59.13	53.33
$J_{DS\text{-}leak}$ (µA/mm)	51	13	64	38
$J_{G1S\text{-}max}$ (µA/mm)	1.38	0.36	1.74	1.02

Table 5: Synthesis of the features extracted from the measurements on the 51 functional buffer MESFETs (R_{ON} @ V_{DS}= 0.12 V and V_{G1S}= 0 V, $J_{DS\text{-}max}$ @ V_{DS}= 12 V and V_{G1S}= 0 V, $J_{DS\text{-}leak}$ @ V_{DS}= 10 V and V_{G1S}= -20 V, $J_{G1S\text{-}max}$ @ V_{DS} = 10 V and V_{G1S} = -20 V). The gate G_2 was floating for these measurements.

c) Power MESFET

Due to the topology of the device, the cells are independently characterized for these electrical measurements. As the previous devices, the power MESFET is working. The current I_{DS} = 600 mA for V_{DS} = 10 V, V_{G1S}= 0 V and a floating G_2 gate (Figure 18). The expected current from the simulation was 1 A, but the value of the current is lower because of the contact resistance. This difference will lead to have a power MESFET with a current I_{DS} =4.8 A instead of 8 A. The average features extracted from the electrical measurements on 22 devices represent only 10% of all power components on the wafer. Table 6 presents the synthetises of the data.

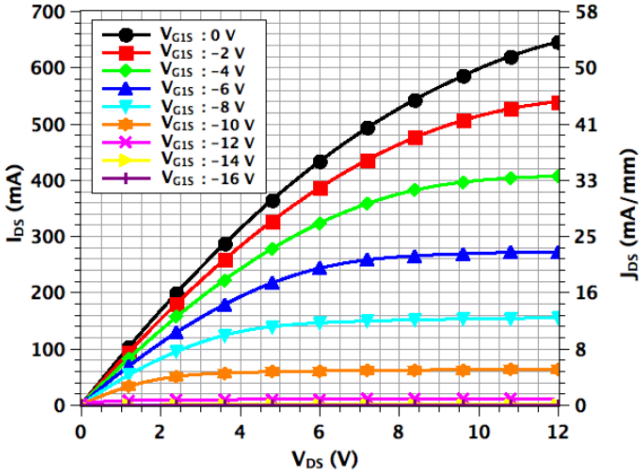


Figure 18: Experimental static characteristics for a cell (1/8th of the whole area) of the power MESFET with a G_1 width gate of 9.9 cm for different values of V_{G1S}.

Feature	Average	σ	σ_high	σ_low
V_{TH} (V)	-14.59	1.37	-13.22	-15.96
R_{ON} (kΩ/mm)	1.03	0.20	1.23	0.83
$J_{DS\text{-}max}$ (mA/mm)	54.97	1.2	56.17	53.74
$J_{DS\text{-}leak}$ (µA/mm)	83	20	103	63
$J_{G1S\text{-}max}$ (µA/mm)	8.3	1.6	9.9	6.7

Table 6: Synthesis of the features extracted from the measurements of the 22 functional power MESFET cells (R_{ON} @ V_{DS}= 0.12 V and V_{G1S}= 0 V, $J_{DS\text{-}max}$ @ V_{DS}= 12 V and V_{G1S}= 0 V, $J_{DS\text{-}leak}$ @ V_{DS}= 10 V and V_{G1S}= -20 V, $J_{G1S\text{-}max}$ @ V_{DS} = 10 V and V_{G1S} = -20 V). The gate G_2 was floating for these measurements.

d) Transconductance of the MESFETs

The transconductances g_m of the MESFETs are represented on Figure 19. The transconductances have been extracted at V_{DS}= 10 V with the floating gate G_2. The behaviours of the transconductances are relatively similar. g_m is virtually zero for the values of V_{G1S} between -20 V and -15 V. g_m increases until V_{GS} = -5 V. Next, the g_m decreases until 0 V. The maximum deviation between the three

transconductances is 37 %. This parameter is an indicator checking the experimental realization of the three lateral SiC MESFETs considered for the integrated circuits.

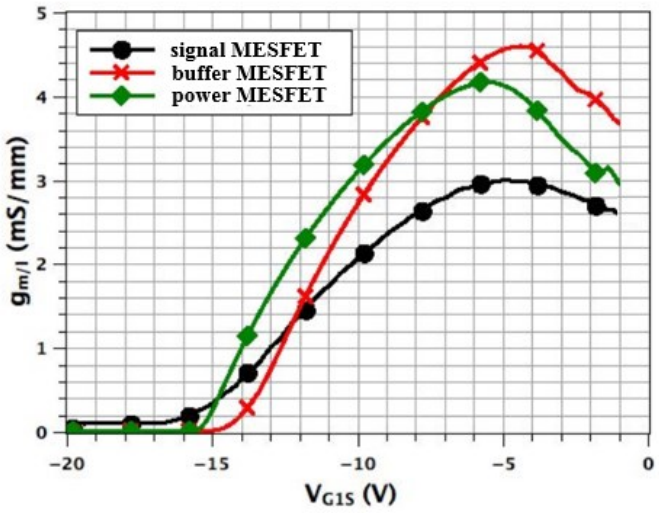


Figure 19: Comparison between the transconductance g_m vs V_{G1S} of the three MESFETs for a V_{DS} of 10 V with the floating gate G_2.

e) Polarization of the gate G_2

The polarization of the gate G_2 has an impact on the I_{DS} current. Figure 20 presents a comparison of the characteristic statics $I_{DS-VS}.V_{DS}$ for a signal MESFET, when G_2 is floating and when G_2 is connected to G_1. It appears that in the second configuration the MESFET presents a better performance for the blocking the current I_{DS}. This behavior has been observed for the three types of MESFETs. The polarization of the gate G_2 involves the modulation of the current value I_{DS} through the channel of the MESFET following the appearance of an area space charge at the level of the buried P^+ layer.

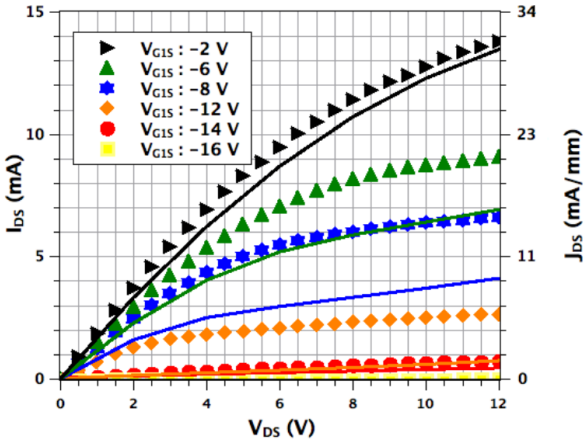


Figure 20: Comparison between the characteristic statics I_{DS-VS} V_{DS} of a signal MESFET, where the gate G_2 is floating (symbol) in a first configuration and the gate G_2 is connected to G_1 (lines) for a second configuration.

f) Breakdown voltage measurement

The breakdown voltage has been measured up to 800 V on a cell of the power MESFET with V_{G1S} = -15 V for blocking the device. The experimental results are displayed in Figure 21. No abrupt breakdown has been observed up to 800 V. However, the drain-to-source leakage current increases monotonically up to ~20 mA/mm. The drain to source leakage current seems to be due to the G_1S current, which represents nearly 10% of the I_{DS} value, but also to the quality of the crystal as discussed in the next part.

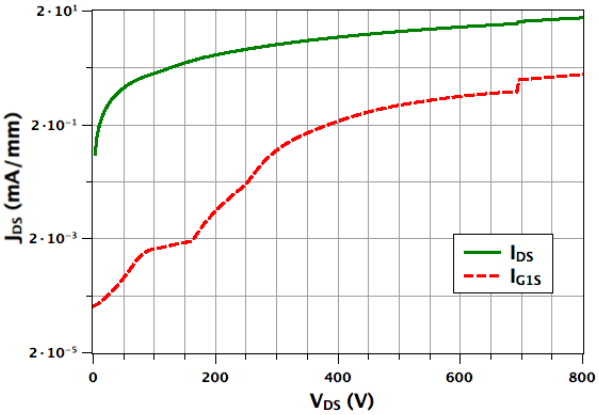


Figure 21: Breakdown voltage measurement for a cell of the power MESFET with V_{G1S} at -15 V and the gate G_2 floating.

g) Comparison of the gate leakage current J_{G1S}

The average values of the maximum gate leakage current J_{G1S} by unit length of the three MESFETs are reported in Table 7. The average has been calculated on the working devices. It represents 40 signal MESFETs (Z = 440 µm), 51 buffer MESFETs (Z = 6.1 mm) and 22 areas for the power MESFETs (Z = 1.2 cm). For the power MESFET, the value is 1.2 cm and not 9.9 cm because the measurements have been made cell by cell. The values for each device are in the same order of magnitude. The power MESFET has a current J_{G1S} 5 times larger than the current of the signal device for an area 17 times larger. These results seem to indicate that the value of the leakage gate current depends rather on the geometrical topology than on the gate width of each device.

MESFET	signal	buffer	power
$J_{G1S\text{-}max}$ (µA/mm)	1.62	1.38	8.31

Table 7: Average values of the maximum current J_{G1S} for the three MESFETs by unit length measured at – 50 V (V_{G1S}).

The analysis has shown that the size of the MESFET has an impact on the number of MESFET, which are working. Higher the surface is and lower is the rate of working MESFETs. Indeed, for the buffer MESFET only 37 % are functional and only 10 % of the power MESFET are functional on the wafer. Many devices, which do not work, have a current J_{G1S} higher than 10 µA/mm. A first hypothesis could be the non-uniformity of the n-type doping level, which could involve a lowering of the Schottky barrier and an increase of the leakage current. Another hypothesis could be the crystal quality. It is well known [9] that the presence of defects such as micropipes is responsible for a reduction of 50 to 70 % of the breakdown voltage compared to the theoretical value and that it is cripple for working components. The presence of threading dislocations is also suspected to increase leakage currents [10].Therefore a device with a high surface has a high probability to have crystal defaults and do not operate. The results seem to confirm this trend because the area of the power MESFET (4.08 mm^2) is higher than the area of the buffer MESFET (0.22 mm^2) and the signal MESFET (0.03 mm^2). The manufacturing process is perfectly adapted for the devices with a surface~0.03 mm^2 (signal devices), but the quality of the crystal and the process must be improved for the devices which have a larger area (buffer and power). It is one of the key for the design of power integrated circuits in SiC.

Conclusion

This paper presents the methodology for the establishment of a starting design-kit based on a dual-gate topology MESFET. From an empirical SPICE model, a new topology of the MESFET has been designed. This elementary MESFET cell with a channel width of 56 µm is used for the design of three specific MESFETs: the signal MESFET, the buffer MESFET and the power MESFET. The first device is dedicated to the analog electronic functions. The second device is for the driver circuit in the purpose to supply current for the gate of the power switches (buffer circuits). The last component is for the power switches of the converters (power component). The electrical measurements have shown that the

MESFETs are functional with the expected static and dynamic behaviors. The analyses have shown several differences between the simulations and the experimental results. These differences can be improved by the optimization of the technology process (e.g. decreasing contact resistances, better quality of the crystal…) for the following batches. The analysis of the measurements shows statistically that larger are the device active areas, weaker is the ratio of functional MESFETs (only 37%, resp. 10% of the buffer, resp. power MESFET are functional). The reduction of the defaults in the SiC crystal will allow to overcome the technology barrier for the integration of the power devices in order to design a full-integrated power converter circuit for harsh environments. The following step of this work will be the realization of this power circuit based on these SiC MESFETs technology.

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