An inductorless CMOS UWB pulse generator with active pulse shaping circuit

Sylvain Bourdel, R. Vauche, O. Ramos, E. Muhr, Jean Gaubert, N. Dehaese, Herve Barthelemy

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S. Bourdel[1], R. Vauché[2], O. Ramos[1], E. Muhr[1], J. Gaubert[1], N. Dehaese[1], H. Barthelemy[3],
[1]Aix-Marseille University, [2]ISEN-Toulon, [3]Toulon University, IM2NP, and CNRS
Campus de Saint-Jérôme, Case 142
Avenue Escadrille Normandie Niemen
F-13397 Marseille, France

***Abstract*— The design of an UWB pulse generator is presented. The pulse generator is based on an elementary pulse combination technique which enables the emitted pulse to be precisely shaped. This technique is implemented with no inductor or passive network and can be used to ensure regulation compliance. This generator has been fully integrated in a 0.13 µm CMOS standard technology. Its area is 0.06mm^2 only and it can be programmed to synthesize different pulse shapes. For FCC compliant pulse shapes, the maximum measured 10dB bandwidth is 3.5GHz, and the maximum peak to peak magnitude is 220mV. The measured maximal power consumption is 87.6mW at 800MHz Pulse Repetition Frequency (PRF).**

***Pulse Generator, UWB, FCC, CMOS, Impulse Radio, Pulse Shaping*.**

I. INTRODUCTION

Interest has grown for Ultra Wide Band (UWB) Impulse Radio (IR) applied to low cost communication systems since it was proposed as a possible physical layer for the IEEE 802.15.4 standard. Recent works show the potential of IR for power saving thanks to the low energy of the emitted pulse and also for multipath resistance, due to the use of energy detectors in low cost receivers [1]. Since of those advantages, IR is also well suited to other low cost applications such as Body Area Network (BAN) [2], Radio Frequency IDentification (RFID) [3] and Sensor NetWork (SNW).

Currently, most pulse generator topologies for UWB-IR require inductors or a passive pulse shape networks to operate which is a major drawback for CMOS integration and production cost. Typically, the LO switching technique uses LC topologies [6] and the filter excitation technique needs a passive resonator [4] for their implementation. To limit the use of inductors, architectures based on ring oscillators or based on digital pulse shaping have been proposed [5][9][10][7]. However, according to recent publications, those techniques still use passive components (filters, baluns or matching cells) that shape the pulse in order to comply with regulation spectrum masks. To reduce the need for such passive networks, a solution is to design pulse generators with active pulse shaping circuits. Active pulse shaping techniques enable a better control of the output spectrum. It can especially be used to reduce the side lobes of the output spectrum which limit the Adjacent Chanel Power Ration (ACPR) in the case of multi-band communications. For example, a side-lobe rejection of 20dB is needed to comply with IEEE 802.15.4a standard. Among the different pulse shaping techniques already presented [12], only a few of them enable the reconfiguration of the shape. The elementary pulse combination technique appears to be well suited to the design of pulse synthesizers with pulse shape tuning capabilities [8] [9] [11].

In this paper, we present a practical implementation in a 0.13µm CMOS technology of a technique described in [8]. Some measurement results of different pulse shapes are also presented to validate the efficiency of the tuning capability of the proposed pulse generator. The first section of this paper presents the principle of pulse synthesis used in the proposed pulse generator. The circuit design is detailed in the second section and the measurement results are given in the last part.

II. PULSE SYNTHESIS PRINCIPLE

The pulse synthesis technique consists in combining elementary baseband pulses ($e_n(t)$) in order to generate a more complex signal. A bandpass pulse ($p(t)$) can be expressed as follows :

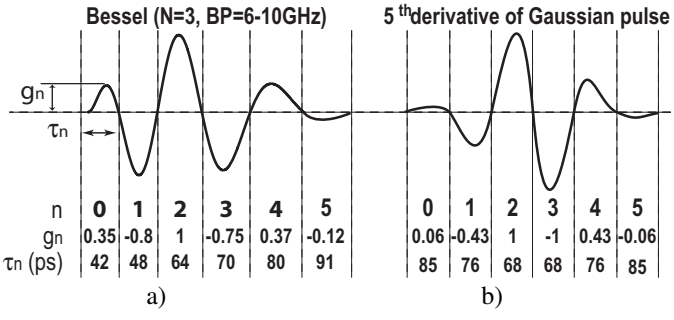


Fig. 1. Bessel impulse response (a) and 5th Gaussian pulse (b) with their associated parameters (g_n and t_n) for pulse synthesis.

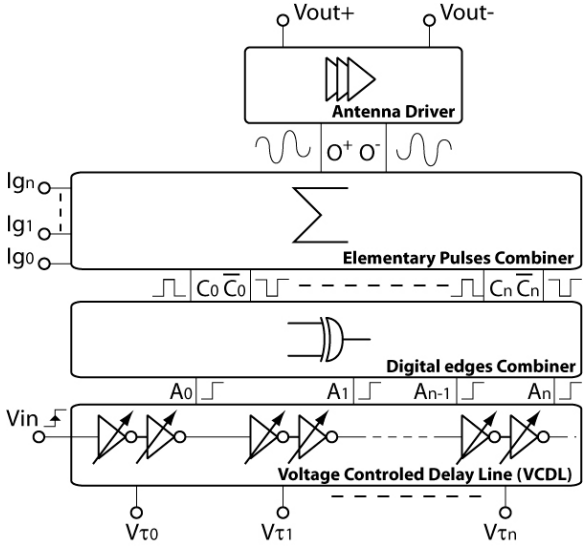


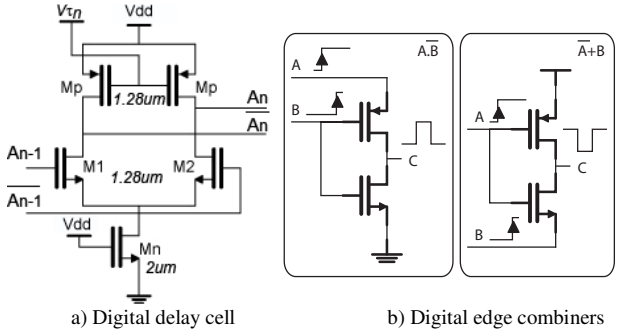
Fig. 2. Principle of the presented pulse generator

$$p(t) = \sum_{n=0}^{N-1} g_n . e_n \left(t - \sum_{p=-1}^{n-1} \tau_p \right) \quad with \quad \tau_{-1} = 0 \quad (1)$$

where g_n and τ_n refer to the magnitude and the width of the n[th] elementary pulse ($e_n(t)$). In Fig. 1 two different bandpass pulses are plotted with their associated coefficients (g_n and τ_n): the 5[th] derivative of a Gaussian pulse (named 5[th] Gaussian pulse in this paper) and the impulse response of 3[rd] order Bessel filter (named Bessel pulse in this paper). The 5[th] Gaussian pulse is known to be FCC compliant [13] and the Bessel pulse presented here has a 4GHz bandwidth centered at 8GHz. Moreover, $p(t)$ spectrum is slightly dependant on $e_n(t)$ shape. This enables FCC compliant pulses to be synthesized with the same elementary pulse ($e(t)$) having the same width τ [11] which reduces the system complexity.

III. UWB Pulse Synthesizer Design

The principle of the synthesizer is given in Fig. 2. It consists of a Voltage Controlled Delay Line (VCDL) that propagates a rising edge. Two consecutive edges (A_{n-1} and A_n in Fig. 2) are then combined to produce complementary elementary baseband pulses (C_n and $\overline{C_n}$ in Fig.2). Varying delay cells are used in the VCDL to control the width (τ_n) of the elementary



a) Digital delay cell b) Digital edge combiners

Fig. 3. Logic cells of the synthesizer

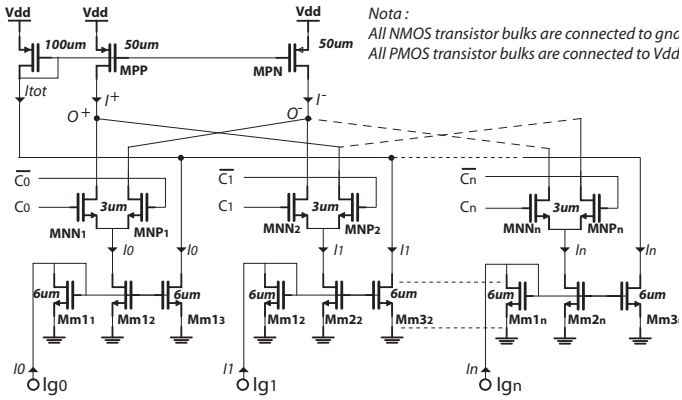


Fig. 4. Elementary pulse combiner

pulses. Complementary pulses are needed here because differential pairs in the elementary pulse combiner are used. Once the elementary pulses are combined, the resulting bandpass pulse is applied to a 50Ω antenna using a driver. The antenna is driven in a differential mode in order to maximize the output power.

The delay cells are MOS Current Mode Logic inverters [4] shown in Fig.3a, and provide very low delay. An external bias voltage is applied at node $V\tau_n$ to control the width of the elementary pulses (τ_n). Varying this bias voltage modifies the dynamic resistance of the transistors Mp which in turn changes the delay of the cell. The logic gates that make the edge combination are fast logic gates and use only two transistors as shown in Fig.3b. Those fast logic gates are connected to the output nodes of the delay cells and achieve $A_{n-1}.\overline{A_n}$ and $\overline{A_{n-1}} + A_n$ functions. Dummy cells are also connected to nodes $\overline{A_n}$ in order to avoid mismatch because only A_n is used by the logic gates. Inverters are added between the delay cells and the edge combiner to reduce the rising time of the output delay cell signal.

The elementary pulse combiner is based on traditional two-transistor differential pairs (MNN_n and MNP_n) as shown in Fig. 4. Each baseband pulse and its opposite (C_n and $\overline{C_n}$) are applied to the differential input of the pair to produce a differential impulse current through the output nodes O^+ and O^-. The combination of each elementary pulse is achieved at node O^+ and O^-. The crossing of each pair output with the following one alternates the polarity of two successive elementary pulses which is necessary to synthesize the pulse

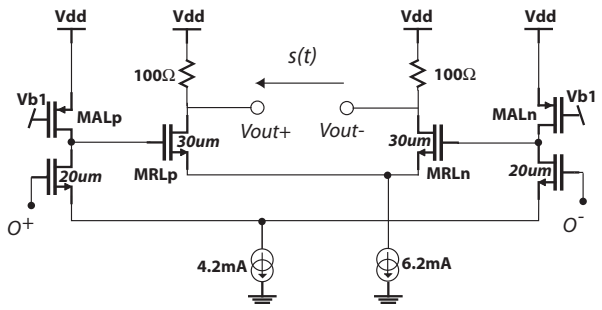


Fig. 5. Antenna driver

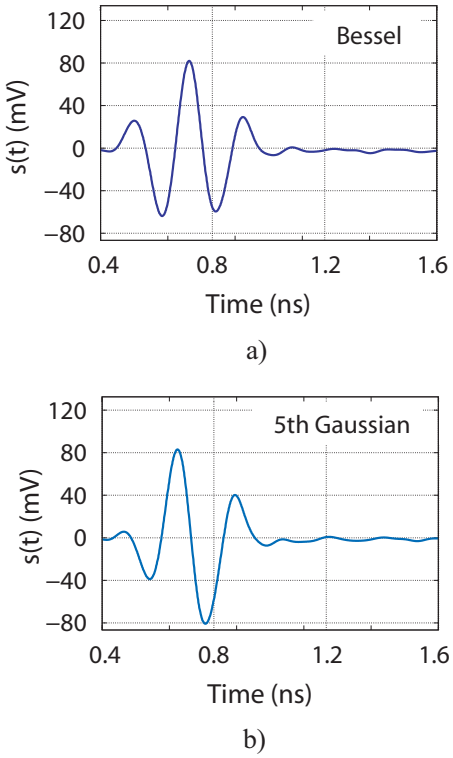


Fig. 6. Measured time response of the differential output (s(t)) for a Bessel pulse synthesis (a) and a 5th Gaussian pulse synthesis (b)

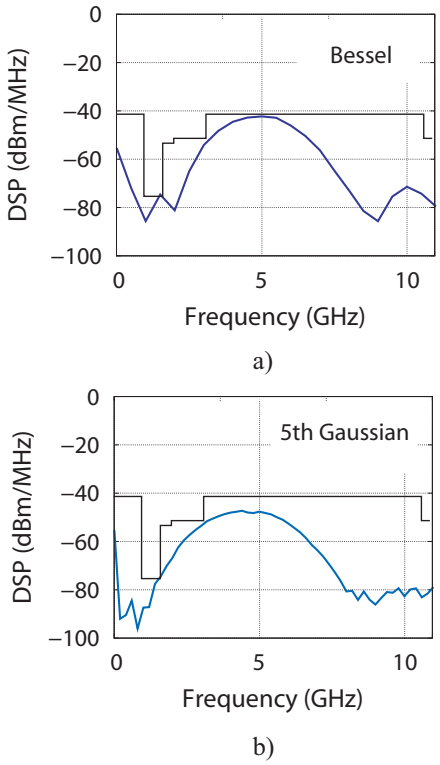


Fig. 7. Measured frequency response of the differential output (s(t)) for a Bessel pulse synthesis (a) and a 5th Gaussian pulse synthesis (b)

shown on Fig. 1. External bias currents I_0 to I_n are applied at nodes Ig_0 to Ig_n in order to control the elementary pulse magnitude (g_n). Varying I_n changes the gain of the differential pair which modifies g_n. To maintain a constant bias voltage at the nodes *O+* and *O-* when I_n vary, two active loads (*MPP* and *MPN*) are used. *MPP* and *MPN* are biased by I_{tot} which is the sum of all the bias currents (I_n) obtained by current copy with $Mm1_n$, $Mm2_n$ and $Mm3_n$.

The antenna driver is presented in Fig. 5 and consists of a common source amplifier with a resistive load driven by a common source stage with an active load. Both stages operate in A class. The output stage is designed in order to drive a simple dipole antenna in differential mode. Thus, the 100Ω output loads leads to a 50Ω differential impedance and no coupling capacitors are used. Active loads (MAL_p and MAL_n) are biased with the same current copy structure used in the elementary pulse combiner. Since this topology is sensitive to common mode effect, the driver has been intensively characterized with Monte-Carlo simulations in order to maintain the gain over a large range of PVT variation.

IV. Measurement Results

The pulse synthesizer has been implemented in a 0.13µm CMOS technology from ST-Microelectronics. The order of the implemented synthesizer is N=7 to generate a signal composed of seven elementary pulses. Seven external current sources connected to nodes Ig_0 to Ig_6 are used to control the elementary pulse magnitudes and only one voltage source ($V\tau$) is used to set their width at the same value ($\tau_n = \tau$). The use of a unique control voltage to tune the width of the elementary pulses reduces the number of I/O pads. All the presented pulses are obtained only by tuning these external sources. Measurements are performed with a two channel Agilent DSO81204B real-time oscilloscope.

The two pulses presented in Fig. 1 have been synthesized and their measured time responses are presented in Fig.6 without cable loss compensation. The values of I_n have been slightly tuned resulting in the pulse spectrums which are compliant with FCC as represented in Fig.7. Suppressing the lower side lobes present in the output power spectrum is commonly a difficult issue which limits FCC standard compliance [12]. Using the tuning capabilities of the pulse generator, the lower side lobe has been significantly reduced as shown in the Fig. 6 and Fig. 7. The generated Bessel and 5th Gaussian pulse exhibit a lower side lobe rejection of 30dB and 38dB respectively.

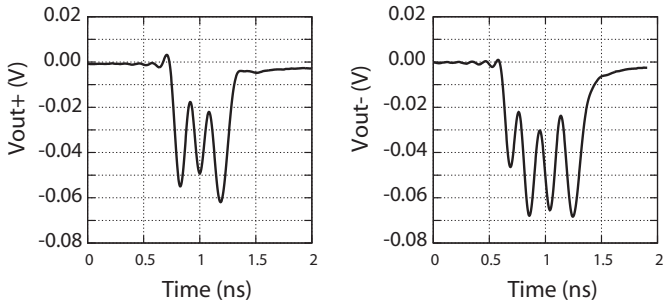
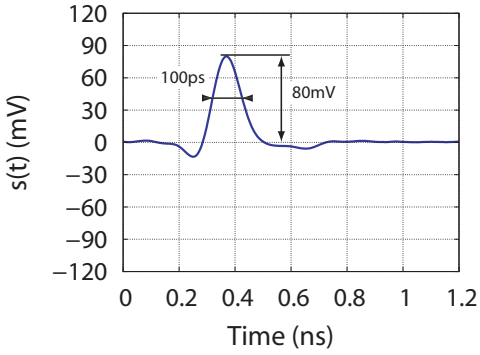
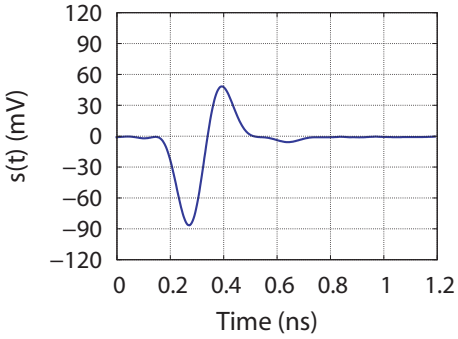


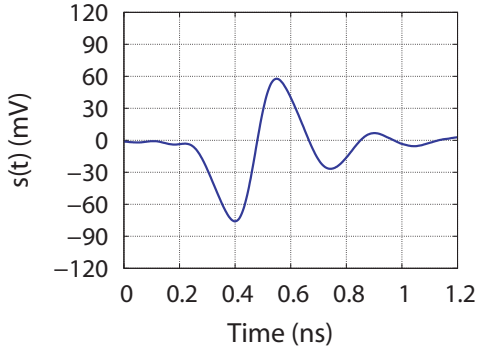
Fig. 8. Filtering effects on the outputs.



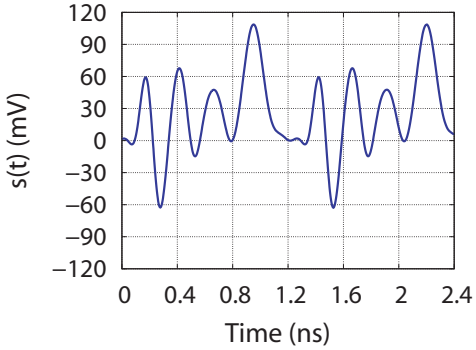
a) Elementary pulse



b) Monocycle pulse



c) Combination of 3 elementary pulses



d) Arbitrary waveform at maximal PRF

Fig.9. Measurement of the tuning Capabilities

When FCC compliant pulses are synthesized, the maximum output peak to peak magnitude is 220mV (taking into account 3dB cable loss). In this case, the maximum 10dB bandwidth is 3.5 GHz and is centered at 4.9GHz. Compared to the theoretical pulses of Fig.1, the bandwidth is reduced. This is due to the limited bandwidth of the antenna driver and also due to the long interconnection wires between all the differential pairs (nodes O^+ and O^- in Fig. 4).

As shown in Fig. 8, this filtering effect changes the pulse shape and needs to be compensated. Here, the compensation is achieved directly by tuning the values of I_n. Due to this compensation, the values of I_n are not a linear function of g_n and are, for the 5th Gaussian pulse: I_0=0, I_1=520uA, I_2=1.9mA, I_3=3.1mA I_4=1.98mA, I_5=0.6mA, I_6=0.07mA. The value of V_τ is 0.4V. Such a compensation technique could also be applied to cancel other effects that might change the pulse shape like PVT variations.

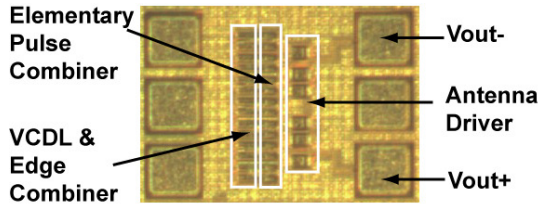


Fig. 10. Chip micro-photograph

As presented in Fig. 9a, the measured minimum width of an elementary pulse is 100ps. This minimum width (τ_{min}) set to $1/(2.\tau_{min})$=5GHz the maximal center frequency which can be achieved by the synthesizer. For such a width, the magnitude of an elementary pulse can be tuned from 0 to 80mV. Depending on the number of elementary pulses used, the pulse generator can synthesize baseband pulses (Fig. 9a), monocyle pulses (Fig. 9b) or arbitrary waveforms (Fig. 9c and Fig. 9d).

The maximal measured Pulse Repetition Frequency (PRF) is 800MHz and is presented in Fig.9d using an arbitrary waveform of 7 elementary pulses. With such a high PRF, this topology is able to generate quasi-continuous waves having a time period equal to $T=N\tau$.

The measured jitter is lower than $25ps_{pp}$ and could be further reduced by using a DLL instead of a simple VCDL. The total power consumption for the pulse presented in Fig.9d is 87.6mW@800MHz and is the maximum measured power consumption. For such a PRF, the energy consumed by pulses is 110pJ. Here more than 50% of the power is consumed by the output stage which is designed with no inductor in order to reduce the silicon area. This design strategy results in a circuit (shown in Fig. 10) having an active silicon area (excluding the pads) of $0.06mm^2$ only. TABLE I shows the good performance of the generator in terms of tuning capabilities and integration.

TABLE I : PERFORMANCE COMPARISON WITH PREVIOUSLY PUBLISHED WORKS

Ref.	Vpp (V)	Vdd (V)	BW (-10dB)	Power Cons.	Integration				Pulse Shape Reconfiguration
					Area (mm^2)	Tech.	On-Chip Inductors	Off-Chip Passives	
[9] - 2007	1.24	2.2	1.4GHz	29.7mW@36MHz	0.4 (core)	0.18µm CMOS	No	Yes	Yes
[4] - 2010	1.42	1.2	6.8GHz	3.84mW@100MHz	0.54 (die)	0.13 µm CMOS	Yes	No	No
[10]- 2008	0.22	1.2	4GHz	129mW@1.8GHz	2.83	0.09µm CMOS	(balun)	No	No
[5]- 2007	0.65	1	550MHz	-	0.08 (core)	0.09 µm CMOS	No	Yes	No
[7] 2009	0.67	2.1	4.5GHz	1.38mW@50MHz	0.11 (core)	0.18 µm CMOS	Yes	No	No
[6]- 2008	0.16	1.5	520MHz	1.68mW@100MHz	0.3 (core)	0.18 µm CMOS	Yes	No	No
This Work	0.22	1.2	3.5GHz	87.6mW@800MHz	0.06 (core)	0.13 µm CMOS	No	No	Yes

V. CONCLUSION

The design of an UWB generator based on pulse synthesis is proposed and implemented in a 0.13µm CMOS technology which is well suited for low cost applications. The pulse generator can be programmed to synthesize different pulse shapes. The tuning capabilities that are demonstrated can be used for different needs such as side lobe suppression or impairment reduction. Our pulse generator is fully integrated in a 0.13µm CMOS technology. It is designed without inductors, baluns or additional passive networks and it can synthesize FCC compliant pulses.

VI. ACKNOWLEDGEMENTS

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VII. REFERENCES

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