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Design of Class-F Power Amplifier with Feedback and Compact Microstrip Resonant Cell

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Abstract
Design of a class F power amplifier (PA) with microstrip feedback and compact microstrip resonant cell (CMRC) by using of the pHEMT ATF-34143 transistor is presented. To have suppress the third harmonic (7.2 GHz) a CMRC with miniaturized size and -50 dB suppression level is designed. On the other hand, a feedback with microstrip lines is used to increasing stability factor without changing the efficiency. Aim of this feedback is increasing stability factor (K) and to create unconditional stability of circuit. The drain voltage and fundamental frequency of the proposed PA is 1.5 V and 2.4GHz, respectively. The power added efficiency of the proposed class-F PA is equal to 61% with 10.2 dB of power gain under 10dBm input power.

Keywords: Class-F Power Amplifier, Harmonic Control Circuit, Microstrip.

Introduction
The use of wireless communication system has become a natural thing. Power amplifiers are used to radars and radio transmitters, in the last section before antennas. Due to the power amplifier (PA) has high energy consumption, improving of power amplifier efficiency is a challenging for designers [1]. High efficiency of the power amplifier can be obtained by using overdriven class-B, class-F, or class-E operation modes and their subclasses, depend on the technical requirements [2, 3]. Class-F power amplifier with creating square drain voltage waveform and half-sinusoidal drain current waveform, can be obtain to high efficiency. High efficiency means reducing power consumption and longer lifetime for the battery [4, 5]. A method to increase power added efficiency (PAE) of class-F power amplifiers is presented in [6, 7]. This method is a microstrip harmonic control circuit design by using parasitic effects of the transistor output. Although, this PA has a high PAE, but the drain voltage is 28 V.

Harmonic control circuit (HCC) have the most important role in designing class-F power amplifier. In [8, 9], a CMRC as HCC to class-F power amplifier design is presented. In [10, 11], front coupled tapered compact microstrip resonant cell (FCTCMRC) is used to a class-F PA design, which creates short circuit for second harmonic and open circuit for third harmonic. In [12, 13], a bow-tie shaped CMRC as harmonic control circuit (BShCC) is presented which has acceptable efficiency but the size of CMRC is relatively large. On the other hand, in [4-6] using of CMRC instead of HCC may cause instability in the amplifier circuit. In this paper, a new method for the design of harmonic control circuit for power amplifier class-F with CMRC and microstrip feedback is proposed. An advantage of this CMRC is miniaturized size without affecting on matching circuit. In this design, pHEMT ATF-34143 transistor is used that obtained a power added efficiency of 61% and output power of 20.2 dBm under 10dBm input power.

Class-F power amplifier
Class-F power amplifier is one of the important switching mode power amplifiers, which can provides theoretically 100% drain efficiency. The PAE equation can be express as follow [14]:

\[
PAE \% = \frac{P_{out} - Pin}{P_{dc}} \times 100
\]  (1)
\[ P_{dc} = P_{out} - P_{in} + P_{diss} \]  

Hence, the power dissipation \((P_{diss})\) can be calculated from:

\[ P_{diss} = \frac{1}{T} \int_{-T}^{T} (V_d \times I_d) dt \]  

So,

\[ PAE \% = \frac{P_{out} - P_{in}}{P_{out} - P_{in} + P_{diss}} \times 100 \]  

According to (4) the PAE can be increase, by reduction the power dissipation. As shown in figure 1, class-F PAs reduces the power dissipation, by creating half-sinusoidal waveform for drain current and square waveform for drain voltage [15].

![Figure 1](image1.png)

(a) Voltage and current waveforms (a) without harmonic control, and (b) with harmonic control

Figure 1(a) shows drain voltage and current waveforms without control harmonics that the purple section is the power dissipation. As shown in figure 1(b), by changing the shapes of drain voltage and current waveforms, the power dissipation can be reduce.

**CIRCUIT DESIGN**

To achieve high PAE, a CMRC as shown in figure 2 (a) has been designed to suppress the third harmonic. Figure 2 (b) shows the CMRC S-parameters response. The proposed CMRC create infinite impedance at the third harmonic. So, fundamental and third harmonic add with together and the drain voltage waveform changes to square waveform. The total size of the proposed CMRC is only 3.5×3.5 mm², which is miniaturized. The physical dimensions of the proposed CMRC are illustrated in figure 2 (a).

![Figure 2](image2.png)

(a) The layout of the proposed CMRC and (b) its S-parameters responses
The proposed class-F PA is depicted in figure 3 (a), which $C_1$ and $C_2$ are the DC blocking capacitors and $C_3$ and $C_4$ are the bypass capacitors. Moreover, the quarter wave length transmission lines are connected between the DC voltage supply and the transistor, in order to separate high frequency signal leakage in to DC voltage supply. In this circuit two microstrip lines (TL1) and (TL2) as compensator are used to matching the CMRC with output impedance of the transistor and to reduce the capacitive and inductive effects of the output of the transistor. The drain voltage and current waveforms are shown in figure 3 (b).

In figure 3 (b), it can be observed that the proposed CMRC by suppressing third harmonic (7.2GHz) makes square voltage waveform in drain while the quarter wave length transmission line make half-sinusoidal current waveform. Figure 3 (c) shows the load voltage waveform, which included only fundamental harmonic and verified the output matching circuit has a good performance. But this amplifier with CMRC is unstable therefor, a feedback between output and input of circuit for stability is used. Microstrip lines and a resistance are used in feedback design. The demission of microstrip lines are optimized. The aims of feedback design are increase stability factor ($k$) and preservation power added efficiency (PAE). Figure 4 (a) shows the stability factor and PAE of the proposed PA without feedback and figure 4 (b) shows the stability factor and PAE of the proposed PA without feedback and preservation PAE.
RESULTS
Figure 5 (a) shows efficiency and power added efficiency (PAE) of the proposed amplifier in range of output power. According to this figure maximum power added efficiency of 61% with output power of 20.2 dBm. Figure 5 (b) shows power gain and output power in range input power. Table 1 performance summary and comparison with other works.

Table 1. Performance summary and comparison with other works

<table>
<thead>
<tr>
<th>Ref.</th>
<th>Mode</th>
<th>Vdd(V)</th>
<th>f (GHz)</th>
<th>Gain (dB)</th>
<th>PAE%</th>
</tr>
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<tr>
<td>[2]</td>
<td>D</td>
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<td>0.05-0.07</td>
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<tr>
<td>[3]</td>
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<td>3.1</td>
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</tr>
<tr>
<td>[5]</td>
<td>F</td>
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<td>1.1</td>
<td>14</td>
<td>86</td>
</tr>
<tr>
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<td>F</td>
<td>3.1</td>
<td>2.4</td>
<td>-</td>
<td>80</td>
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<tr>
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<td>1.5</td>
<td>2.4</td>
<td>10.2</td>
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</tr>
</tbody>
</table>

CONCLUSION
This paper presents a class-F power amplifier with feedback and a CMRC as harmonic control circuit. The CMRC and the quarter wave length transmission lines creates zero impedance at the second harmonic and infinite impedance at the third harmonic. Moreover, to increase stability factor a feedback consists of transmission lines and a resistor is designed. Simulation results demonstrates PAE of 61% and output power of 20.2 dBm under 10 dBm input power. The proposed amplifier can be used in communication system.

References


