Learning with memristive devices: How should we model their behavior?

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***Abstract*—This work discusses the modeling of memristive devices, for architectures where they are used as synapses. It is shown that the most common models used in this context do not always accurately reflect the actual behavior of popular devices in pulse regime. We introduce a new behavioral model, intended towards the nanoarchitecture community. It fits the conductance evolution of Univ. Michigan's synaptic memristive devices. A variation of the model fits HP labs's memristors' behavior in the same conditions. Finally, we discuss using a simple example the importance of this type of modeling for learning architectures and how it can impact the behavior of the learning.**

Keywords-component; formatting; style; styling; insert (key words)

I. INTRODUCTION

In recent years, memristive devices have emerged as a fantastic opportunity for renewal in electronic systems. Memristive devices are a family of two-terminal devices whose resistance evolves according to the bias and currents they experience [1]. Different applications fields have been targeted for such technology. Memory and reprogrammable logic are probably the most direct application of memristive devices and other nanoscale switches [2]-[9]. A reinvention of logic using schemes appropriate to their device physics has also been proposed [10]. Most current proposals, however, do not exploit the multivalued resistance capability (analog memory) which is a fantastic property of some memristive technology. HP lab's original memristors [1] have this feature. It is present in Univ. Michigan's synaptic devices [11], and others [12],[13]. It has also been reported in memristive three-terminal devices (optically gated carbon nanotube FETs [14],[15], nanoparticle organic memory FETs [16], Palermo organic devices [17] and UCLA ionic transistors [18]).

A currently highly researched approach is to use such memristive devices as synapses for learning [19], since this may be a way to exploit the intermediate resistance states of the devices, with relaxed requirements on the controllability of such states. Various proposals go into that direction. Some use conventional artificial neural networks [20],[21], a concept that has been experimentally demonstrated in [15]. Some use novel approaches inspired directly by Biology (like amoeba learning [22]). Finally, a popular idea is to associate memristive devices with spiking neural networks (neural networks that compute with asynchronous spikes, like the brain). It has indeed been suggested [23],[24],[25] and shown experimentally [11] that memristive devices can implement a learning rule observed in biological synapses (Spike Timing Dependent Plasticity [26]). In different contexts, this rule has been shown to have important potential for machine learning [27],[28].

Such research could lead to particularly innovative electronic architectures and develop intelligent and low power electronic systems able to learn and to adapt themselves to their environment. Many explorations are now performed in this direction, both on devices and architectures. A serious difficulty for the "nanoarchitects" working in that field, however, is that the many memristive technologies that exist rely on different physics. Therefore, they can have extremely different behaviors, which can lead to different results if used for learning. To invent the applications of memristive technology, we have to rely on simplified models of devices. Are they sufficient? How do they compare with the actual technology developed in device labs, especially in "learning-type" situations?

In this paper, we review the most popular device models used to develop nano-architectures capable of learning with memristive devices and introduce a new one. We then compare these models with measurements from two popular technologies for use as synapses that rely on different physics: Univ. Michigan's nanoscale synapses [11] and HP Labs's TiO_2 memristors [1]. We explore strengths and weaknesses of the models and conclude how we believe memristive devices should be considered for studies involving learning.

II. MEMRISTOR MODELS FOR LEARNING

A. The original linear memristor model (model A)

Different models have been used by nanoarchitects for exploratory studies that aim at taking advantage of multivalued resistance capability of memristive devices. Actually, memristors were introduced by HP Labs using a simple model [1] taking inspiration from Chua's pioneering views on the "fourth passive element", the memristor [29]. In HP's model, a memristor of thickness D has two layers: one of low linear resistance R_{ON}, and the second (of thickness w) of high resistance R_{OFF}. The device resistance is therefore:

$$R = R_{ON}(D - w) + R_{OFF}\, w\,. \qquad (1)$$

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The front between the two regions evolves according to (where μ is the front mobility)

$$\frac{dw}{dt} = \mu \frac{R_{ON}}{D} i \ , \qquad (2)$$

which leads to:

$$\frac{dR}{dt} = \alpha i = \alpha \frac{V}{R} \ . \qquad (3)$$

(where we have introduced $\alpha = \mu(R_{OFF} - R_{ON})R_{ON}/D$). The resistance is additionally bounded between a minimum and a maximum value ($R_{\min} = DR_{ON}$ and $R_{\max} = DR_{OFF}$ respectively).

Using the devices for learning usually involves repeated, short voltage pulses that aim at changing the conductance of the devices only moderately [20]-[23]. Some learning proposals also involved more complex voltage pulses [24], but understanding the effect of constant voltage pulses is an important step in order to grasp how learning could be done with memristive devices. In addition, we focus primarily on conductance because it corresponds to the synaptic weights in the context of neural networks and thus has more significance than resistance for learning. If the voltage V during such a pulse is constant, the conductance of the device evolves as

$$\frac{dG}{dt} = -\alpha \frac{V}{R^3} = -\alpha V G^3 \ . \qquad (4)$$

This law leads to small conductance steps when conductance is low, and to large conductance steps when conductance is already high. The two top plots of Fig. 1 illustrate how this behaves in situation (the model parameters are listed in Table 1). On the left graph we apply a series of short "potentiating" (i.e. $V<0$ with the convention used within this paper) identical pulses and plot the conductance of the device after each pulse. The conductance increase starts slowly and accelerates sharply after 70 pulses until conductance reaches the maximum conductance of the device. On the right graph we apply a series of "depressing" (i.e. $V>0$) pulses. In this case, the conductance decrease starts rapidly and then slows down after 10 pulses. In both cases, the envelope of the curve conductance vs. N is in $1/N^2$ (where N is the number of pulses). In this paper, these two series of repeated pulses are the reference experiments to identify how memristive devices behave in a learning situation.

If we plot the device resistance instead of its conductance (top plots of Fig. 2), the same qualitative behavior is seen, but is not as sharp, the resistance steps being in $1/R$. The envelope of the curve is in *log N*.

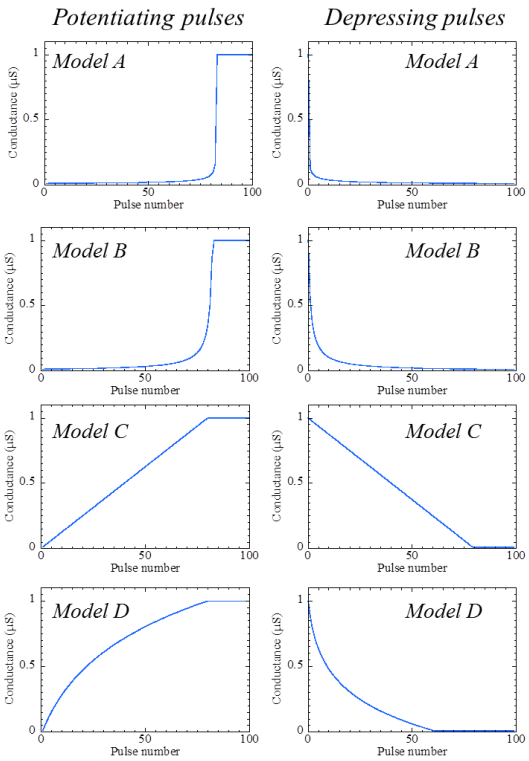

Figure 1. Conductance vs pulse number for a serie of "potentiating" (V=-1V) voltage pulses (left) and depressive (V=+1V) pulses (right) with the four devices models (pulse durations: 1 ms). From top to bottom: linear memristor (model A), threshold models (models B and C), asymmetric model (model D). Model parameters are listed in Table I.

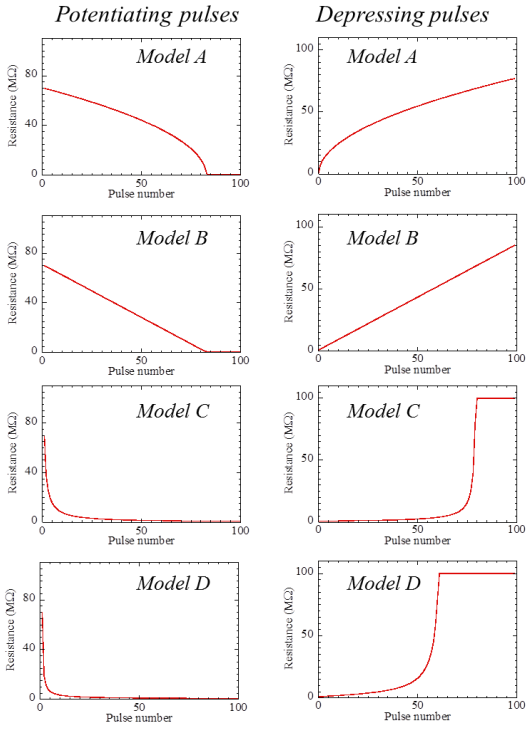

Figure 2. Same as Fig 1 with resistance plotted instead of conductance.

B. *Threshold model (models B and C)*

Though particularly helpful to understand how memristive devices work, the linear memristor model lacks important properties of actual devices. In this model, the time derivative of resistance is proportional to the current. This is not the case for actual devices that are all deeply nonlinear. Most devices even have a threshold voltage below which they experience no or little change [10],[11]. This makes a huge difference for nanoarchitectures since this allows probing the resistance state without changing it, and should be accounted for when designing them. Therefore, other models have been developed that include a threshold effect. We introduce the most commonly used model, for example by Snider [30], Pershin [22] or Linares-Barranco [24] (model B). The device resistance evolves as:

$$\frac{dR}{dt} = f(V), \tag{5}$$

where f is generally nonlinear, typically a hyperbolic or piecewise linear function, as illustrated on Fig. 3. This leads to (for a constant voltage pulse)

$$\frac{dG}{dt} = -G^2 f(V). \tag{6}$$

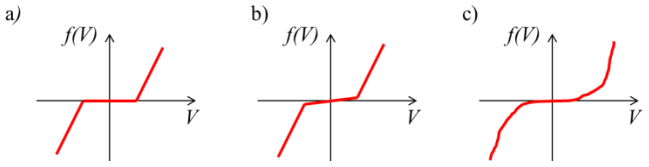

Figure 3. Examples of typically used f functions for equations (5) to (11), to model the nonlinearity of resistance change depending on the voltage applied across the device.

On the second line of Fig. 1 and 2, we illustrate the behavior of this model in the same test situation used for the linear memristor model. Conductance evolution (Fig. 1) is actually similar: potentiation (left graph) starts slow and accelerates, and depression (right graph) starts rapidly and decelerates. The envelope of the curve is $1/N$ instead of $1/N^2$ in the linear memristor case. The resistance (Fig. 2) has, however, a distinct and characteristic feature: it is a linear function of pulse number. This should be recognizable immediately on measured devices if they behave consistently with this model.

A variation (model C) is also used by nanoarchitects [21]. It consists of the same model, with conductance instead of resistance:

$$\frac{dG}{dt} = f(V), \tag{7}$$

which leads to

$$\frac{dR}{dt} = -R^2 f(V). \tag{8}$$

As illustrated on the third line of Figs. 1 and 2, the behavior is identical to model B, but with conductance and resistance inverted. On experimental devices, this behavior should be easily recognizable by the linear behavior of the conductance with pulse number.

C. *Asymmetric model (model D)*

We finally introduce a new model that we will show to have value in matching with device measurements. Unlike all the other models, the conductance change is asymmetric for potentiation and depression. For negative voltages (leading to increase of the conductance, or potentiation), we model the change of conductance with:

$$\left.\frac{dG}{dt}\right)_+ = f_+(V) e^{-\beta_+ \frac{G-G_{\min}}{G_{\max}-G_{\min}}}. \tag{9}$$

The more potentiated it is, the smaller the step. For positive voltages (depression), the expression is similar:

$$\left.\frac{dG}{dt}\right)_- = -f_-(V) e^{-\beta_- \frac{G_{\max}-G}{G_{\max}-G_{\min}}} \tag{10}$$

For the resistance, this translates to

$$\frac{dR}{dt} = -R^2 \frac{dG}{dt}. \tag{11}$$

The behavior of this model is illustrated on the last lines of Figs. 1 and 2. The conductance (Fig. 1) curves are different from that of the other models. Depression (left graph) starts rapidly and then slows down (in models A and B it starts slowly and accelerates, in model C it is linear). Potentiation also starts rapidly and then slows down (which is similar to models A and B). This asymmetry of potentiation and depression should be easy to recognize in experiments.

Resistance behavior (Fig. 2) is different due to the competition between R^2 and exponential in the resistance derivative, and may look different depending on the parameters of the model.

III. Confrontation With Current Technology

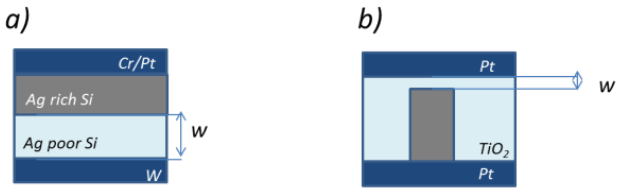

Figure 4. Schematization of the two kind of devices considered . a) **Univ Michigan nanoscale synapses**. The position of the front between Ag-rich and Ag-poor regions determines conductance, b) **HP Labs' TiO_2 memristors**.Conductance is determined by the thickness of a barrier at the end of an electroformed conductive channel.

A. *Univ. Michigan's nanoscale synapses*

We first study devices from [11]. They are a variation of the devices introduced in previous works [31],[32], but specifically targeted toward synaptic operation with continuous variation of the resistance (whereas the original devices had binary resistance, i.e. distinct low and high resistance states). The physics of these devices actually seems close to the original memristor model. Silver is cosputtered with the device thin film material (silicon), on top of a silver-free layer of thin film. An electric field moves the silver atoms giving rise to Ag-rich and Ag-poor regions, the width of which defining the device conductance (Fig. 4, a). Thus, unlike many resistive memory technologies and the group's previous samples, these devices do not switch by rupturing or reforming filaments (in which case a more binary switching behavior is obtained).

Fig. 5 plots (red diamonds) measurements on these devices reproduced from [11]. On the left plot, devices were subjected to brief -3.2 V potentiating pulses, and the conductance after each pulse (measured by 1 V read pulses) is plotted. On the right plot the same is done with depressing (2.8 V) pulses. Fig. 6 plots the corresponding resistance data. As seen on Fig 5 conductance can indeed be tuned finely by the short voltage pulses. However, neither the conductance nor the resistance is linear in respect to pulse number. This invalidates both models B and C for this technology. We also notice an extremely asymmetric behavior between potentiation and depression. They both start rapidly and then slow down. This invalidates model A. By contrast model D can fit the measurements (blue line in Fig. 1 and Fig. 2) and thus seems appropriate for architectural studies. More experimental data will be needed however to fit $f_+(V)$ and $f_-(V)$ for other voltages than those reported in [11].

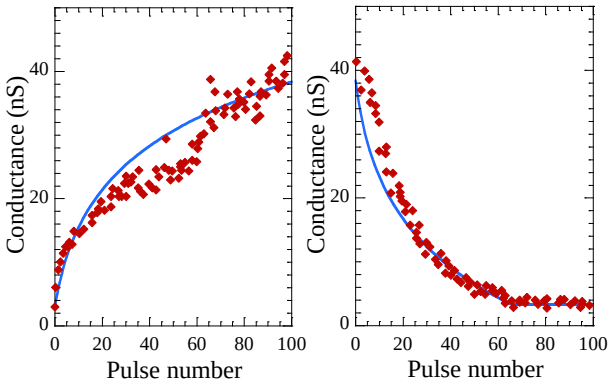

Figure 5. Evolution of the conductance for the devices from Michigan, fitted with the model D. Left: device conductance (measured at 1 V) after each pulse in a serie of potentiating (V=-3.2V) pulses. Right: same with depressing (V=2.8V) pulses. Diamond: experimental data, reproduced from [11]. Full line: Model D (parameters listed in Table I).

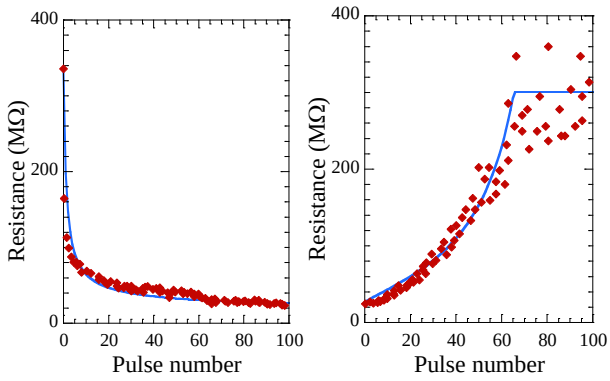

Figure 6. Same as Fig. 5 with resistance.

B. *HP TiO_2 memristors*

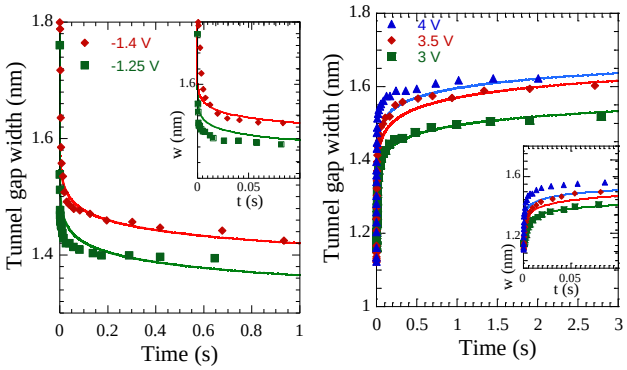

Figure 7. Tunneling gap width *w* as a function of time in a serie of potentitation (left) or depressing (right) pulses on HP memristors (symbols: experimental data from [33], full line: Model D), for different pulse voltages (left: -1.4 and -1.25 V; right: 4, 3.5 and 3 V). Insets show details of the figure for short times. Model D parameters are listed in Table I.

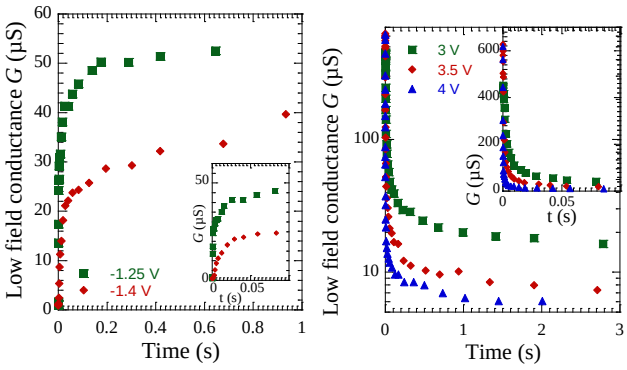

Figure 8. Low field conductance computed from tunneling gap width *w* from Fig 7 in the same conditions. For depressing pulse, conductance is shown in a log scale because of its abrupt change. The insets (details for short time) are both in linear scale.

HP Labs' TiO_2 memristors were first introduced with a simple physical interpretation [1]. The physical view has largely progressed with subsequent experiments and analysis [34],[35],[36]. Comprehensive characteristics of their dynamical behavior at room temperature were introduced in [33] and are used as a reference in this paper. The devices appear to operate via modulation of tunnel barrier width at the end of a conductive channel that was obtained by

electroformation (Fig. 4, b) [33]. The tunnel width w is the essential state parameter that can be connected to current by the model presented in [37] and in the supplementary information of [33].

In [33], the authors extracted the parameter w as a function of time t after potentiating and depressing voltage pulses. This is plotted on Fig. 7 (left: potentiating, right: depressing). This data was obtained by repeating voltage pulses whose duration was not constant. That is why the graphs are plotted as a function of time and not pulse number, and can still be read similarly to the previous plots of this paper. On Fig. 8, we converted w into a low field conductance using the well-established model given in [33]. Potentiation (left) starts with an extremely abrupt increase of conductance and then becomes a lot slower. Similarly depression (right) starts with an extremely abrupt decrease of conductance, and then becomes a lot slower. Among our models, only model D has this behavior. The initial increase or decrease of conductance is however so abrupt that Fig. 8 cannot be fitted by model D. Without any change, none of our device model is thus appropriate.

Interestingly, however, the evolution of w can be fitted roughly by the equations of model D, with w taking the place of conductance G (full lines of Fig. 7). The fit is not perfect, but can give an acceptable model of device behavior for architectural studies. Alternatively the full model given in [33] may be used, but is a lot more complex than model D.

The reason for which these devices (unlike Michigan's) cannot be fitted by model D directly seems to be due to the tunneling aspect of transport. If the conductance had a linear dependence on w, model D would work, but the conductance is rather an exponential function of w. This extremely abrupt start of the potentiation and depression would have significant impact if the device is used for learning.

IV. Discussion

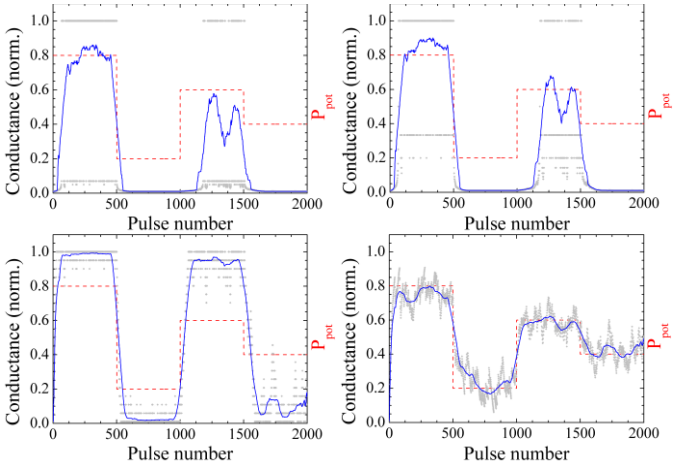

Figure 9. Conductance as a function of the potentiating / depressing pulses ratio for the four models described above. From top-left to bottom-right: linear memristor (model A, top, left), threshold models (models B, top, right, and C,bottom, left) and asymmetric model (model D, bottom, right). The dashed red curve is the probability P_{pot} of the pulse to be a potentiating pulse and the blue curve is a moving average of the conductance of the device.

We have seen in part II that the different models used for designing learning architectures with memristive devices lead to qualitatively different conductance evolution dynamics when voltage pulses are used to change the conductance (these pulses constituting a baseline at evaluating memristive device modeling for learning architectures). In that regard, a significant difference between the common models (A, B, C) and the new model D is that models A, B, C use symmetric equations for potentiating ($V<0$) and depressing ($V>0$) pulses, whereas model D uses asymmetric equations. In particular, for models A and B, this implies that if a device is in low conductance state, potentiating pulses (pulses that increase the conductance) have a small effect and a number of them is required before potentiation becomes efficient. Whereas with model D, for a device with a low conductance, the first potentiating pulses cause the most conductance change, and then potentiation slows down (assuming identical pulses). In part III, we have seen how two popular devices actually behave more like the new model D. Michigan's devices can be fitted by model D. In HP's devices, the state's variable w may be roughly modeled by model D, and the conductance switches abruptly when the device is in a low or high conductance state.

Now, how important is it to catch this behavior correctly when developing nanoarchitectures capable of learning? It seems to be significantly, in that the considered memristive device behavior can have significant repercussions on the learning strategy that needs to be put in place. To illustrate this point, we performed a simple computational experiment. We simulated the behavior of the four models for a series of 2000 pulses of either potentiating type (with a probability of P_{pot}) or depressing type (with a probability of $1 - P_{pot}$). In Fig. 9, we show the evolution of the conductance for each model for different values of the probability P_{pot} (0.8, 0.2, 0.6, and 0.4 successively). It is noteworthy that the mean conductance approximates the probability P_{pot} for the asymmetric model (model D). For the models A and B, the initial increase in conductivity being very slow compared to its initial decrease, the mean conductance stay close to zero for low values of the probability P_{pot}. The model C has a different behavior: since the conductivity change is independent of the current state of the device, the conductivity always tends to increase when $P_{pot} > 0.5$ and decrease when $P_{pot} < 0.5$ .The conductance of the device therefore does not stabilize to intermediate values with this simple scheme.

This illustrates that the type of learning will be different depending on the model used. In model A and B, low conductance states are extremely stable. In model C, the memristive device is naturally led to low or high conductance states that are more stable. In model D, depending on the model parameters, any intermediate resistance can be stable. Of course, the simple computational experiment presented above does not preclude the learning of stable arbitrary conductance states with devices best modeled by models A, B or C. It suggests, however, that the commonly used models that may look similar will give very different results regarding the final state of learning.

V. CONCLUSION

In this work, we first saw that the equations (linear memristor A, and threshold models B and C) commonly used to model the conductance change of memristive device in nanoarchitectures lead to significantly different behaviors when used with short voltage pulses. Such pulses are fundamental for nanoarchitectures involving learning. We then presented two memristive technologies targeted towards learning, and saw that their behavior matched none of these common models. For both devices, potentiation (the process that increases the conductance of the memristors) and depression (the processes that decreases it) are extremely asymmetric, which none of the three models captures. The new model that we introduced (asymmetric model D) corrects this issue and fits measurements on Univ. Michigan's synaptic devices directly, and after an adaptation measurements on HP Labs' original memristors. Finally, we pointed with a simple simulation that using one or the other of the models will change the stability of the memristors' states in a learning situation. All this suggests that existing memristors' models should be used with caution when developing this kind of architectures.

TABLE I. MODEL PARAMETERS USED IN THIS PAPER

Figure	Model parameters
Fig. 1, 2 model A	$\alpha = 1.25.10^{12}\,\Omega^2/V/ms$
Fig. 1, 2 model B	$f(1V)=-f(-1V)=0.85\ M\Omega/ms$
Fig. 1, 2 model C	$f(1V)=-f(-1V)=12.5\ nS/ms$
Fig. 1, 2 model D	$\beta_+ = 2.0$, $\beta_- = 3.5$, $f_+(1V)= 40\ nS/ms$, $f_-(-1V)=150\ nS/ms$
Fig. 1,2 all models	$G_{min} = 10\ nS$, $G_{max} = 1\ \mu S$
Fig. 5,6	$\beta_+ = 3.0$, $\beta_- = 2.8$, $f_+(1V)= 600\ nS/ms$, $f_-(-1V)=900\ nS/ms$, $G_{min} = 3.3\ nS$, $G_{max} = 40\ nS$
Fig. 7	*Potentation:* $\beta_- = 20.0$, $f_+(-1.4V)= 0.1\ mm/s$, $f_+(-1.25V)= 0.9\ mm/s$, $w_{min}=1.3nm$, $w_{max}=1.8\ nm$ *Depression*: $\beta_-(4\ V, 3.5\ V, 3\ V) = 14.2, 13.0, 14.8$, $f_-(4\ V, 3.5\ V, 3\ V) = 0.0026, 0.0028, 0.23\ mm/s$, $w_{min}=1.1nm$, $w_{max}=1.65nm$

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