On-Wafer Characterization of Silicon Transistors Up To 500 GHz and Analysis of Measurement Discontinuities Between the Frequency Bands

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Abstract— **This paper investigates on-wafer characterization of SiGe HBTs up to 500 GHz. Test structures for on-wafer TRL calibration have been designed and are presented. The TRL calibration method with silicon standards has first been benchmarked through EM-simulation. Passive and active components are then characterized up to 500 GHz. The slight discontinuities between the frequency bands are explored. A specific focus was placed on incorrect horizontal probe positioning as well as on probe deformation, resulting in a better assessment of possible measurement errors.**

Index Terms—S parameter measurement, probe station, THz, SiGe HBT, on wafer, calibration, de-embedding

I. Introduction

Sub-THz system development based on very advanced silicon transistors and especially Silicon Germanium bipolar-MOS (BiCMOS) technology opens new applications for medical imaging, security and also automotive applications like anti-collision radar [1]–[3]. The circuit design in this frequency range is very challenging and requires accurate model cards for active and passive devices. To this aim, precise characterization and modelling of the devices in the sub-THz frequency range is compulsory to optimize the circuit performance and to minimize the number of design to fabrication loops [4]. While very high frequency on-wafer measurement of III-V based devices and circuits have frequently been published [5], [6], [7], [8], and reported up to 750 GHz [9], [10], the characterization of transistors above 110 GHz on Si-wafers remains challenging [11]. Only very few demonstrations of transistor measurements at higher frequencies have been performed on silicon substrate [12]. Voinigescu et al. [13] have demonstrated measurement up to 325 GHz of an advanced SiGe HBT (hetero-junction bipolar transistor) showing results of S21 and H21 parameters as well as of the maximum available gain MAG. Calibration has been carried out with impedance standard substrate (ISS) and the calibration methods used were LRRM (line-reflect-reflect-match) and TRL (Thru, Reflect, Line). In [14], Deng et al. have presented an exhaustive set of S parameter measurements up to 325 GHz on HBTs from an advanced 55nm BiCMOS technology using a similar approach as [13] for calibration (LRRM on ISS). Finally, Williams et al. [15] have presented measurement results from an silicon on insulator (SOI) technology, where passive elements have been characterized up to 500 GHz, while the transistor measurement was performed up to 110 GHz. On-wafer TRL (and multiline-TRL) calibration was applied. Again Galatro et al. [16] have designed an on-wafer calibration-kit dedicated to transistor characterization. Measurement results are shown from 220 GHz up to 325 GHz.

The main issue related to off-wafer calibration with the ISS calibration-kit concerns discontinuities that are often observed from one frequency band to another frequency band. These discontinuities are attributed to spurious wave modes propagating into the substrate [7], to crosstalk [17] and to the different measurement environments: calibration is performed on ISS calibration-kit and the measurements are performed on Si substrate. For example in [9] and [11], different calibrations have been realized showing the limitations of calibrations on ISS compared to the on-wafer TRL. In [15], the TRL has been claimed as the calibration of reference for on-wafer measurements at microwave frequencies.

On the other hand, the difficulties related to on-Silicon wafer calibration are: the less ideal characterization environment for on-wafer measurement in terms of (i) substrate loss, (ii) back-end-of-line (BEOL) complexity and (iii) probe contact quality. For example, Williams et al. have reported the difficulty to perform repeatable measurements on aluminum pads that are commonly used in Silicon technologies [15] and the lower quality of microstrip lines on SOI substrate compared to microstrip lines using a benzocyclobutene (BCB) dielectric, when measuring S parameters in the sub-THz frequency range. In addition, discontinuities on measured S parameters between

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the different frequency bands (1-110GHz, 220-325GHz, 325-500GHz) are often observed [18]. But very broad frequency range measurements over the different frequency bands are mandatory for device modelling, model accuracy and validity assessment.

The aim of this paper is (i) to present the design of an on-Si wafer calibration-kit, (ii) to reveal a methodology to characterize passive devices and HBTs up to 500 GHz from a silicon BiCMOS technology and (iii) to investigate the different origins for the frequency band discontinuities.

The remainder of this work is organized as follows. Section II is dedicated to the analysis of the measurement results. To this aim, the test structures are exhibited, the EM simulation-based methodology is presented, and a thorough analysis of test structure measurements is performed by comparison to EM simulation using the same calibration technique. In Section III, measurement results are assessed versus simulation by evaluating the variation in probe tip planarity, positioning, probe overdrive and the impact of probe deformation. Conclusions are then drawn in Section IV.

II. Characterization Results of Passive Elements and SiGe HBT

To cover the frequency range from 1 GHz to 500 GHz, four measurement benches were used: An E8361A Vector Network Analyzer (VNA) from Agilent working up to 110 GHz using frequency extenders (N5260-60003) above 67 GHz. Furthermore for the other frequency bands 220-330 GHz (WR-3) and 325-500 GHz (WR-2), measurements were carried out with a four port Rohde & Schwarz ZVA24 VNA, coupled with Rohde & Schwarz VNA frequency extenders (ZC330 and ZC500, respectively). Despite the fact that we have the equipment to measure between 140 to 220 GHz, it was not possible to carry out the measurements. In fact, the geometry of the probe at port 2 is not compatible with the pad layout. The frequency extenders are installed on a SIGNATONE on-wafer probe station. The GSG probes used in this work are Picoprobe from GGB with a pitch of 50 µm in each frequency band. The signal power level is set to less than -32 dBm in the four bands for the measurement of active and passive elements. For all the frequency bands, raw on-wafer measurements have been carried out on dedicated test structures and the data have been processed by our in-house TRL calibration tool. A detailed description of the test structures is given in the following part.

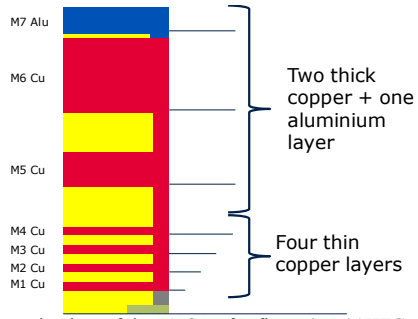


Fig. 1: Schematic view of the BEOL of Infineon's B11HFC process [19], [20].

A. Description Of Test Structures

The test structures have been designed in a 130 nm BiCMOS technology from Infineon featuring 6 levels of Cu metals (see Fig. 1). The last level of Cu metal used for the design of the microstrip line is 2.8 µm thick. The ground plane is made stacking metal level 1 up to metal level 4 and the dielectric thickness between ground plane and the line is about 4 µm. Pads have been designed for 50 µm probe pitch. The reference plane is positioned after the pad and a piece of line of 4 µm (see Fig. 2). Concerning the TRL calibration, the through and the lines standards have a length of 50 µm, 160 µm and 560 µm, (see Fig. 2 on the top left and in the middle). The 560µm line is used for the measurement between 13 to 120 GHz, while the 160µm long line is used from 70 GHz to 560 GHz. A pad-open was used as the reflect. The pad-open is composed by the pad including the 4 µm line only (see Fig 2 on the top right). Finally a load was employed to extract the characteristic impedance using the methodology described in [21].

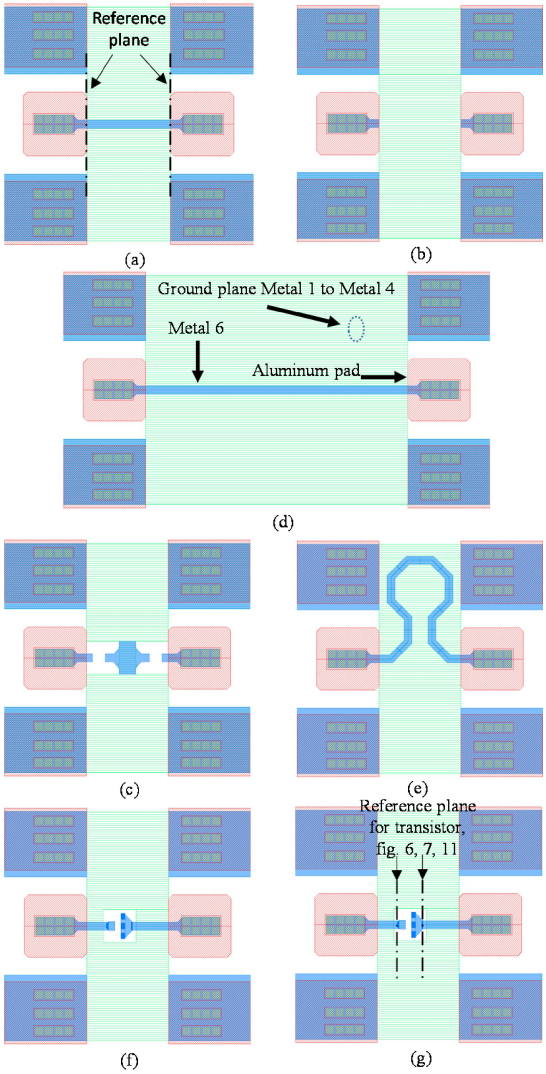
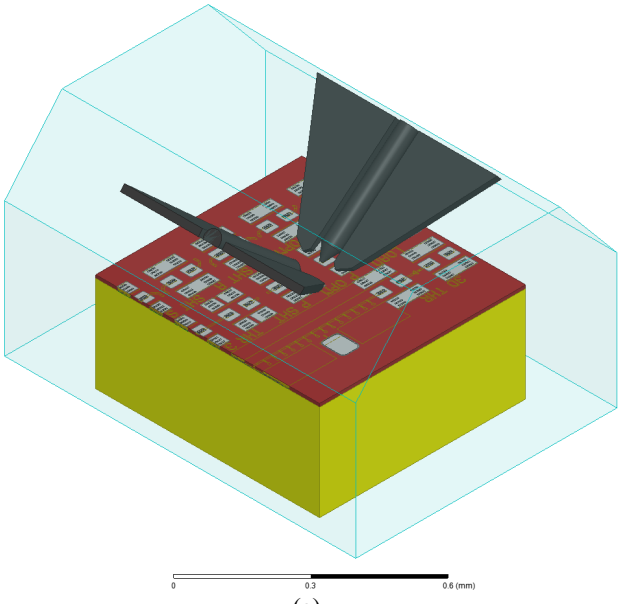


Fig. 2: Simplified representation of the layout of some of the test structures (through, reflect, line, transistor open, meander line, transistor): (green horizontal line) is M1 to metal 4 (Ground plane), blue dotted is metal 6, red right-hatched is aluminum used for the pad. The probe pitch is 50 µm. a) Thru of 50µm, b) Reflect, c) Line of 160µm, d) Load, e) Meander line, f) Transistor open, g) Transistor.

Doing so, we could take into account the characteristic impedance of the transmission lines and transform the reference impedance of the TRL calibration to 50 Ω. A SiGe HBT has also been embedded in the set of test structures. For de-embedding purposes dedicated transistor-open and transistor-short have been designed. The transistor-open test structure is identical to the transistor test structure except that the transistor itself has been removed: the BEOL contribution of both structures is identical down to M1. The same holds for the transistor-short. The transistor is removed and all the connections are shortened on M1. In addition, we introduced a meander-type line as passive test structure for comparison purposes of measurements vs. EM simulation[22].

B. Investigation Of On-Wafer TRL Calibration By EM Simulation

The test structures described above have been investigated by 3D-EM simulation. We employed the following EM simulation strategy: i) simulating all the intrinsic structures at the reference plane just after the pads (including the 4 µm line): an example of the intrinsic transistor-open structure is shown in Fig. 3b whereas the intrinsic meander line is highlighted in Fig. 3c; ii), the thru-reflect-line structures, the load structure as well as the transistor-open and meander line are simulated setting the ports at the CPW probe level as described in Fig. 3a. From these data we benchmark the TRL on-Si-wafer calibration for very high frequency using the following methodology: We apply the TRL calibration with the simulated test structures results including the probes and move the reference plane after the pads where the intrinsic part of the test structure begins. Then we compare the TRL calibrated simulation results with the first set of the simulation results corresponding to the intrinsic test structure only. Results are shown for the transistor open (see Fig. 4 a and b) and for the meander line structures (see Fig. 4 c and d for magnitude and phase or capacitance from the S parameters vs. frequency).



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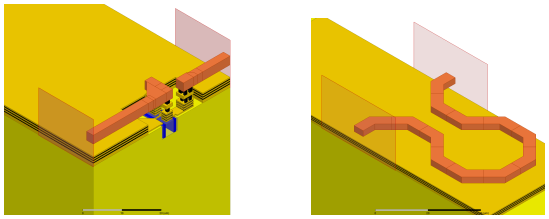
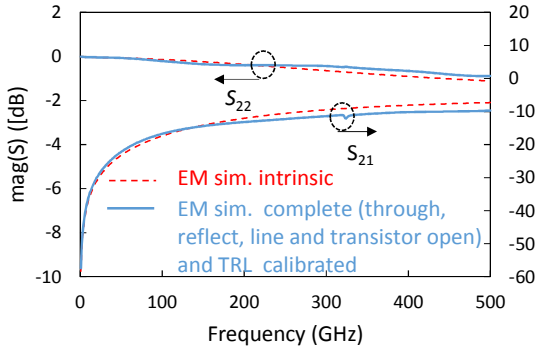


(b) (c)

Fig. 3: Geometrical model for EM simulation including neighboring structures of a) the EM full structure including probes, pad open and b) half intrinsic transistor open c) intrinsic meander line (wave ports correspond to reference plane of the TRL calibration). (gold: metal 1 bis metal 5, orange : metal 6, yellow: Si, brown SiO2).



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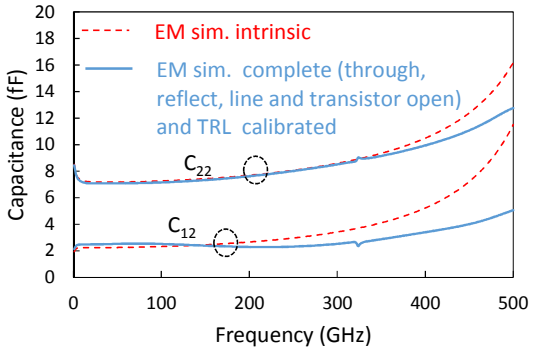

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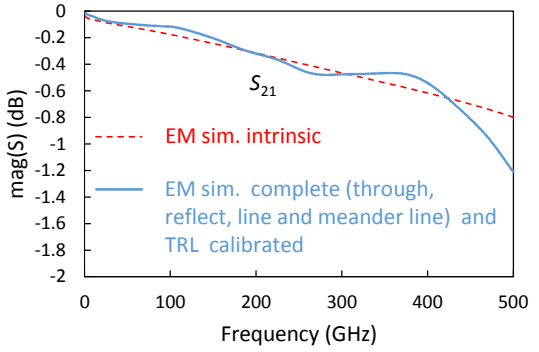

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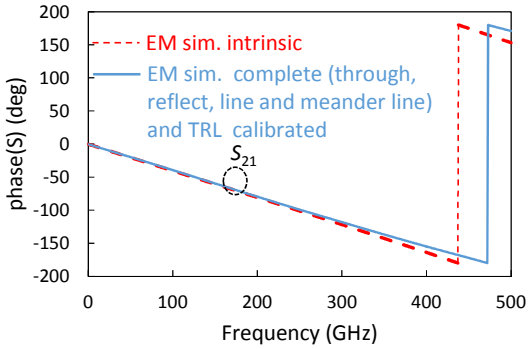


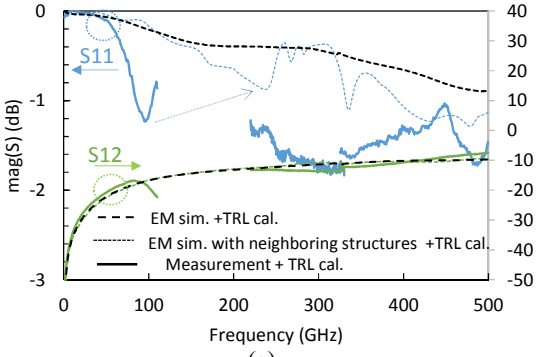
(d)

Fig. 4: Comparison of EM simulation of the on-wafer TRL calibration (blue) with EM simulation of the intrinsic device (red-dashed) for a) magnitude of S-parameter and b) capacitance for the transistor-open and c) magnitude of S-parameter and d) phase for the meander line.

Comparing the intrinsic test structure simulation results to the simulation results where the complete test structure has been simulated and the influence of probes and pads has been corrected through TRL calibration, we can recognize a high level of accuracy of the on-wafer TRL calibration at least up to 200GHz. From 200GHz up to 500GHz a small difference with respect to the intrinsic simulation results can be recognized. This may be due to coupling and crosstalk.

C. Measurements Of Passive Devices And Comparison To EM Simulation

In this part, calibrated measurement results and calibrated EM simulation results are compared using the same TRL calibration methodology. Fig. 5 presents the S-parameter measurements of the transistor-open and the meander line and its comparison to EM simulation up to 500 GHz. A good matching between simulation results and measurement results is observed despite the complexity of the BEOL. We can observe in the frequency band between 70 GHz and 110 GHz a resonance like behavior for S11 (decrease/increase) that appears in the measurement of the transistor-open, see Fig. 5a. This artifact does not appear when investigating the test structure as a standalone structure by EM simulation. As suggested in [23], we introduced adjacent structures corresponding to the layout in the EM simulator as depicted in Fig. 3a. For example, the pad-open has a pad short on its left, a pad load on its right, an open below and an integrated tuner above.



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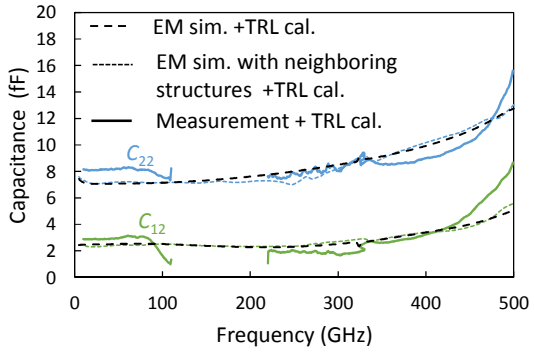

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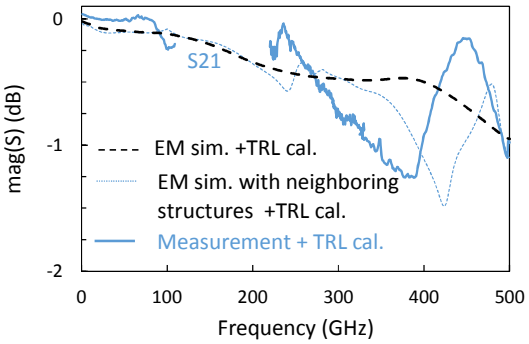

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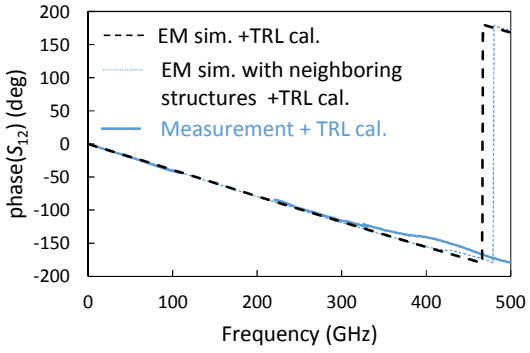


(d)

Fig. 5: S parameter measurements with on-wafer TRL calibration and comparison to several EM simulations for: a) magnitude of S parameters and b) capacitance of a transistor-open, c) magnitude and d) phase of a meander line up to 500 GHz.

Performing simulations including the adjacent structures, we are observing a decrease of S11 starting at 140 GHz and an increase at 220 GHz, see Fig. 5a. This decrease/increase of S11 is shifted in magnitude and frequency compared to the measurement. This difference is due to the simplified probe model that we used for EM simulation.

Also, concerning the meander line structure in the higher frequency range above 350 GHz, Fig. 5 c and d, we can observe when comparing simulation including adjacent structures versus measurements that the magnitude of the transmission S21 parameter does not show a monotonous decrease as predicted by the simulation of the standalone structure. Including the adjacent structures, the tendency of the measurement results is correctly reproduced but shifted in frequency range. Despite these imperfections, a quite good continuity in the different frequency bands is obtained up to 500

GHz for both, the reflection coefficients of the open as well as for the transmission coefficient of the meander line.

D. Characterization Of SiGe HBTs Up To 500 GHz

The on-wafer TRL calibration procedure described above has been used to measure a SiGe HBT from Infineon's B11HFC technology with a drawn emitter size of 0.22*1µm² with a 2*CBEBC configuration [19]. Moreover, since the reference plane after calibration is behind the pads, we shifted this reference plane using the TRL (phase shifting) to remove the M6 access line contribution (see Fig. 2) and set the reference plane in front of the M1-M6 via-hole stack. Doing so, we avoid the de-embedding steps. (The via-hole stack is considered as a part of the transistor.) Previous work showed that de-embedding is only valid up 170 GHz [24], other authors reported the validation range to be limited up to 60 GHz [11]. In fact, the validity depends on test-structure layout and on the applied de-embedding procedure itself. The M1-M6 via-hole stack is considered to be part of the transistor. The magnitude of the current gain H21 and of the unilateral gain is shown in Fig. 6 for different bias conditions: V_{BE} varies from 0.7 to 0.94 V by a 60 mV step and V_{CB} is set to 0 V.

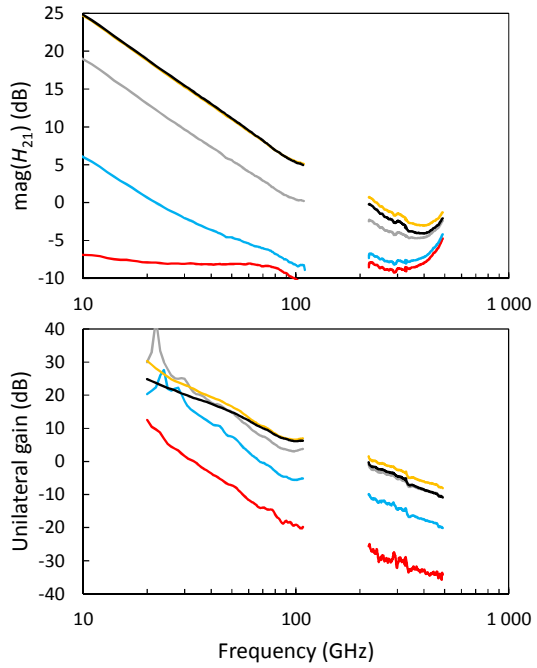


Fig. 6: Unilateral gain and Current gain H21 of a 2*CBEBC SiGe HBT of (0.22*1µm²) drawn emitter window size from Infineon for different V_{BE} ranging from 0.7-0.94 V with 60 mV step and V_{CB}=0 V, using an on-wafer TRL calibration with impedance correction, plus move of the reference plane above vias at M6 (see Fig. 2).

The magnitude and phase of the four S parameters are then shown in Fig. 7 for the same operation points. A decent continuity of the S parameters between the different frequency bands can be observed on both the gain and phase except for the phase of S22. The origin of the measurement discontinuities between the different frequency bands is explored in the next section. In fact, changing the frequency range involves a change of the measurement environment including the usage of different probes, but re-use of the same test-structure on the wafer.

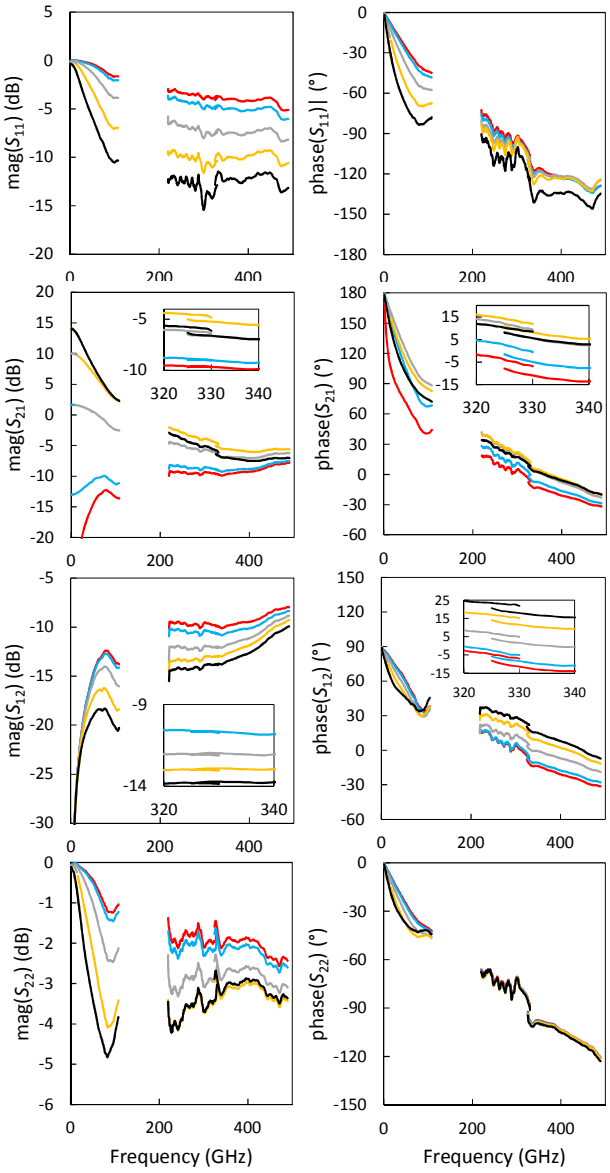


Fig. 7: S parameter measurements of a 2*CBEBC SiGe HBT of (0.22*1µm²) drawn emitter size from Infineon for different V_{BE} ranging from 0.7-0.94 V with 60 mV step and V_{CB}=0 V, using an on-wafer TRL calibration with impedance correction and move of the reference plane above vias at M6 (see Fig. 2); magnitude and phase.

III. Results Analysis and Measurements Uncertainties

A. CPW Probe Planarity And Impact On TRL Calibration.

The planarity control is a major adjustment step and must be carried out before starting the probe positioning. The planarity adjustment is achieved by observing the footprint of the probe tips on a test structure with the microscope. Identical footprints for the ground-signal-ground tips indicated perfect planarity. We need no specific tools to monitor the angle of the probe head. For further investigation, an EM simulation study has been performed to evaluate the impact of this probe rotation.
We compared two cases: (i) perfect planarity, (ii) one of the ground tips is not anymore in contact with the ground pad, position called "TILT 1". Then for each configuration, a

complete set of simulation has been done: The TRL structures such as through, reflect, line and the transistor-open have been simulated. Fig. 8 highlights the probe position in "tilt1" configuration. Please note that in the EM simulation study, the probe is considered as fully rigid while in the experimental case the CPW probe keeps the mechanical contact up to a larger tilt angle thanks to the flexibility of the probe.

In each tilt probe position, a TRL calibration is applied and the capacitance of the transistor-open is extracted for the port 2 (see Fig. 9). When losing the contact for position "tilt1", resonances appear especially around 120 GHz and the results becomes inaccurate.

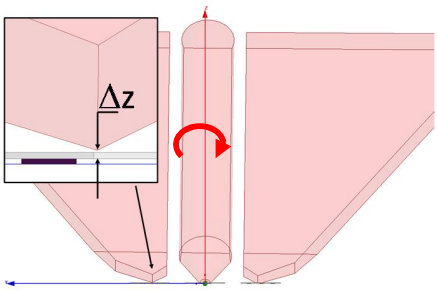


Fig. 8: EM model used for planarity of the probe (reference: Δz=0nm, tilt1: Δz=600nm contact is lost in the last case)

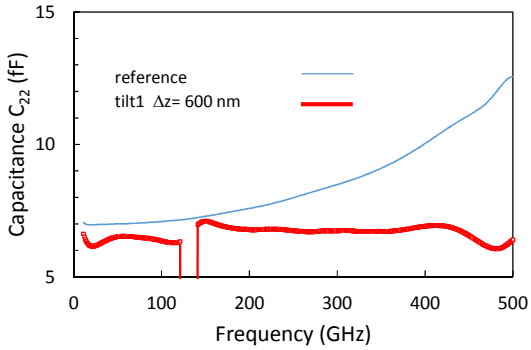


Fig. 9: Capacitance "C22" versus frequency of the transistor-open obtained from EM simulation including a TRL calibration with an ideal probe and with tilt default (reference: Δz=0nm, tilt1: Δz=600nm).

B. Probe Tip Positioning: Geometrical Analysis

For the measurements, a manual probe station was used to contact the probe tips to the pads of the test structures. Doing so, inaccuracies in the probes' positioning may occur due to the mechanical precision of the equipment and to the dexterity of the user. 3D images using an optical interferometer have been taken of the pads (thru, reflect, line, transistor, open) after one probe contact showing the footprint of the probes (see Fig. 10). These images highlight some discrepancies in the probe contact positioning in term of X, Y and also in term of pressure (Z) from test structure to test structure. A cross section in the middle of the signal pad from one signal pad to the other one has been carried out on each contacted test structure (see Fig 9). We can recognize a difference in x positioning of +/-3 µm for the port 1 and of +/-4 µm on port 2. Moreover, we can identify a slight difference of depth for each contact which is about +/-0.5µm. The origin is a difference in pressure or overdrive when manually contacting each pad. This pressure can slightly modify the symmetry of the GSG probe head fingers and eventually the electrical properties such as the characteristic impedance. The latter is of particular concern for CPW probe types.

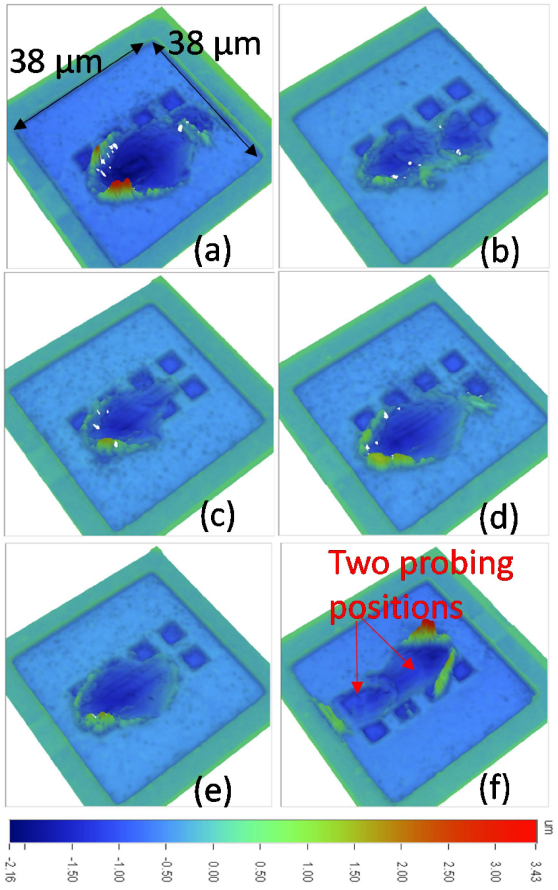


Fig. 10: 3D imaging of the signal pads used in the WR-2 band (a) line Port 1, b) reflect Port 1, c) through Port 1, d) transistor-open Port 1, e) transistor Port1, f) line Port 2). Images are taken with optical interferometry. Images of the line Port 2 show two probe contacts at different positions on the pad.

To get a clear picture of the issues concerning probe positioning in X, Y, Z direction, S parameter measurement results are analyzed and compared to EM simulation, as will be shown in the following part.

C. Probe Tip Positioning: Electrical Analysis

In the ideal case, calibration standards, test structures and devices have all the same distance between port one and two avoiding the movement of the probe heads when measuring the different components. But when using the TRL calibration method, the measurement of the Line standard involves an increase of the probe to probe distance. This modification is usually performed manually and can entail some inexactness in the probe positioning on the pad. Hence, in this part, we are investigating a voluntary wrong positioning in X direction on the pad of the Line standard during a TRL calibration: a raw measurement of the Line in the frequency band (325-500 GHz) is performed for two different positions of the probes, called line contact 1 & line contact 2. We estimated the difference between the two positions of the probe to be about 17 µm thanks to the above described 3D images obtained with an optical interferometer (see Fig. 10). The trace of the two different

contacts can be observed on Fig. 10f. A raw measurement of each test structure is also carried out (thru, reflect, transistor, transistor-open, and meander line). Two sets of TRL error terms have been calculated using for set 1: through, reflect, load and line contact 1, for set 2: through, reflect, load and line contact 2. Finally, we performed the calibration of the meander line, the transistor open and the transistor measurements with the two calibration sets and compared the results. In order to strengthen the results, we applied the same methodology through the EM simulation. Doing so, we get rid of the contact problem that may occur in real measurements.

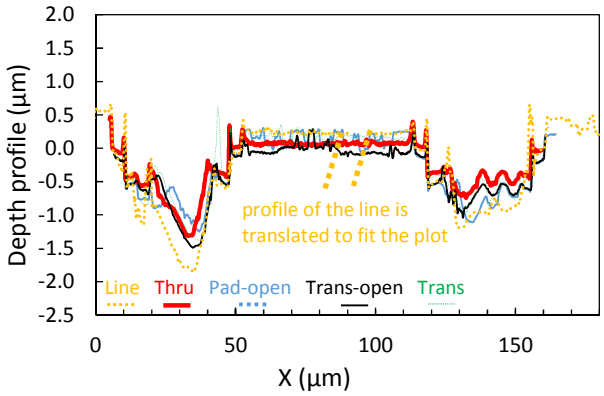
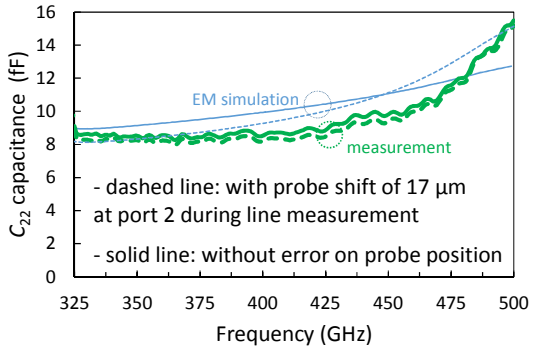


Fig. 11: Depth profile of the test structures (from Port 1 signal to Port 2 signal pads) after probing, highlighting probe positioning – measurement performed with an optical interferometer. Note that the profile of the line has been cut and has been translated to over-impose the profile at the pad position

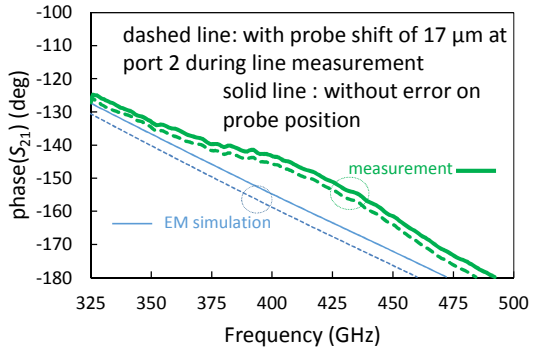
Figure 12a shows the capacitance of the transistor open for the two calibration sets in the 325-500 GHz frequency band. The inaccuracy in probe positioning introduces an error of 0.4 fF for this capacitance, which is about 3%. EM simulation results reveal a similar trend. The same procedure is applied to the meander line. In Fig. 12b we can recognize a phase shift of about 3° in the measurement and 4° in the simulation at 500 GHz.

Finally, we employed the two calibration sets on the SiGe HBT measurements. The transistor is biased close to peak f_T with V_{BE}=0.9 V and V_{BC}=0 V, Magnitude and phase of the S parameters are presented in Fig. 13. We can observe a slight difference in magnitude and phase that is more pronounced for the magnitude of the S22 parameter as well as for the phase of the S11 and S22 parameter close to 500 GHz.

From the previous figures, we can say that the detected variation in magnitude and phase due to inaccurate positioning is not substantial if we consider the large positioning error introduced (17 µm) and cannot completely explain the discontinuities observed in Fig. 7 but can only be part of the explanation.



(a)



(b)

Fig. 12: Error introduced by inaccurate positioning of the probe during Line standard measurement when performing TRL calibration with ZC (characteristic impedance of the line) correction: impact on a) the capacitance of the transistor-open and b) the phase of the meander line. (solid line: TRL set 1 with contact 1, dotted line: TRL set 2 with contact 2)

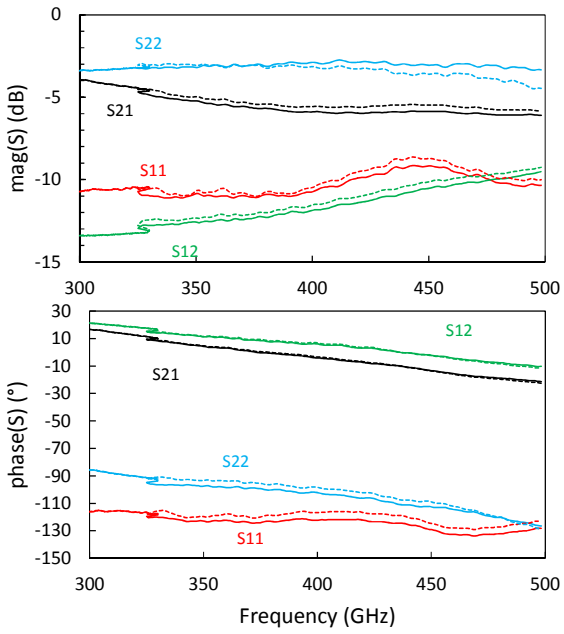


Fig. 13: Error introduced by inaccurate positioning of the probe during Line standard measurement when performing TRL calibration. Transistor measurement at V_{BE}=0.9V and V_{BC}=0V - TRL calibrated and ZC (characteristic impedance of the line) corrected S parameter measurement and same reference plane as Fig. 6 . (solid line: TRL set 1 with line contact 1, dotted line: TRL set 2 with line contact 2)

D. CPW Probe Deformation, Probe Characteristic Impedance And Impact On TRL Calibration.

CPW probes are particularly suited for very high frequency measurement due to their low insertion loss. Also, measuring up to 500 GHz implies using a small pitch distance for the probes (50 µm) which makes probe tips less rigid compared to the 100 µm pitch ones (for CPW probe type). When broadband measurements are required (e.g. 1 GHz to 500 GHz), the measurement must be performed for each single frequency band 1 GHz-110 GHz, WR5, WR3 and WR2, on the same test structures and each frequency range has its own probe tips. This procedure entails that the different probe tips have to be landed on the same pad several times, deteriorating the pad surface at each contact. Moreover, the mechanical pressure is not perfectly controlled when a manual prober is employed and the applied force on the probe can introduce deformation of the probe tip geometry, in particular when pads are re-contacted several times. This deformation may engender an alteration of the probe geometry and especially the variation of the gap between the central conductor and the ground involves a modification of the characteristic impedance. Fig. 14 shows an unaltered probe tip before the contact (Fig. 14a) and an altered one after the contact (Fig. 14b). It clearly highlights a deformation of the probe tip when contacting a pad of a test structure that has already been contacted before. It should be mentioned at this point that this deformation is reversible: the center finger moves back to its original position when lifting off the contacts. In order to quantify the impact on measurement accuracy caused by a probe deformation, an EM simulation reproducing this principle of probe deformation is carried out. Hence, a set of test structures including the probe tip and its deformation are simulated. From the simulated through, reflect, line and load results, a TRL calibration is performed. The obtained error terms are used to calculate the intrinsic device characteristics of the transistor-open test structure. The procedure is repeated by introducing a deformation of the probe tip as described above when simulating the transistor open. We assume a rotation around the vertical axes (see Fig. 14c) of the signal tip which deviates horizontally of 3µm and 6µm at contact of the signal tip. The results are presented in Fig. 15. The simulation shows that the impact of probe tip deformation introduces a large discrepancy appears on the whole frequency band.

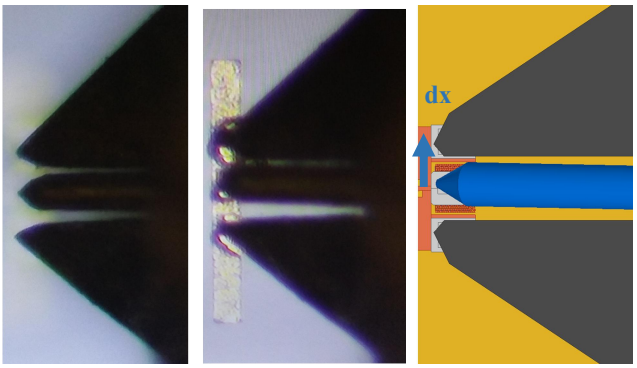


Fig. 14. Image of a 50 µm pitch CPW probe a) before contact and b) after contact on a used ISS short standard. The probe flexibility in combination with a deteriorated ISS standard causes a deformation of the probe eventually modifying its characteristic impedance; c) Geometrical Model for EM simulation showing a default on CPW probe (dx=6µm movement at port 2).

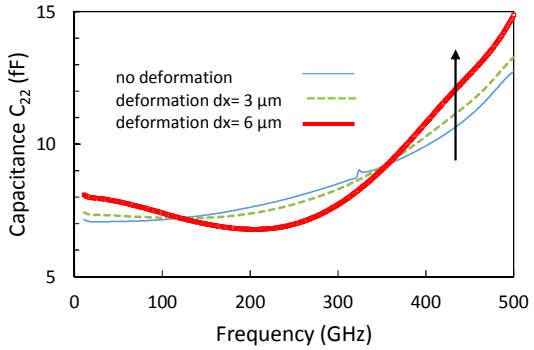
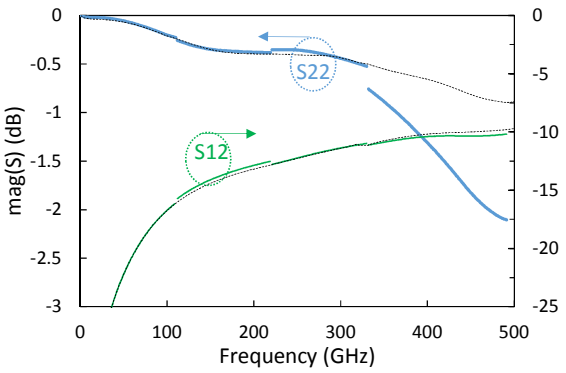


Fig. 15: Capacitance "C22" versus frequency of the transistor-open obtained from EM simulation including a TRL calibration with an ideal probe and with defaults (dx=3µm, sx=6µm) when simulating the transistor open.

E. Analysis Of The Results

In order to illustrate the effect of imprecise probe positioning and its associated deformation, we have arbitrarily combined some EM simulation data that include these faults doing the TRL calibration and applying the resulting error terms for the calculation of the intrinsic device characteristics of the transistor-open test structure. In the first frequency band (1-110 GHz), we assume a wrong positioning of the probe of -15 µm for the Line Standard. On the second frequency band (WR-5: 140-220 GHz), we consider again a wrong positioning of the probe of +5 µm for the Line Standard. On the WR-3 frequency band (220 GHz-330 GHz), we assume that two effects are combined with a wrong positioning of -5 µm of the probe tip on the pad of the Line standard combined with a deformation of the probe-tip of 3µm for the through standard. Finally, on the WR-2 frequency band (330 GHz-500 GHz) a probe deformation of dx=6µm is considered. Figure 16 shows the magnitude of the S parameters and capacitance for the transistor-open. We can recognize some discontinuities at the band edges in both, the magnitude and phase. In that example, the maximum jump in magnitude is 0.25 dB in S11 and about 0.4 dB in S12 which is lower than in the experimental data. In the same example, the maximum capacitance jump is about 0.5fF, which is about the same order of magnitude compared to the measurement (see Fig. 5 for measured data). The larger discontinuities in the magnitude of the measurement can also be attributed to issues related to contact quality on aluminum pads which is a major challenge for high quality measurement as already analyzed in [15].



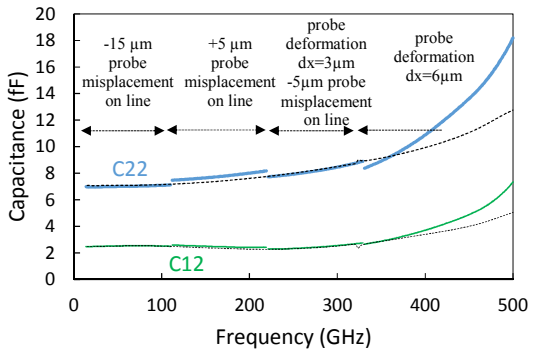


Fig. 16: EM simulation results after calibration of the transistor-open. During calibration errors have been introduced due to not-centered positioning and deformation of the probe-tip with different errors for each frequency band. Dashed line represents ideal results and solid line represents the impact of the introduced errors during TRL calibration.

IV. Conclusion

A BiCMOS technology has been characterized up to 500 GHz. The on-wafer TRL calibration procedure has been verified first through EM simulation, and second by comparing EM simulation with measurement results. The methodology is then applied to the SiGe-HBT over the full frequency range in a large bias range. Starting from these measurements, an analysis of the origin of discontinuities from frequency band to frequency band is performed. Three different sources have been investigated and their impact is quantified: (i) planarity, ii) incorrect horizontal probe positioning and (iii) probe deformation. We have shown, that a combination of both errors can explain partly the discontinuities between the frequency bands. Future work will be dedicated to investigation of substrate coupling, optimizing the design of the test structures and probe contact quality. The latter may also have an impact on discontinuities between the different frequency bands, in particular for the magnitude. Finally, the VNA precision and contact repeatability have not been investigated here but they must be considered when evaluating the global quality of a measurement.

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